Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt296

27 MHz VideoNet™ TTL-to-10KH ECL 11-Bit Translator

Distinguishing Features

- Latched TTL-Compatible Inputs
- 10KH ECL-Compatible Parallel Outputs
- PLL Operation for Stable Timing
- Separate TTL and ECL Supply Pins
- TTL-Compatible Control Inputs
- 68-pin PLCC Package

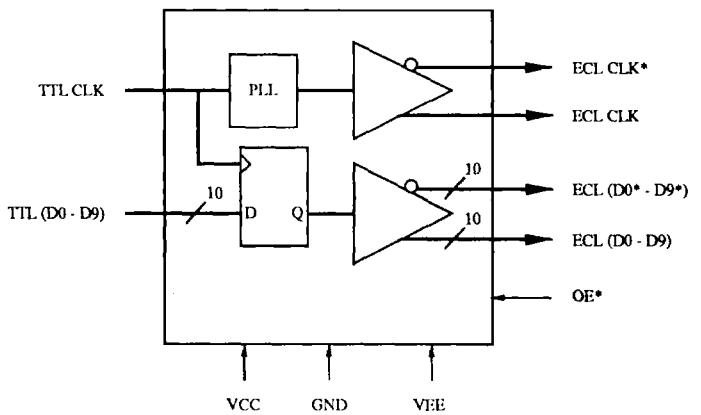
Applications

- CCIR601
- SMPTE RP125
- EBU 3246-E

Related Devices

- Bt297

Functional Block Diagram



Product Description

The Bt296 TTL/ECL Translator converts 11 bits of TTL data to 11 bits of differential 10KH ECL data.

In many cases involving the transmission of digital video signals, differential ECL signals levels are used. In addition, the phase relationship between the clock and data signals (and between data signals) is tightly defined. Thus, the TTL video data must be converted to ECL levels, and the phase relationship between clock and data adjusted to compensate for part-to-part output delay variations of TTL devices.

The Bt296 incorporates all translators in one package to eliminate delay skew that results when using multiple devices. A 10-bit data path is supported for high-end systems and compatibility with future products.

The clock-to-data timing on the ECL outputs is controlled by the on-chip PLL, enabling CCIR601, EBU 3246-E, and SMPTE RP-125 timing requirements to be met without adjustment. In addition, the ECL CLK outputs have a 50% duty cycle regardless of the TTL CLK duty cycle.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L296001 Rev. B

Brooktree®

Pin Descriptions

Pin Name	Description
TTL (D0–D9)	TTL data inputs (TTL compatible). They are latched on the rising edge of TTL CLK, converted to differential ECL levels, and output onto the ECL (D0–D9) and (D0*–D9*) pins. Unused pins should be connected to GND. In 8-bit systems, TTL D0 and TTL D1 should be connected to ground, using the TTL D2 (LSB)–TTL D9 inputs for the 8 bits of data.
TTL CLK	TTL clock input (TTL compatible). The rising edge of TTL CLK latches the TTL D0–D9 data.
ECL (D0–D9), ECL (D0*–D9*)	Differential ECL data outputs (ECL compatible). These are open emitter-follower outputs.
ECL CLK, ECL CLK*	Differential ECL clock outputs (ECL compatible). These are open emitter-follower outputs.
OE*	Output enable control (TTL compatible). A logical one forces the ECL outputs low and the ECL* outputs high (both data and clock) asynchronously to the clocks.
REXT	VCO free-running control. A resistor between this pin and GND sets the free-running frequency of the VCO. For 27 MHz, a value of 4220 ohms is recommended.
LF	Loop filter pin. The loop filter for the PLL is connected between this pin and GND. See Figure 1 (resistor values are in ohms, capacitor values are in µF).
VCC	TTL power supply. All VCC pins must be connected together as close to the device as possible.
GND	Ground. All GND pins must be connected together as close to the device as possible.
VEE	ECL power supply. All VEE pins must be connected together as close to the device as possible.

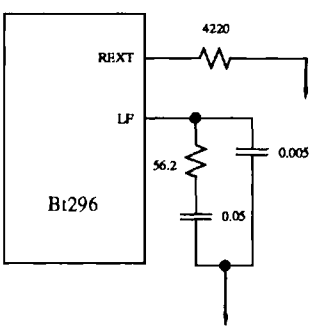


Figure 1. PLL Loop Filter (27 MHz Clock, 100 KHz Loop Bandwidth).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	GND	0	0	0	Volts
TTL Power Supply	VCC	+4.75	+5.0	+5.25	Volts
ECL Power Supply	VEE	-4.9	-5.2	-5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device, either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to GND)				-8.0	Volts
VCC (measured to GND)				+7.0	Volts
Voltage on Any ECL Pin		-1.8		GND	Volts
Voltage on Any TTL Pin		GND-0.5		VCC + 0.5	Volts
ECL Output Current				-50	mA
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ECL DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Output High Voltage*	VOH	0 +25 +70	-1020 -980 -920		-840 -810 -735	mV mV mV
Output Low Voltage*	VOL	0 +25 +70	-1950 -1950 -1950		-1630 -1630 -1600	mV mV mV
Output Impedance Output Capacitance				7 tbd		Ohms pF
VEE Supply Current**	IEE	0 +25 +70		55 55 55	70 70 70	mA mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL output loading of 50 Ω to -2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to GND.
**For power calculations, it is necessary to add an additional 330 mW due to emitter-follower devices.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device, either mounted in the test socket or on the printed circuit board.

TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	2.0		TTL VCC +0.5	Volts
Input Low Voltage*	VIL	TTL GND -0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			-0.7	mA
Input Capacitance			tbd		pF
VCC Supply Current	ICC		80	110	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to GND.

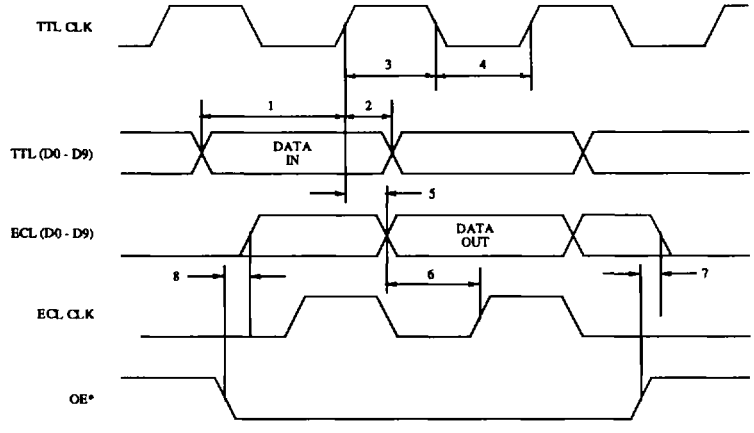
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL D0–D9 Setup Time	1	3			ns
TTL D0–D9 Hold Time	2	3			ns
TTL CLK High Time	3	10			ns
TTL CLK Low Time	4	10			ns
TTL CLK Input Rate	Fin	tbd		27	MHz
ECL D0–D9 Output Delay	5	tbd		10	ns
ECL D0–D9 Delay Skew*				3	ns
ECL CLK Output Delay**	6	(0.5 / Fin)–3	0.5 / Fin	(0.5 / Fin)+3	ns
ECL CLK Output Duty Cycle		42	50	58	%
PLL Acquire Time***					
100 KHz Loop Bandwidth				10,000	Clocks
1 MHz Loop Bandwidth				200	Clocks
Output Rise/Fall Time (20%–80%)		0.5	1	2	ns
Output Disable Time	7			15	ns
Output Enable Time	8			15	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL output loading of 50 Ω to –2 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Fastest/slowest (unipolar).
**Rising edge of ECL CLK relative to ECL (D0 - D9).
***At 27 MHz. Initial frequency offset of ± 30%, final residual frequency error of ±1 %.

Timing Waveforms



Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt296KPJ	68-pin Plastic J-lead	0° to +70° C