Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt294

27 MHz VideoNet™ YCrCb-to-RGB 8-bit Converter for 4:2:2 Video Applications

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Distinguishing Features

- NTSC and CCIR Compatible
- YCrCb to RGB Conversion
- 16-bit Multiplexed YCrCb I/O Bus
- 8-Bit Ancillary Data Output Bus
- Selectable Cr/Cb Interpolation Filters
- Optional Data Rate Doubling to 27 MHz
- Three 256 x 8 RGB Output RAMs
- Video Timing Recovery
- Programmable Color Key Output
- TTL Compatible Inputs and Outputs
- +5 V Monolithic CMOS
- 100-pin PLCC Package
- Typical Power Dissipation: 900 mW

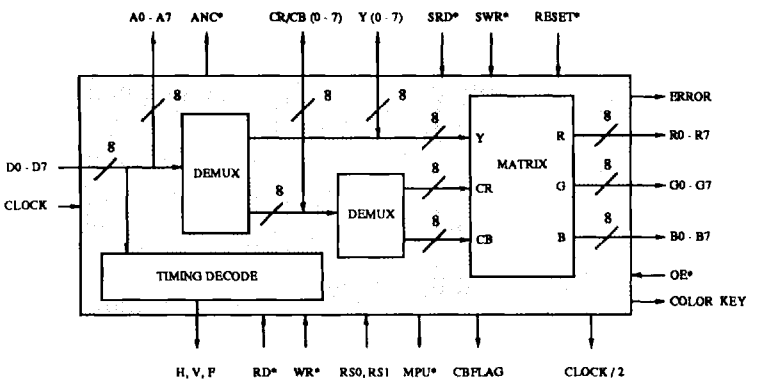
Applications

- CCIR601
- SMPTE RP125
- EBU 3246-E
- Image Processing and Capture
- YCrCb-to-RGB Conversion

Related Products

- Bt291, Bt297

Functional Block Diagram



Product Description

The Bt294 performs real-time YCrCb to RGB conversion. Eight bits of multiplexed YCrCb information are input and converted to RGB color information (8 bits each).

The incoming D0–D7 data has video timing information extracted, generating the horizontal blanking (H), vertical blanking (V), and field (F) outputs. Y and Cr/Cb data are demultiplexed, and available on the 16-bit Y and Cr/Cb I/O bus.

The Cr and Cb data are demultiplexed and interpolated data is generated using one of two interpolation filters, selectable by the MPU.

Ancillary data is detected and output onto the A0–A7 pins. ANC* is a logical zero while outputting Ancillary data.

Three 256 x 8 lookup table RAMs are provided, to support gamma correction, etc.

The output enable (OE*) control three-states the R0–R7, G0–G7, and B0–B7 outputs asynchronously to clock. YCrCb data (4:4:4 format) may also be output onto the RGB outputs.

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Detailed Block Diagram

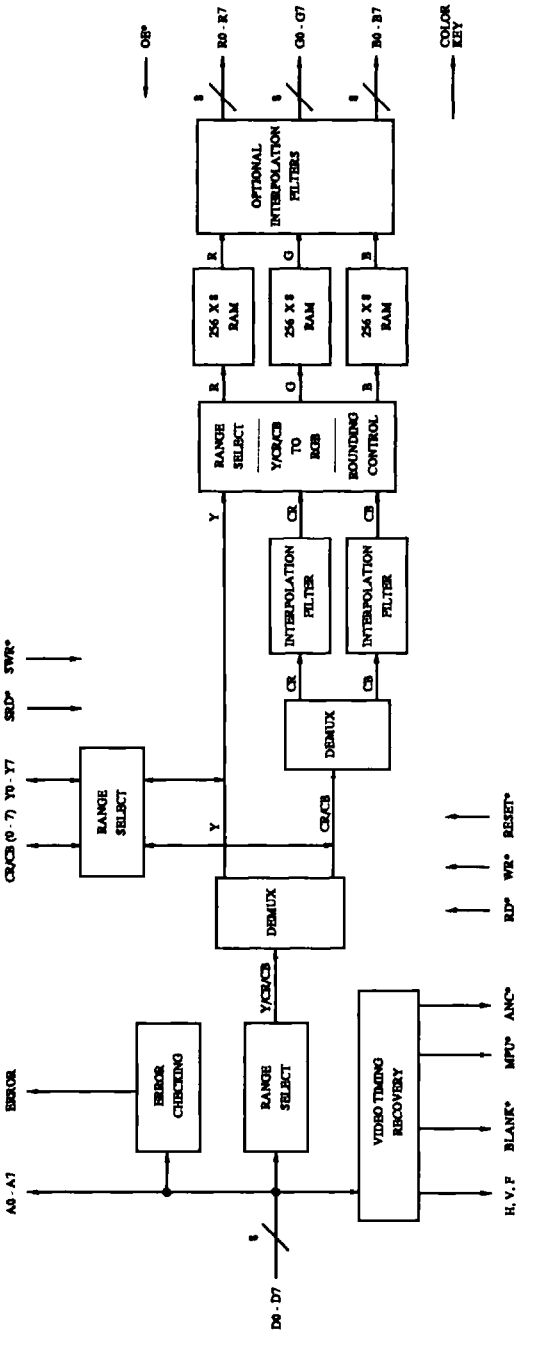


Figure 1. Detailed Block Diagram.

Circuit Description

Video Timing Recovery

The D0–D7 inputs are monitored for start of active video (SAV) and end of active video (EAV) sequences. (See Figure 1.) The SAV and EAV sequences are as follows:

$FF $00 $00 $xx

where $xx is defined as follows:

D7 = logical one
D6 = F (F = 1 for field 2; = 0 for field 1)
D5 = V (V = 1 during vertical blanking)
D4 = H (H = 0 at SAV, H = 1 at EAV)
D3–D0 = protection bits

After the necessary error-checking and correcting are performed, the H, V, and F signals are output onto their respective pins following the rising edge of CLOCK. The Bt294 corrects single-bit errors in the fourth byte of the SAV and EAV sequences; double-bit errors, and some multiple-bit errors, are detected and flagged (via the ERROR output), but not corrected. If there is an uncorrected error, the ERROR output pin will be a logical one for five CLOCK cycles, three CLOCK cycles after the error has been input via the D0–D7 inputs. Refer to the Application Information section for more details regarding the protection bits and their operation.

To ease system timing requirements, the RGB, YCrCb, CbFLAG, and H, V, and F outputs have the same relative output timing.

Note: a minimum of 36 CLOCK cycles must occur between the end of a SAV sequence and the beginning of an EAV sequence and between the end of a EAV sequence and the beginning of an SAV sequence. (See Figures 3 and 4.)

D0–D7 Color Data Recovery

If the CR07 command bit is a logical one, then, if the Y, Cr, or Cb input value is zero, it is made 1; if the Y, Cr, or Cb input value is 255, it is made 254.

If the CR07 command bit is a logical zero, then, if the Y input value is 0–15, it is made 16; if the Y input value is 236–255, it is made 235. If the Cr or Cb input value is 0–15, it is made 16; if the Cr or Cb input value is 241–255, it is made 240.

Outputting Ancillary Data

The ANC* output is a logical zero during the horizontal and vertical digital blanking intervals, except during the EAV and SAV sequences. All D0–D7 data is output onto A0–A7 unmodified.

Ancillary sequences can occur multiple times per scan line if different blocks of data are received.

The Ancillary input sequence via D0–D7 is:

$00 $FF $FF TT MM LL xx xx...

TT is the Ancillary data identification code, MM and LL specify the Ancillary data word count. xx are information data words.

While receiving the TT Ancillary data identification code, the parity is recalculated and checked against the transmitted parity bit (odd parity). If there is an error in parity, the ERROR output pin will be a logical one for five CLOCK cycles, three CLOCK cycles after the TT data has been input via the D0–D7 inputs. The TT data is output onto the A0–A7 outputs, following the rising edge of CLOCK.

Byte TT
A7 = D7
A6 = D6
A5 = D5
A4 = D4
A3 = D3
A2 = D2
A1 = D1
A0 = D0 (odd parity bit)

While receiving the MM and LL Ancillary data word count, the parity is recalculated and checked against the transmitted parity bit (odd parity). If there is an error in parity, the ERROR output pin will be a logical one for five CLOCK cycles, three CLOCK cycles after the MM or LL data has been input via the D0–D7 inputs. The MM and LL data are output onto the A0–A7 outputs, following the rising edge of CLOCK.

Circuit Description (continued)

Byte MM	Byte LL
A7 = D7 (output as received)	A7 = D7 (output as received)
A6 = M5 (D6)	A6 = L5 (D6)
A5 = M4 (D5)	A5 = L4 (D5)
A4 = M3 (D4)	A4 = L3 (D4)
A3 = M2 (D3)	A3 = L2 (D3)
A2 = M1 (D2)	A2 = L1 (D2)
A1 = M0 (D1)	A1 = L0 (D1)
A0 = D0 (odd parity bit)	A0 = D0 (odd parity bit)

While receiving the Ancillary data (xx), the parity is recalculated and confirmed against the transmitted parity (odd parity). If there is an error in parity, the ERROR output pin will be a logical one for five CLOCK cycles, three CLOCK cycles after the Ancillary data has been input via the D0–D7 inputs. The Ancillary data is output onto the A0–A7 outputs, following the rising edge of CLOCK.

Byte(s) xx
A7 = D7
A6 = D6
A5 = D5
A4 = D4
A3 = D3
A2 = D2
A1 = D1
A0 = D0 (odd parity bit)

Note that the number of Ancillary data words specified by the data word count are parity-checked by the Bt294. After the specified number of data words, parity checking is disabled until the next Ancillary sequence.

Line count ANC sequences (such as implemented on the Bt291) do not follow the standard Ancillary data format. Thus, upon reception of line count ANC sequences, error conditions may occur. No error will occur if the line count ANC sequence occupies the last six words of the digital blanking interval (as implemented on the Bt291).

Note: a minimum of 36 CLOCK cycles must occur between the end of a EAV sequence and the beginning of an SAV sequence.

SAV sequences take precedence over Ancillary data. Therefore, if a SAV sequence is received before the number of Ancillary data words (as specified by the Ancillary data word count) has passed, the Ancillary data sequence is aborted and no ERROR is generated.

Ancillary Data Blocks (NTSC)

During horizontal blanking, small blocks of data, less than 268 words in total length (including the ANC preamble), can be received within a horizontal blanking interval, starting with the end of EAV and terminating with the SAV.

During vertical blanking, large blocks of data, up to 1440 words in total length (including the ANC preamble), may be received with the interval starting with the end of the SAV and terminating with the beginning of EAV.

Ancillary Data Blocks (CCIR)

During horizontal blanking, small blocks of data, less than 280 words in total length (including the ANC preamble), can be received within a horizontal blanking interval, starting with the end of EAV and terminating with the SAV.

During vertical blanking, large blocks of data, up to 1440 words in total length (including the ANC preamble), may be received with the interval starting with the end of the SAV and terminating with the beginning of EAV.

YCrCb Demultiplexer

The YCrCb demultiplexer separates the Y (8 bits) and multiplexed Cr/Cb (8 bits) information using the SAV sequence as a reference.

CbFLAG is also generated using the SAV sequence as a reference. It is output aligned with the YCrCb I/O bus.

YCrCb I/O Bus

A 16-bit bidirectional multiplexed YCrCb bus is provided for reading and writing active video data. The SRD* and SWR* inputs are used to synchronously read and write YCrCb data. SRD* and SWR* must be synchronous to CLOCK. (See Figure 2.)

Circuit Description (continued)

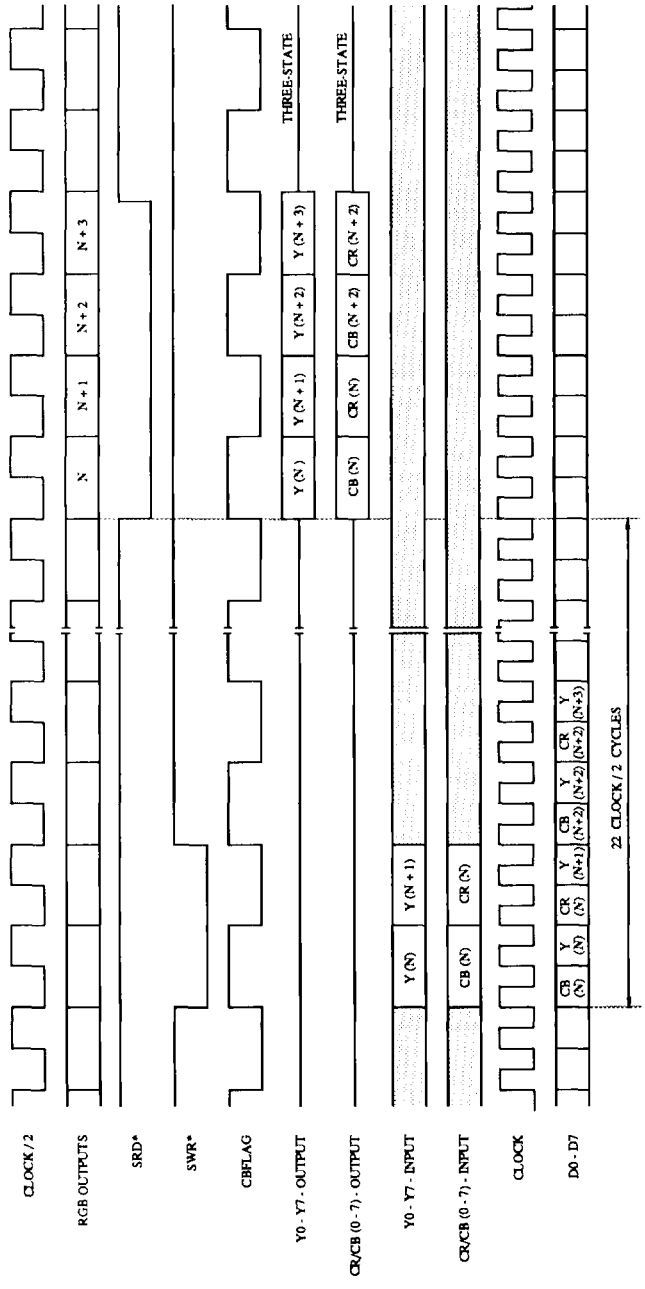


Figure 2. Reading/Writing Active Video Data (13.5 MHz RGB Output Rate).

Circuit Description (continued)

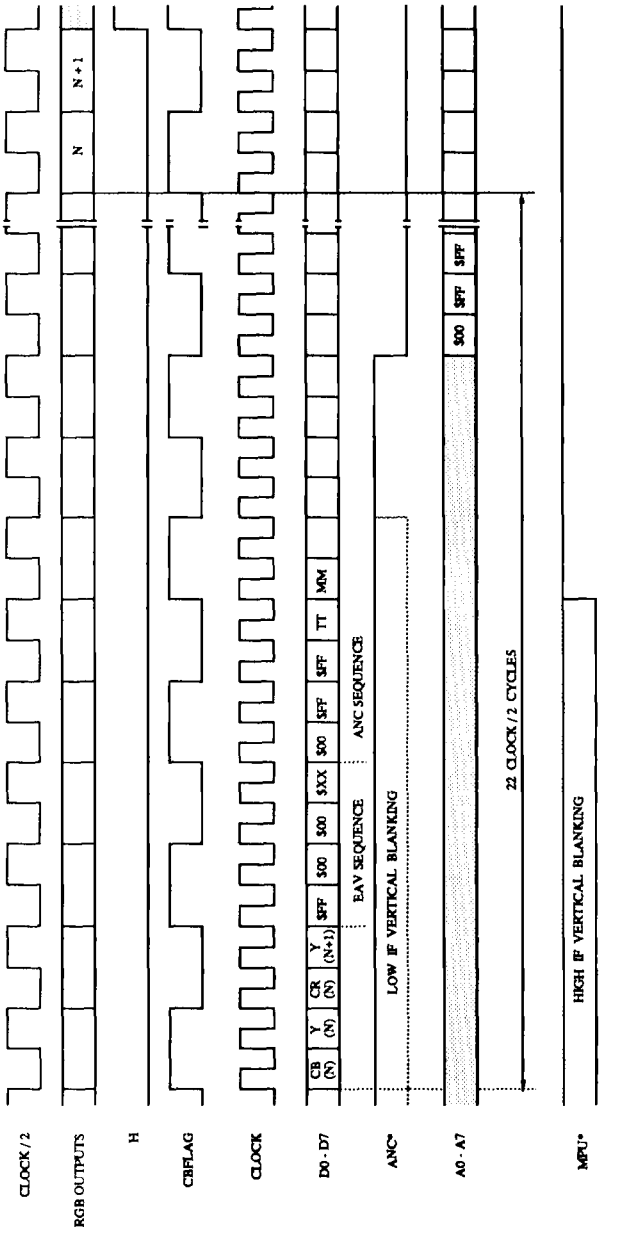


Figure 3. EAV Sequence and Reading Ancillary Data (13.5 MHz RGB Output Rate).

Circuit Description (continued)

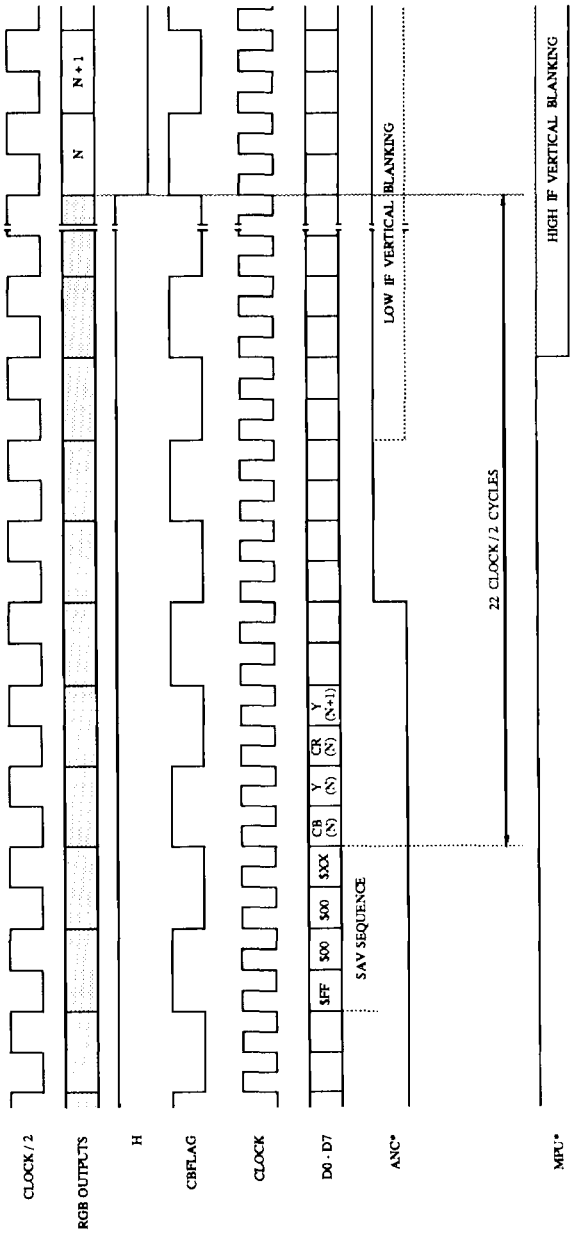


Figure 4. SAV Sequence (13.5 MHz RGB Output Rate).

Circuit Description (continued)

Reading YCrCb Data

While SRD* is a logical zero, YCrCb information from the RD0–D7 inputs is output onto Y (0–7) and CrCb (0–7) following the rising edge of CLOCK while CLOCK/2 is a logical one. Cb data is being output onto the CrCb bus while CbFLAG is a logical one.

The YCrCb output range is selected by the CR07 command bit:

(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR07 command bit is a logical one, then if the Y, Cr, or Cb output value is zero, it is made 1; if the Y, Cr, or Cb output value is 255, it is made 254.

If the CR07 command bit is a logical zero, then if the Y output value is 0–15, it is made 16; if the Y output value is 236–255, it is made 235. If the Cr or Cb output value is 0–15, it is made 16; if the Cr or Cb output value is 241–255, it is made 240.

If CbFLAG is a logical one, Cb data is present on the CrCb bus; if CbFLAG is a logical zero, Cr data is present. CbFLAG is output following the rising edge of CLOCK while CLOCK/2 is a logical one.

While SRD* is a logical one, the YCrCb bus is three-stated. Note: SRD* must be synchronized to CLOCK externally for proper operation.

Writing YCrCb Data

While SWR* is a logical zero, YCrCb information is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. This YCrCb information is used to generate the RGB output data, rather than the D0–D7 inputs.

The YCrCb input range is selected by the CR07 command bit:

(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR07 command bit is a logical one, if the Y, Cr, or Cb input value is zero, it is made 1; if the Y, Cr, or Cb input value is 255, it is made 254.

If the CR07 command bit is a logical zero, then if the Y input value is 0–15, it is made 16; if the Y input value is 236–255, it is made 235. If the Cr or Cb input value is 0–15, it is made 16; if the Cr or Cb input value is 241–255, it is made 240.

While CbFLAG is a logical one, Cb data is latched on the CrCb bus; if CbFLAG is a logical zero, Cr data is latched. CbFLAG is output following the rising edge of CLOCK while CLOCK/2 is a logical one.

CrCb Demultiplexer / Filters

The CrCb demultiplexer, using the CbFLAG signal, separates the 8 bits of multiplexed Cr and Cb data.

As Cr and Cb data are to be co-sited with the odd (first, third, fifth, etc.) Y samples, digital interpolation filters provide the even 8 bits of Cr and Cb data, converting the 4:2:2 YCrCb data to 4:4:4 YCrCb data.

YCrCb-to-RGB Matrix

The matrix converts the 24 bits of YCrCb data (8 bits each) to 24 bits of RGB data (8 bits each), and outputs the data onto R0–R7, G0–G7, and B0–B7.

The YCrCb to RGB conversion is selected by the command register and is either:

analog coefficient matrix:

$$R = Y + 1.402(Cr - 128)$$

$$G = Y - 0.714(Cr - 128) - 0.344(Cb - 128)$$

$$B = Y + 1.772(Cb - 128)$$

or digital coefficient matrix:

$$R = Y + 1.370(Cr - 128)$$

$$G = Y - 0.698(Cr - 128) - 0.336(Cb - 128)$$

$$B = Y + 1.730(Cb - 128)$$

Circuit Description (continued)

ROM lookup tables are used to perform the multiplications and 4 bits of fractional data are maintained. The final result is rounded to 8 bits as specified by command register_1. If the resulting R, G, or B value is less than zero, it is set to zero. If the resulting R, G, or B value is greater than 255, it is set to 255.

Note the digital coefficient matrix operates properly only when the YCrCb input range is Y = 16 to 235; Cr and Cb = 16 to 240 (the RGB output range will typically be 16 to 235). The analog coefficient matrix can handle the YCrCb input range of Y = 16 to 235; Cr and Cb = 16 to 240 (the RGB output range will typically be 16 to 235) or YCrCb = 1 to 254 (the RGB output range will typically be 1 to 254).

The YCrCb to RGB matrix may also be bypassed via the command register.

Output Lookup Table RAMs

Note that gamma-corrected RGB data is generated by the YCrCb to RGB matrix. The three output lookup table RAMs may be used to remove gamma correction on the R0–R7, G0–G7, and B0–B7 outputs in the event that they are to contain linear (rather than gamma-corrected) RGB data.

As the RGB data range from the YCrCb to RGB matrix is typically 16 to 235 (or 1 to 254), the lookup table RAMs may also be used to expand the range to 0 to 255.

The lookup table RAMs are not dual-ported, so MPU accesses have priority over pixel accessing. During MPU access to the color palette RAMs, the lookup table RAM outputs are undefined and invalid.

The lookup table RAMs are not initialized following a reset condition or power-up sequence.

RS1, RS0	CR03, CR02	ADDR0–ADDR7	Accessed by MPU
00	xx	$xx	address register
01	00	$00	red RAM location $00
01	00	$01	red RAM location $01
:	:	:	:
01	00	$FF	red RAM location $FF
01	01	$00	green RAM location $00
01	01	$01	green RAM location $01
:	:	:	:
01	01	$FF	green RAM location $FF
01	10	$00	blue RAM location $00
01	10	$01	blue RAM location $01
:	:	:	:
01	10	$FF	blue RAM location $FF
10	xx	$00	command register_0
10	xx	$01	command register_1
10	xx	$02	red color key register
10	xx	$03	green color key register
10	xx	$04	blue color key register
10	xx	$05	red color mask register
10	xx	$06	green color mask register
10	xx	$07	blue color mask register
10	xx	$08	reserved
:	:	:	:
10	xx	$FF	reserved
11	xx	$xx	reserved

Table 1. Internal Register Addressing.

Circuit Description (continued)

The RGB (or YCrCb) output rate may optionally be doubled to 27 MHz via the command register. In this mode of operation, the RGB outputs are updated every CLOCK cycle. The doubling of the data rate occurs after the lookup table RAMs.

Note that RGB data addressing the RAM is $00 during digital blanking intervals (including EAV and SAV sequences). When YCrCb data is selected as the output (CR06 is set to one), the lookup table is bypassed.

Output Enable Control

Command bit CR01 is logically gated with the OE* input, and the resulting value is used to control three-stating the R0–R7, G0–G7, and B0–B7 outputs asynchronously to the clocks as described in the Pin Descriptions section.

Color Key Output

The Bt294 generates a COLOR KEY output, determined by the color key and color mask registers. For a programmed color, or range of colors, the COLOR KEY output will be a logical one coincident with the specified color being output on the RGB outputs. COLOR KEY is output following the rising edge of CLOCK.

MPU Interface

The Bt294 supports a standard MPU interface (A0–A7, RD*, WR*, RS0, and RS1).

The MPU* output indicates when the MPU may access the Bt294 via the A0–A7 pins. A logical zero indicates MPU accesses may be done without contention with Ancillary data timing.

RS0 and RS1 are used to select address register (logical zero) or RAM location or control register specified by the address register (logical one), as shown in Table 1. The 8-bit address register specifies which control register or RAM location the MPU is accessing. The address register resets to $00 following a read or write cycle to location $FF. Write cycles to reserved addresses are ignored, and read cycles from reserved addresses return invalid data.

The address register increments after each MPU read or write cycle (except when reading or writing to the address register), and is not initialized. ADDR0 is the least significant bit and corresponds to bit A0.

As the MPU shares the Ancillary bus with Ancillary information, care must be taken that the MPU does not attempt to access the internal registers and lookup table RAMs during the digital blanking intervals. The MPU* output signal may be used to provide arbitration; while MPU* is a logical zero, the MPU may access the Bt294 without contention with any Ancillary data.

The rising edge of WR* latches A0–A7 into the selected register or lookup table RAM location. While RD* is a logical zero, the contents of the selected register or lookup table RAM location are output onto A0–A7.

Circuit Description (continued)

Typical Application

Figure 5 illustrates a typical application of the Bt294. The Bt294 converts the incoming D0–D7 data stream from the Bt297 ECL to TTL receiver, recovering video timing information, and reformatting the color data into 16 bits of multiplexed Y and Cr/Cb color data for loading into the frame buffer. Data from the frame buffer may also be clocked into the Bt294.

The Bt294 converts the YCrCb data into the RGB format for driving a true-color VIDEODAC and RAMDAC, such as a Bt101 or Bt473.

The RGB outputs may also be used to interface to an RGB frame buffer, rather than driving a VIDEODAC or RAMDAC, as shown in Figure 6.

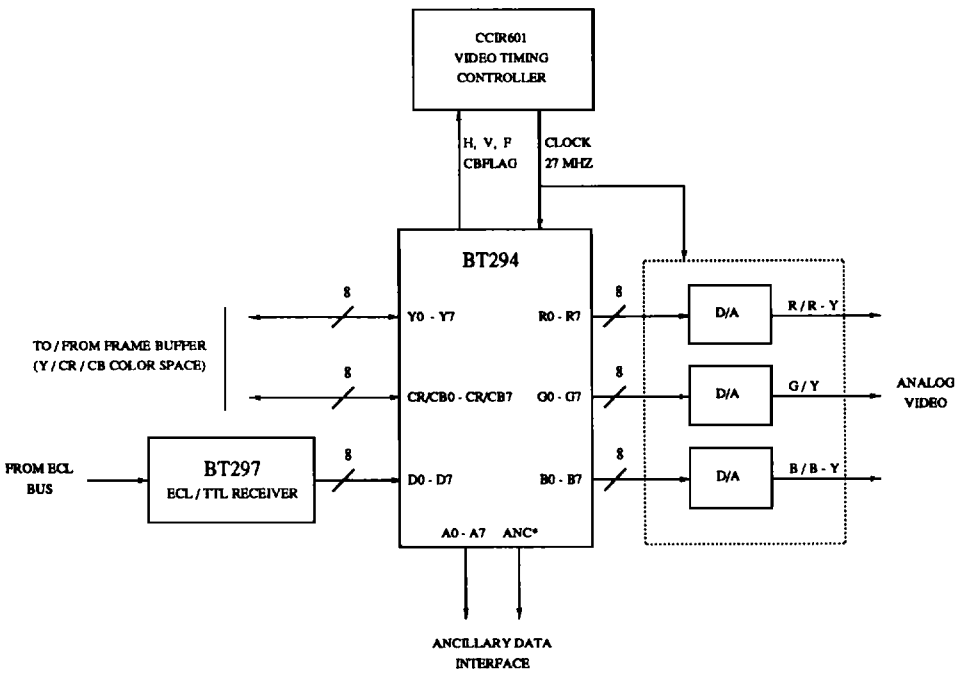


Figure 5. Typical Application.

Circuit Description (continued)

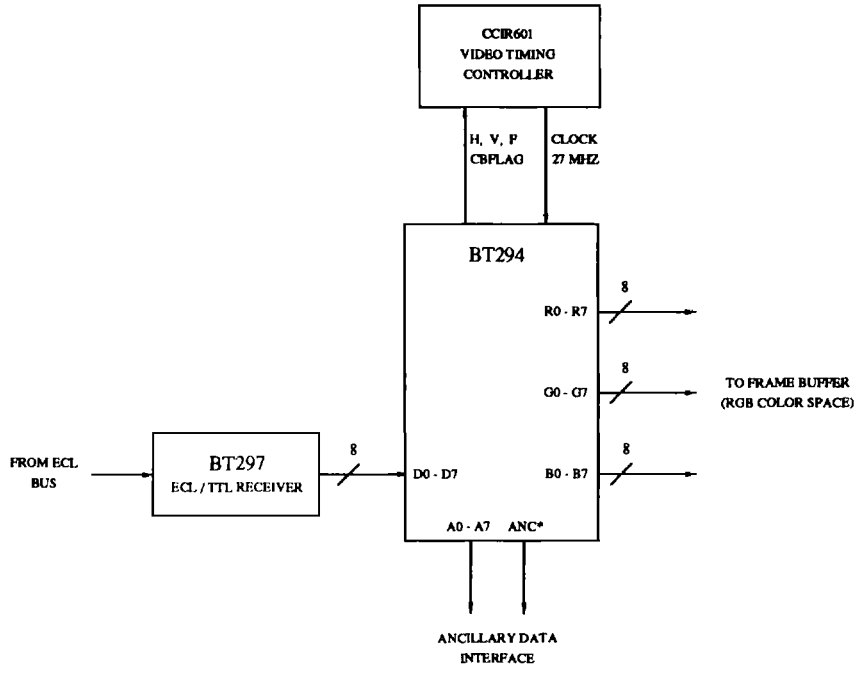


Figure 6. Typical Application.

Internal Registers

Command Register_0

This command register may be written to or read by the MPU at any time and is initialized to $03 following a reset condition. CR00 is the least significant bit and corresponds to data bit A0.

CR07	YCrCb range (0) Y = 16 to 235, Cr/Cb = 16 to 240 (1) Y, Cr, Cb = 1 to 254	This bit specifies the range of Y, Cr, and Cb on the YCrCb I/O bus (when inputting or outputting color data), and the D0–D7 color data. Typically, mode (0) should be used. Regardless of the selection, there is no change in the pipeline delay.
CR06	RGB or YCrCb output select (0) RGB (1) YCrCb	This bit specifies whether the RGB outputs are outputting RGB or YCrCb color information. Y information is output onto the G0–G7 outputs, Cr information is output onto the R0–R7 outputs, and Cb information is output onto the B0–B7 outputs. Regardless of the selection, there is no change in the pipeline delay.
CR05	13.5 MHz or 27 MHz RGB outputs (0) 13.5 MHz (1) 27 MHz	This bit specifies whether or not to double the data rate of the RGB data.
CR04	Cr/Cb interpolation filters select (0) use 12-tap filters (1) use 2-tap filters	This bit specifies which interpolation filters to use for the Cr and Cb data. Typically, the 12-tap filters should be used. Regardless of the selection, there is no change in the pipeline delay.
CR03, CR02	Lookup table RAM select (00) red lookup table RAM (01) green lookup table RAM (10) blue lookup table RAM (11) reserved	These bits specify which lookup table RAM the MPU is accessing.
CR01	RGB output disable (0) enable RGB outputs (1) disable RGB outputs	This bit is logically gated with the OE* input pin, and the resulting value is used to control three-stating the RGB outputs.
CR00	Matrix coefficient select (0) analog matrix (1) digital matrix	This bit selects which set of coefficients to use in the YCrCb-to-RGB matrix, as described in the text. Typically, the digital matrix should be used. Regardless of the selection, there is no change in the pipeline delay.

Internal Registers (continued)

Command Register_1

This command register may be written to or read by the MPU at any time and is initialized to 11xx xxxx following a reset condition. CR10 is the least significant bit and corresponds to data bit A0.

CR17, CR16	Rounding select (00) normal rounding (01) even rounding (10) reserved (11) Dynamic Rounding™	This bit specifies the type of rounding used. Regardless of the selection, there is no change in the pipeline delay. (00) specifies round up if the fractional data is ≥ 0.5. If the fractional data is < 0.5, the number will be rounded down. (01) specifies round up if the fractional data = 0.5 and the rounded result will be an even number (LSB = 0) or if the fractional data is > 0.5. If the fractional data is < 0.5, the number will be rounded down. (11) specifies to use Dynamic Rounding™, where the fractional data is compared to a random number, and the result (1 bit) added to the 8 bits of color data. If the fractional data = 0, no rounding is done. R, G, and B each have their own random number generator. Typically, this mode should be used. Dynamic Rounding™ is used under license from Quantel Limited.
CR15–CR10	reserved (test bits)	These bits should be ignored when the MPU reads this register. Data written to these bits are ignored.

Color Key Registers

The three 8-bit color key registers may be written to or read by the MPU at any time and are initialized to $00 following a reset condition. Data bit A0 is the least significant bit and corresponds to the R0, G0, and B0 output bits.

The red color key register is compared against the R0–R7 outputs, the green color key register is compared against the G0–G7 outputs, and the blue color key register is compared against the B0–B7 outputs. If all unmasked bits match, the COLOR KEY output is a logical one.

Color Mask Registers

The three 8-bit color mask registers may be written to or read by the MPU at any time and are initialized to $00 following a reset condition. Data bit A0 is the least significant bit and corresponds to the R0, G0, and B0 output bits.

A logical zero specifies that the corresponding RGB output bit is to be compared against the corresponding bit in the color key registers. A logical one specifies that no comparison for the corresponding bit is to take place, and is not used in the generation of the COLOR KEY output signal.

Pin Descriptions

Pin Name	Description
D0–D7	Data inputs (TTL compatible). D0–D7 are latched on the rising edge of CLOCK. D0 is the least significant bit.
Cr/Cb0–Cr/Cb7	Cr/Cb data inputs/outputs (TTL compatible). Multiplexed Cr and Cb information is input or output via these pins depending on the value of SWR* and SRD*. CrCb0 is the least significant bit. If inputting Cr/Cb data, it is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. If outputting Cr/Cb data, it is updated following the rising edge of CLOCK while CLOCK/2 is a logical one.
Y0–Y7	Y data inputs/outputs (TTL compatible). Y information is input or output via these pins depending on the value of SWR* and SRD*. Y0 is the least significant bit. If inputting Y data, it is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. If outputting Y data, it is updated following the rising edge of CLOCK while CLOCK/2 is a logical one.
CbFLAG	CbFLAG control output (TTL compatible). A logical one indicates Cb data may be input or output on the Cr/Cb (0–7) bus. It is output following the rising edge of CLOCK while CLOCK/2 is a logical one.
SWR*	Synchronous write control input (TTL compatible). A logical zero enables Y/Cr/Cb data to be input via the Y0–Y7 and Cr/Cb (0–7) pins. Both SRD* and SWR* should not be asserted simultaneously.
SRD*	Synchronous read control input (TTL compatible). A logical zero enables Y/Cr/Cb data to be output onto the Y0–Y7 and Cr/Cb (0–7) pins. Both SRD* and SWR* should not be asserted simultaneously.
A0–A7	Ancillary data outputs (TTL compatible). D0–D7 data is output onto A0–A7 following the rising edge of CLOCK. MPU data is also input and output via this bus. A0 is the least significant bit.
ANC*	Ancillary output (TTL compatible). A logical zero indicates Ancillary data may be present on the A0–A7 pins. ANC* is output following the rising edge of CLOCK.
R0–R7	Red outputs (TTL compatible). Red color information is output via these pins. Data is output following the rising edge of CLOCK. R0 is the least significant bit.
G0–G7	Green outputs (TTL compatible). Green color information is output via these pins. Data is output following the rising edge of CLOCK. G0 is the least significant bit.
B0–B7	Blue outputs (TTL compatible). Blue color information is output via these pins. Data is output following the rising edge of CLOCK. B0 is the least significant bit.
H, V, F	Video timing control outputs (TTL compatible). They are output following the rising edge of CLOCK.
RESET*	Reset control input (TTL compatible). RESET* is sampled on the rising edge of CLOCK, and must be a logical zero for a minimum of three consecutive CLOCK cycles to reset the device. RESET* must be a logical one for normal operation.
ERROR	Error indicator output (TTL compatible). This output indicates a parity error in the EAV, SAV, Ancillary data identification code, Ancillary data word count, or Ancillary data. If an error is detected, ERROR will be a logical one for five CLOCK cycles, three CLOCK cycles after the error has occurred.

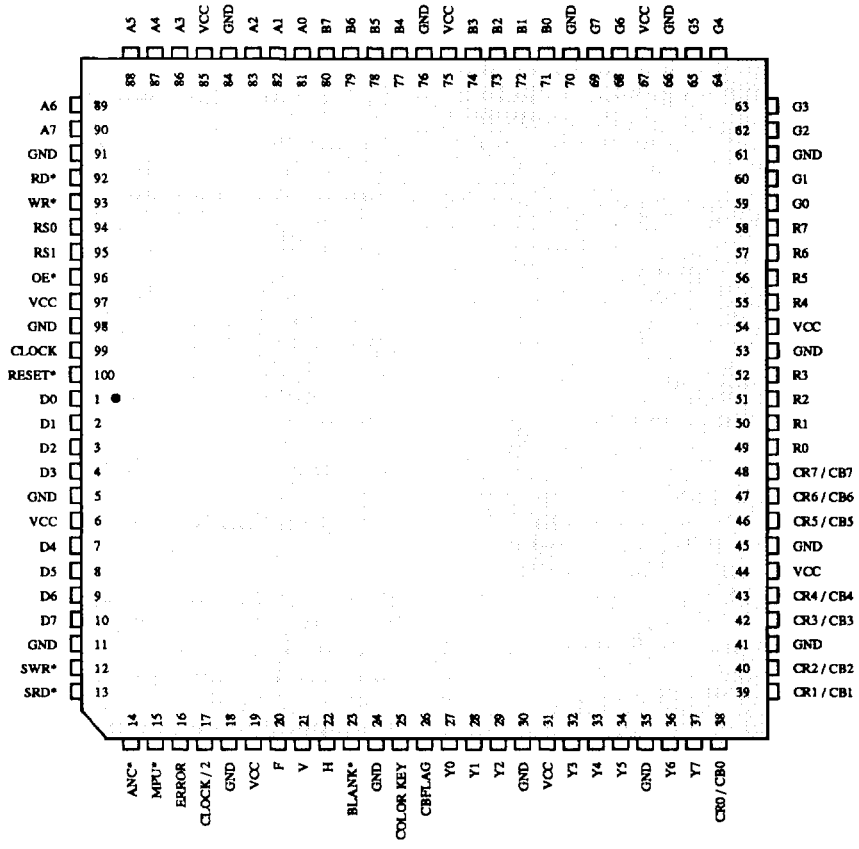
Pin Descriptions (continued)

Pin Name	Description
OE*	Output enable control input (TTL compatible). This input is logically gated with command bit CR01, and the result controls three-stating the RGB outputs as follows:

CR01	OE*	RGB Outputs
0	0	enabled
0	1	three-stated
1	0	three-stated
1	1	three-stated

CLOCK	27 MHz clock input (TTL compatible). The clock must be present for the MPU to access the internal control registers.
CLOCK/2	13.5 MHz clock output (TTL compatible). The clock output is 1/2 the CLOCK rate.
RD*	MPU read control input (TTL compatible). While a logical zero, the contents of the control register/RAM location are output onto A0–A7. If both RD* and WR* are asserted simultaneously, all signal pins are three-stated (note the device should be reset after three-stating the signal pins).
WR*	MPU write control input (TTL compatible). The rising edge of WR* latches A0–A7 into the control register/RAM location. WR* is internally resynchronized to CLOCK, so CLOCK must be a continuous clock. If both RD* and WR* are asserted simultaneously, all signal pins are three-stated (note the device should be reset after three-stating the signal pins).
RS0, RS1	Register select control inputs (TTL compatible). These bits specify whether the MPU is accessing the address register or the control register/RAM location specified by the address register. See Table 3.
MPU*	MPU access control output (TTL compatible). A logical zero indicates the MPU may access the internal registers without contention with Ancillary data. MPU* is output following the rising edge of CLOCK.
BLANK*	Composite blanking output (TTL compatible). BLANK* is the logical NOR of the H and V outputs, and has the same timing.
COLOR KEY	Color key output (TTL compatible). This output is a logical one for clock cycles where the RGB outputs contain color information specified by the color key and color mask registers. It is output following the rising edge of CLOCK.
VCC	Power pins. All VCC pins must be connected together.
GND	Ground pins. All GND pins must be connected together.

Pin Descriptions (continued)



Application Information

Cr and Cb Interpolation Filters

The Cr/Cb linear phase interpolation filters interpolate the missing Cr and Cb data to generate 4:4:4 YCrCb data. Input color data samples are passed unchanged to the output; computed color data (from the filters) are inserted into the output flow.

If the CR07 command bit is a logical one, then if the interpolated result is zero, it is made 1; if the interpolated result is 255, it is made 254. If the CR07 command bit is a logical zero, then if the interpolated result is 0–15, it is made 16; if the interpolated result is 241–255, it is made 240.

The transfer function of the 12-tap filters is:

$$H(Z) = (160/256)*(Z^{-1} + Z^{+1}) + (-48/256)*(Z^{-3} + Z^{+3}) + (24/256)*(Z^{-5} + Z^{+5}) + (-12/256)*(Z^{-7} + Z^{+7}) + (6/256)*(Z^{-9} + Z^{+9}) + (-2/256)*(Z^{-11} + Z^{+11})$$

Seventeen-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1. Figure 7 shows the transfer function of the 12-tap Cr and Cb interpolation filters.

The transfer function of the 2-tap filters is:

$$H(Z) = (128/256)*(Z^{-1} + Z^{+1})$$

Eleven-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1.

The Y data and control signals are pipelined to maintain synchronization with the Cr and Cb data. There is no change in the pipeline delay regardless of which filter is used.

During blanking periods, the input color data is undefined, possibly disturbing the computed color data at the beginning and end of active color data. To avoid this, if the 12-tap is filter-selected, the 2-tap filter is automatically used at the beginning and end of the active line unless the 12-tap filter is available (i.e., the filter pipe is full). Regardless of the filter selection, the last active pixel per scan line uses the previous Cr and Cb data for color information.

Doubling the RGB Data Rate

The data rate of RGB output data may be doubled from 13.5 MHz to 27 MHz via the command register. In this instance, new RGB data is output following the rising edge of every CLOCK cycle, rather than every other CLOCK cycle.

To accomplish this, an additional set of 2-tap linear interpolation filters are used to double the RGB data rate from 13.5 MHz to 27 MHz. Input color data samples are passed unchanged to the output; computed color data (from the filters) are inserted into the output flow.

The transfer function of the 2-tap filters is:

$$H(Z) = (128/256)*(Z^{-1} + Z^{+1})$$

Eleven-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits using Dynamic Rounding™ (used under license from Quantel Limited).

Outputting RGB data at the 27 MHz rate may simplify the analog filtering if the RGB outputs are driving external D/A converters. Note that any sin x / x correction must be done with the analog filters after the D/A converters.

SAV and EAV Error Correction

Table 2 gives corrected values for F, V, and H where possible. Multiple (uncorrectable) errors are denoted by an asterisk. D1–D3 are Hamming (6:3) protection bits, and D0 is an even parity bit for D1–D6.

In the event of an uncorrectable error, the H, V, and F outputs assume the state specified by the EAV or SAV sequence (as if an error did not occur).

Application Information (continued)

Random Number Generators

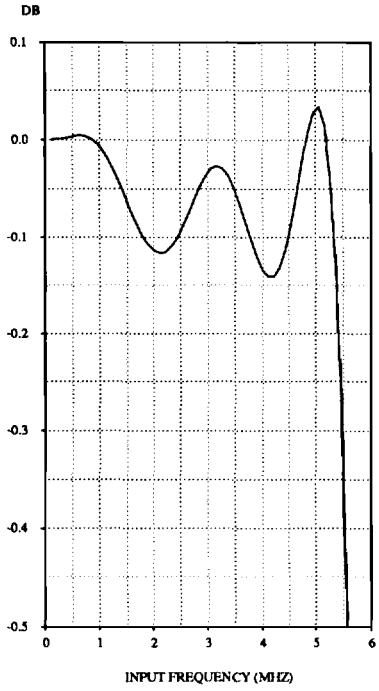
The Bt294 contains two random number generators, as shown in Figures 8 and 9, used when Dynamic Rounding™ (used under license from Quantel Limited) is selected.

Figure 8 shows the random number generator used for the YCrCb to RGB matrix and the RGB data rate doubling (it is initialized to $000 following a reset condition). As each RGB value in the matrix has 4 fractional data bits, 4 bits of random numbering is generated for each RGB value. The LSB of each 4-bit random number (D0, D4, D8) corresponds to the LSB of fractional RGB data.

The RGB rate doubling filters have 1 bit of fractional data. Random number bit D12 corresponds to red fractional data, bit D13 corresponds to green, and bit D14 corresponds to blue.

Figure 9 shows the random number generator for the Cr and Cb filters (it is initialized to $00 following a reset condition). As a single CrCb filter is used in a multiplexed fashion, a single CrCb random number generator is used. The 12-tap filter has 7 bits of fractional data. The LSB of the 7-bit random number (D0) corresponds to the LSB of fractional Cr and Cb data. The LSB of this random number generator (D0) is used for the 2-tap filters, which have 1 bit of fractional data.

3



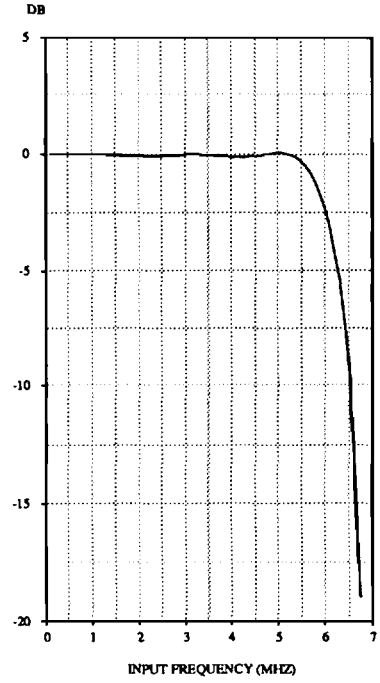


Figure 7. CrCb Pass-Band and Stop-Band Interpolation Filter Characteristics.

Application Information (continued)

Typical Applications

Figure 10 shows the Bt291 and Bt294 being used with a 24-bit RGB frame buffer. The Bt291 and Bt294 provide another video I/O port to the imaging/graphics system.

Figure 11 shows the Bt291 and Bt294 being used with a 16-bit YCrCb frame buffer. The Bt291 and Bt294 provide another video I/O port to the imaging/graphics system.

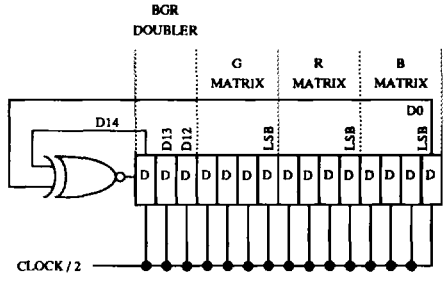


Figure 8. Random Number Generator.

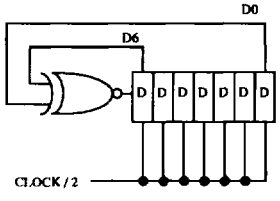


Figure 9. Random Number Generator for Cr and Cb Filters.

Application Information (continued)

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by assuring that all VCC pins are at the same potential, and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

PLCC Sockets

100-pin PLCC sockets for the Bt294 are available from:

McKenzie Technology
44370 Old Warm Springs Blvd.
Fremont, CA 94538
Phone: (415) 651-2700
FAX: (415) 651-1020
TLX: 910-240-6355
Part Number: PLCC-100-P-T

or

Yamaichi Electric Mfg. Co., LTD.
3-28-7 Nakamagome, Ohta-ku,
Tokyo 143 Japan
Phone: 03-778-6161
FAX: 03-778-6181
US Representative: (408) 452-0797

	Received F, V, H (Bits D6–D4)							
D3 - D0	000	001	010	011	100	101	110	111
0000	000	000	000	*	000	*	*	111
0001	000	*	*	111	*	111	111	111
0010	000	*	*	011	*	101	*	*
0011	*	*	010	*	100	*	*	111
0100	000	*	*	011	*	*	110	*
0101	*	001	*	*	100	*	*	111
0110	*	011	011	011	100	*	*	011
0111	100	*	*	011	100	100	100	*
1000	000	*	*	*	*	101	110	*
1001	*	001	010	*	*	*	*	111
1010	*	101	010	*	101	101	*	101
1011	010	*	010	010	*	101	010	*
1100	*	001	110	*	110	*	110	110
1101	001	001	*	001	*	001	110	*
1110	*	*	*	011	*	101	110	*
1111	*	001	010	*	100	*	*	*

Table 2. SAV and EAV Error Correction Table.

Application Information (continued)

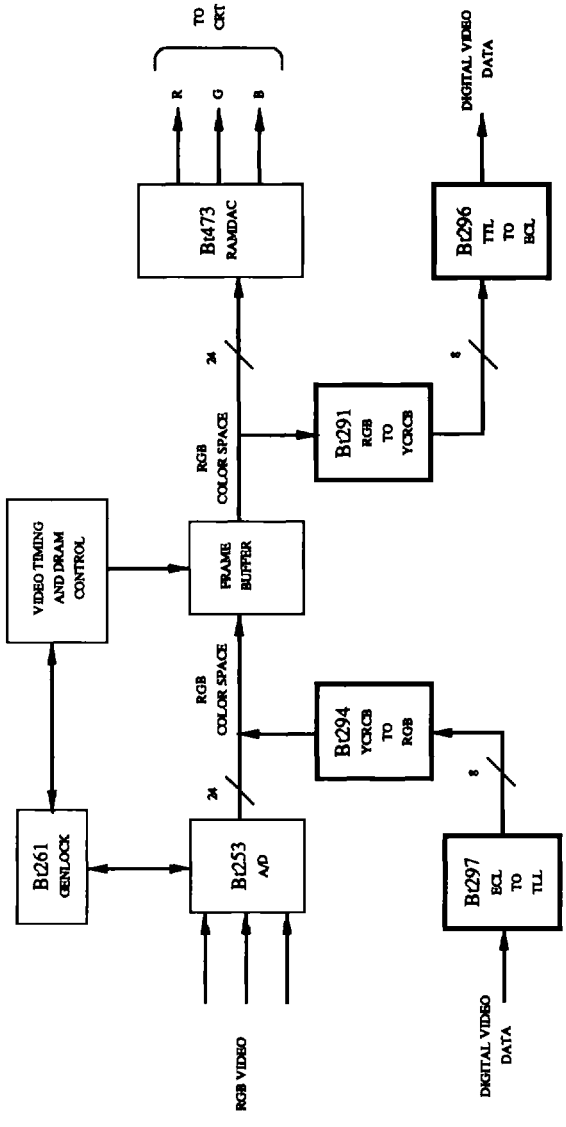


Figure 10. Typical Application.

Application Information (continued)

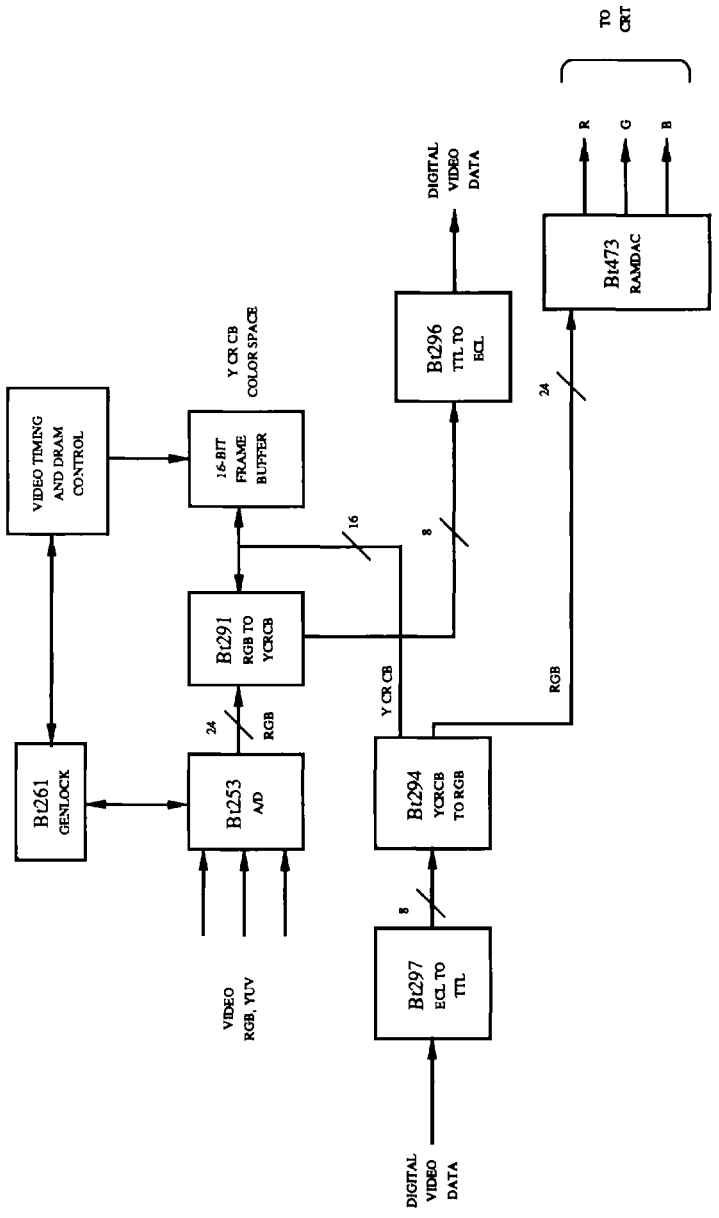


Figure 11. Typical Application.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on any Signal Pin*		GND–0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current (if applicable)	IOZ			50	µA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

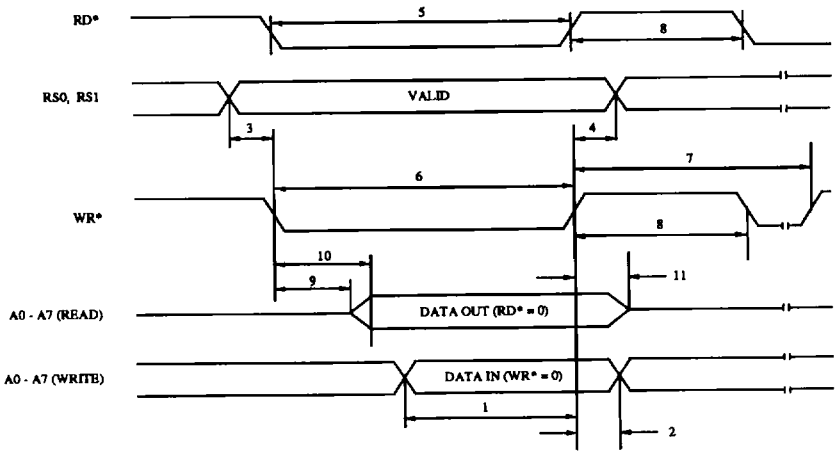
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			27	MHz
MPU Data Setup Time	1	10			ns
MPU Data Hold Time	2	10			ns
RS0, RS1 Setup Time	3	10			ns
RS0, RS1 Hold Time	4	10			ns
RD* Low Time	5	1			Clock
WR* Low Time	6	100			ns
WR* Cycle Time	7	3			Clocks
RD*, WR* High Time	8	30			ns
RD* Asserted to Data Bus Driven	9	5			ns
RD* Asserted to Data Valid	10			100	ns
RD* Negated to Data Bus 3-Stated	11			25	ns
CLOCK/2 Low Time	12	15		tbd	ns
CLOCK/2 High Time	13	15		tbd	ns
CLOCK/2, H, V, F, Y/Cr/Cb (0–7), RGB (0–7), CbFLAG, BLANK* Output Delay	14	5		23	ns
Y/Cr/Cb Input Data, SRD*, SWR*					
Setup Time	15	10			ns
Hold Time	16	4			ns
D0–D7 Input Data					
Setup Time	17	10			ns
Hold Time	18	4			ns
MPU*, ANC*, ERROR, COLOR KEY Output Delay	19	5		23	ns
A0–A7 Output Delay	20	5		23	ns
SRD* Asserted to YCrCb Bus Driven				25	ns
SRD* Negated to YCrCb Bus 3-Stated				25	ns
RGB Three-State Disable Time	21			25	ns
RGB Three-State Enable Time	22			25	ns
Clock Cycle Time	23	37.04			ns
Clock Pulse Width High	24	15			ns
Clock Pulse Width Low	25	15			ns
VCC Supply Current*	ICC		180	tbd	mA

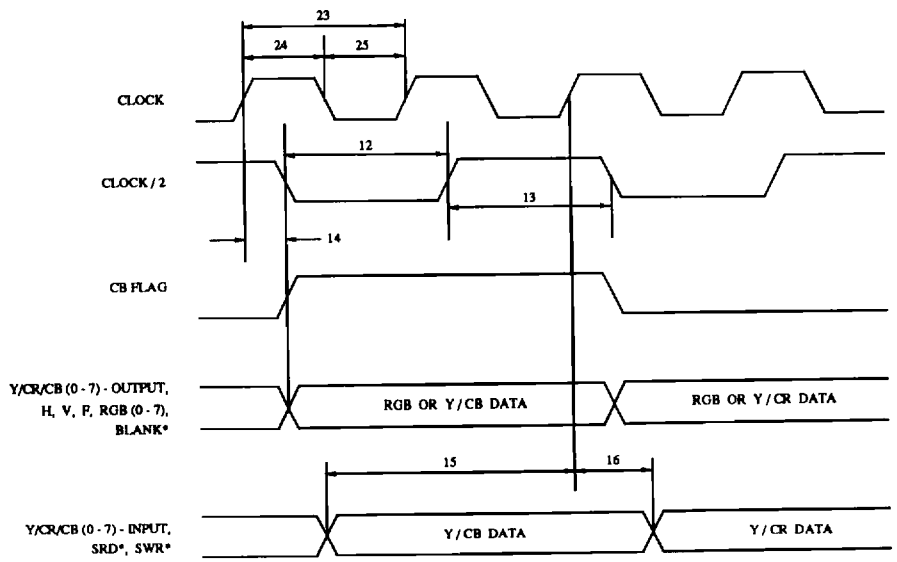
Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. CbFLAG, CLOCK/2, ANC*, Yx, Crx/Cbx, A0–A7, R0–R7, G0–G7, B0–B7, MPU*, COLOR KEY, and ERROR output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC (max).

Timing Waveforms

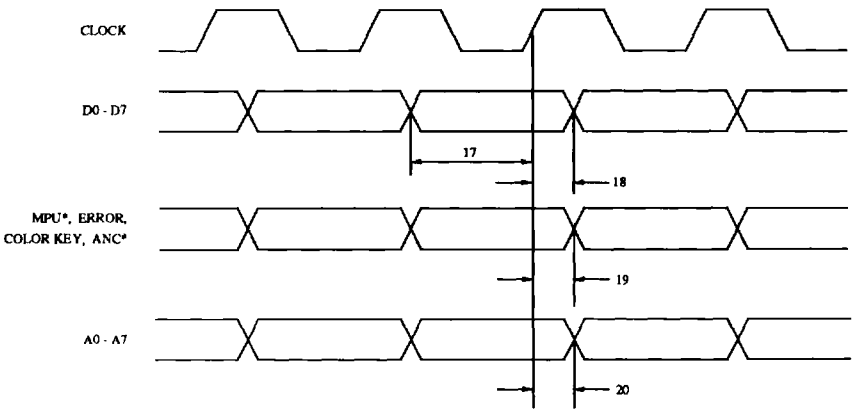


MPU Read/Write Timing.

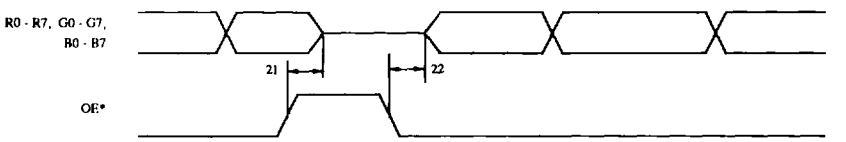


RGB, YCrCb Timing.

Timing Waveforms (continued)



A0–A7, D0–D7 Timing.



Output Enable Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt294KPJ	100-pin Plastic J-Lead	0° to +70° C