⊗YAMAHA

YTD436

ISTC

ISDN BRI controller with S/T ref. pt. analog D/R

YTD436 is a high-performance communication LSI for the ISDN BRI user-network interface function (digital four-wire time-division full-duplex operation), supporting D channel layer 1 and layer 2 functions in one 100-pin SQFP chip.

YTD436 supports layer 1 (physical layer) control function conforming to ITU-T Recommendation I.430 and fully supports layer 2 (LAPD protocol) function conforming to ITU-T Recommendations Q.920 and Q.921. ETSI (European Telecommunication Standards Institute) and North American standard operating modes are also supported.

In addition, YTD436 includes layer 3 processor interface function which operate in DMA transfer mode or I/O transfer mode. This gives a great advantage for mounting and functional designing of both "active" (CPU on board) terminal equipment and "passive" (no CPU on board) PC cards.

The layer 1 function has a built-in S/T reference point analog driver/receiver to support the S/T reference point interface. In order to support the U interface, YTD436 also has a I.430 TTL interface (no built-in analog driver/receiver) suitable for connecting to an NT1 chip or a DSU module.

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Features

1. Layer 1 function

• Conforms to ITU-T Recommendation I.430 (1992 edition) and
TTC Standard JT-I430 (1997 edition) (default)

- 192 kbps transmission rate
- Interface structure : 2B + D (B = 64 kbps, D = 16 kbps)
- Frame assembling and disassembling function
- Collision control (built-in random number (Ri) reset),
priority control (built-in retransmission control), and state transition control
- Programmable T3 and T4 timers

• Supports ETSI ETS 300 012 (April 1992) and ANSI T1.605 operating modes

• Leased line capability (JT-I430-a)

• Built-in driver and receiver

- I.430 TTL interface (when the driver / receiver is disconnected)
- No external relay or common-mode choke needed
- Supports 1-to-2 pulse transformer

• Abundant Test functions (for testing and maintenance)

- Demo mode in which no switch simulator is needed.
- Three kinds of loop-back modes (Loop-back 1 to 3)
- INFO signals output for testing
- Test pulse output for pulse shape check

• Multiframing capability

• INFO1 transmission and INFO4 reception monitor pins

• Power down monitor pin

• I.430 transmission frame phase adjustment function

2. Layer 2 function

• Conforms to ITU-T Recommendation Q.920 (1992 edition) and Q.921 (1997 edition)
and TTC Standard JT-Q920 (1993 edition) and JT-Q921 (1998 edition)

- HDLC frame control (Flag control, FCS generation/checking,
Automatic zero insertion/deletion, Abort pattern transmission/detection, etc.)
- LAPD status control (Sequence control, Flow control, SAPI control)
- Built-in timer for time-out check

• Supports ETSI ETS 300 125 (September 1991), National ISDN-1/2,
AT&T 5ESS 5E9 and Nortel DMS-100 S208-6 operating modes

• Multilink capability
(circuit switching × 2 links, packet switching/teleaction communications × 2 links)

• Automatic assigned TEI/non-automatic assigned TEI (VC/PVC)

• Leased line mode (disable layer 2 function)

3. Layer 3 interface function

- Connects to 8-bit or 16-bit microprocessor

  (8086 family, 80186 family, 6800 family, 68000 family)
- Operates in one of two data transfer modes :
    - DMA transfer mode (with the built-in 16-bit address DMA controller)
    - I/O transfer mode (with the built-in FIFO)
- Primitive logical interface

4. B channel interface

- Data rate setting : 64 k, 56 k and 32 kbps
- Serial mode
    - B channel I/O clock selection function
        - Internal clock mode

          Inputs/outputs the B channel data with 64 k, 56 k or 32 kHz internal clock
        - External clock mode (PCM Highway mode)

          Inputs/outputs the B channel data with a 128 k to 2048 kHz external clock
    - B channel selection function
        - Internal clock mode

          Selects/switches B channel I/O pins
        - External clock mode (PCM Highway mode)

          Selects/switches B channel time slots
- Parallel mode
    - LSB/MSB switching function
    - Bit shift function
    - Data transfer mode
        - DMA transfer mode with the DMA request function
        - I/O transfer mode with the built-in FIFO

5. Low-power operation

   (Host processor clock control function, Powerdown mode)

6. High-performance CMOS technology

7. 100-pin SQFP

8. DigitalSupply Voltage (+5V or +3.3V), Analog +5V supply

Applications

- **ISDN telephone**
- **Video telephone**
- **Telemeter**
- **PBX**
- **Terminal adapter (TA)**
- **Other ISDN terminals**

Functional Comparison of YAMAHA ISDN S/T Interface LSIs

FUNCTION			YTD410	YM7405B	YTD418	YTD423	YTD436
Layer 1	ITU-T Recommendation I.430		1992 edition	1992 edition	1992 edition	1992 edition	1992 edition
	TTC Standard	JT-I430	1993 edition	1993 edition	1993 edition	1993 edition	1997 edition
Layer 2 (LAPD)	ITU-T Recommendation	Q.920 Q.921	1992 edition	1992 edition	1992 edition	1992 edition	1992 edition 1997 edition
	TTC Standard	JT-Q920 JT-Q921	1993 edition	1993 edition	1993 edition	1993 edition	1993 edition 1998 edition
ETSI ETS 300 012, ETS 300 125				√	√	√	√
North American Switches National ISDN-1/2, AT&T 5ESS, Nortel DMS-100						√	√
S/T Reference Point Analog Driver/Receiver			Internal	Internal	External [YTD421B]	External [YTD421B]	Internal
Maximum D Channel Links	Circuit Switching		1	2	2	2	2
	Dch Packet Switching (Teleaction Communication)		1	2	2	2	2 (2)
D Channel Layer 3 Data Transfer Method			DMA Transfer	DMA Transfer	DMA Transfer	DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer
HDLC Controller and DMA Controller for B Channel Data			External	External	External	Internal	Internal
B Channel Data Transfer Method			–	–	–	DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer **(Note 1)**
B Channel Internal Clock Mode (kHz)			56, 64	64	64	32, 56, 64	32, 56, 64
B Channel External Clock Mode				√	√	√	√
Clock Output Function for MPU			√			√	√
Signal Output Function for Testing			√			√	√
Supply Voltage (V)			+5	+5	+5	+5	+5 or +3.3 **(Note 2)**
Power Consumption during Operation [typ.] (mW)			65	125	75	85	75 (@+5V) 40 (@+3.3V)
Power Consumption during Sleep [typ.] (mW)			2	30	21	1	less than 0.5 **(Note 3)**
Package			80 pin QFP 100 pin TQFP	80 pin QFP 100 pin TQFP	80 Pin QFP	100 pin SQFP	100 pin SQFP

Note 1: DMA Transfer: Request function only
I/O transfer: 4 byte FIFO
Note 2: With respect to Digital Supply Voltage
Note 3: State at Line interface disconnection + Power down (SLEEP state)

BLOCK DIAGRAM

User Network Interface Block Diagram

YTD436 is the most-suited LSI for terminal equipment such as ISDN telephones and video telephones and for PHS base stations.

YTD436 contains layer 1 and layer 2 functions, analog driver/receiver for the S/T reference point, DMA request function for B channel data transfer, and DMA controller for D channel data transfer. Because of this, terminal equipment can be optimally configured by adding few circuits such as the layer 3 control processor.
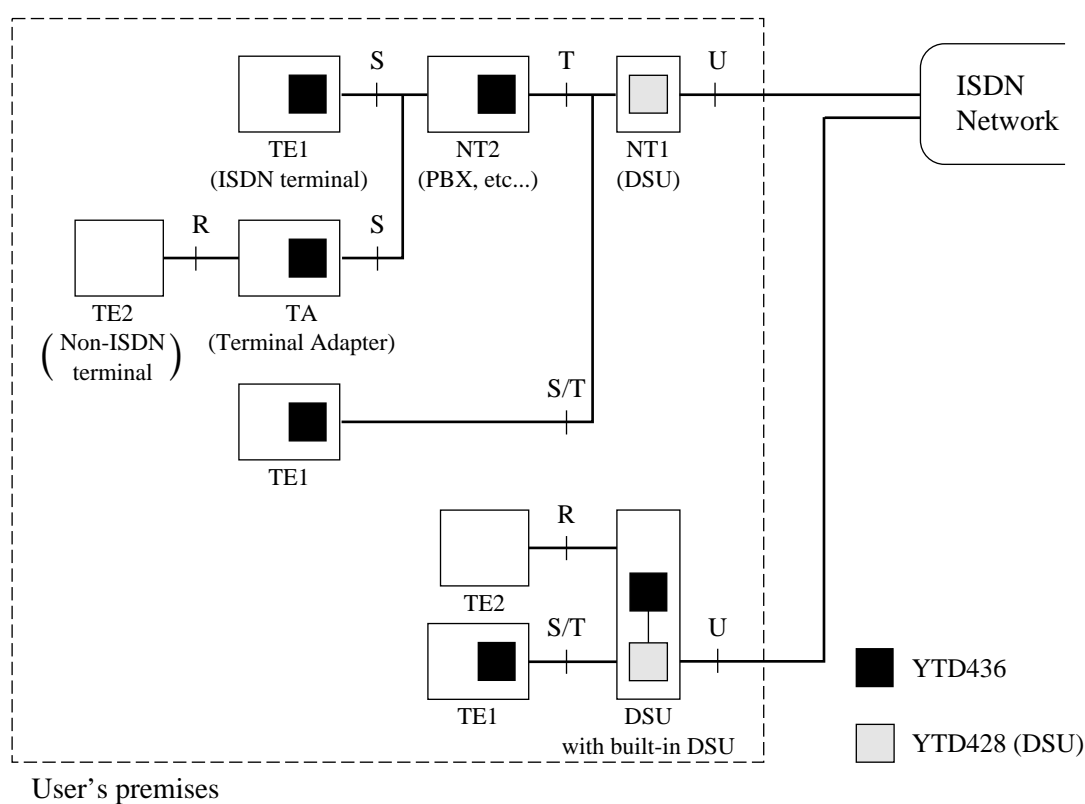
YTD436 Peripheral LSI Interface Block Diagram
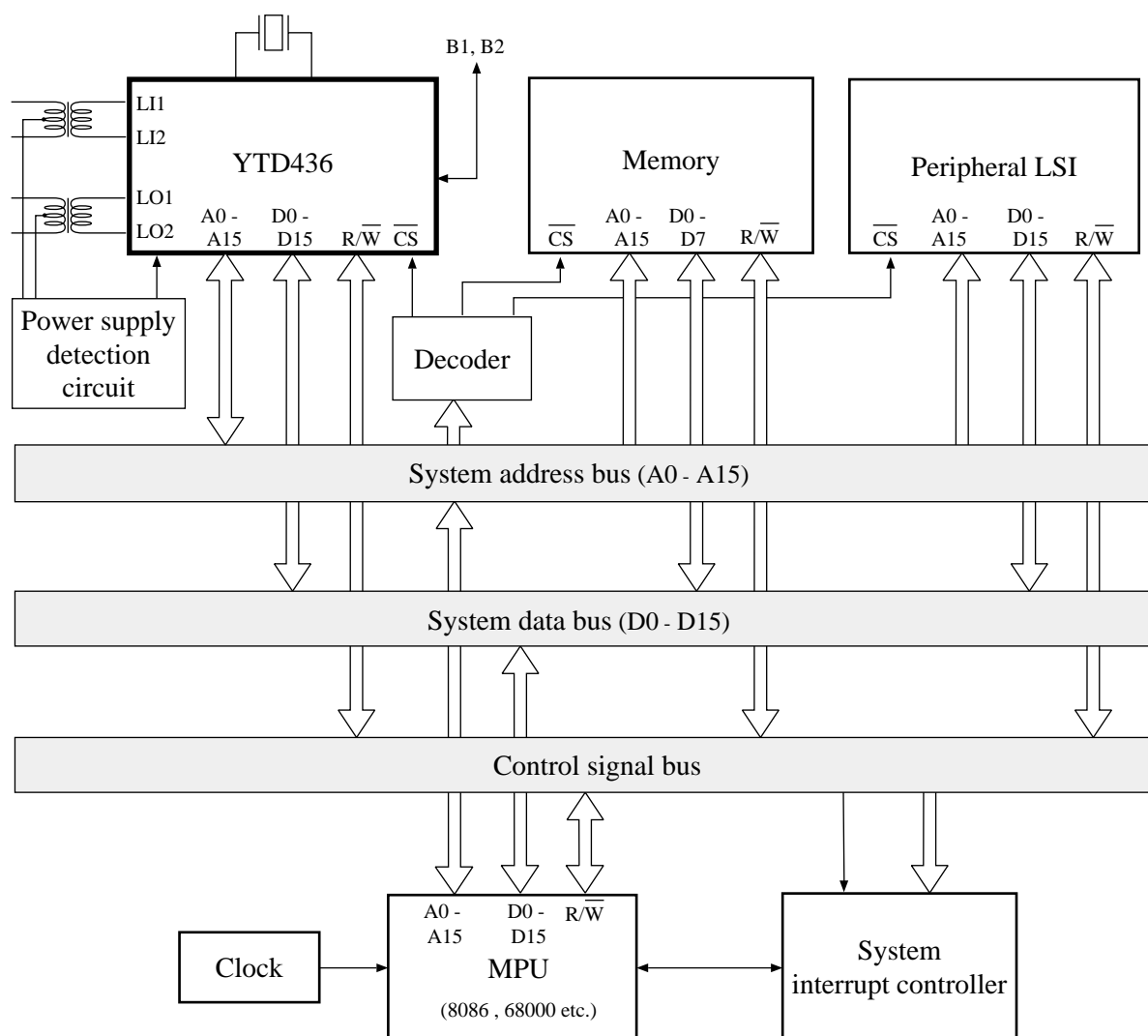
YTD436 Internal Block Diagram

Pin Assignments

Top pins (left to right, 50 to 26):
LI2, CX1, AVss, LO1, AVDD, LO2, RX, 80/$\overline{68}$, 16/$\overline{8}$, $\overline{TEST1}$, VDSEL, CLKSEL, $\overline{WAKEUP}$, RBHW / RB1, DVss, TBHW / RB2, RSYNC / TB1, TSYNC / TB2, EXTCLK / CL64K, CL128K / CL32K, CL56K, CL8K, CL4K, AEN, A15

Left pins (top to bottom, 51 to 75):

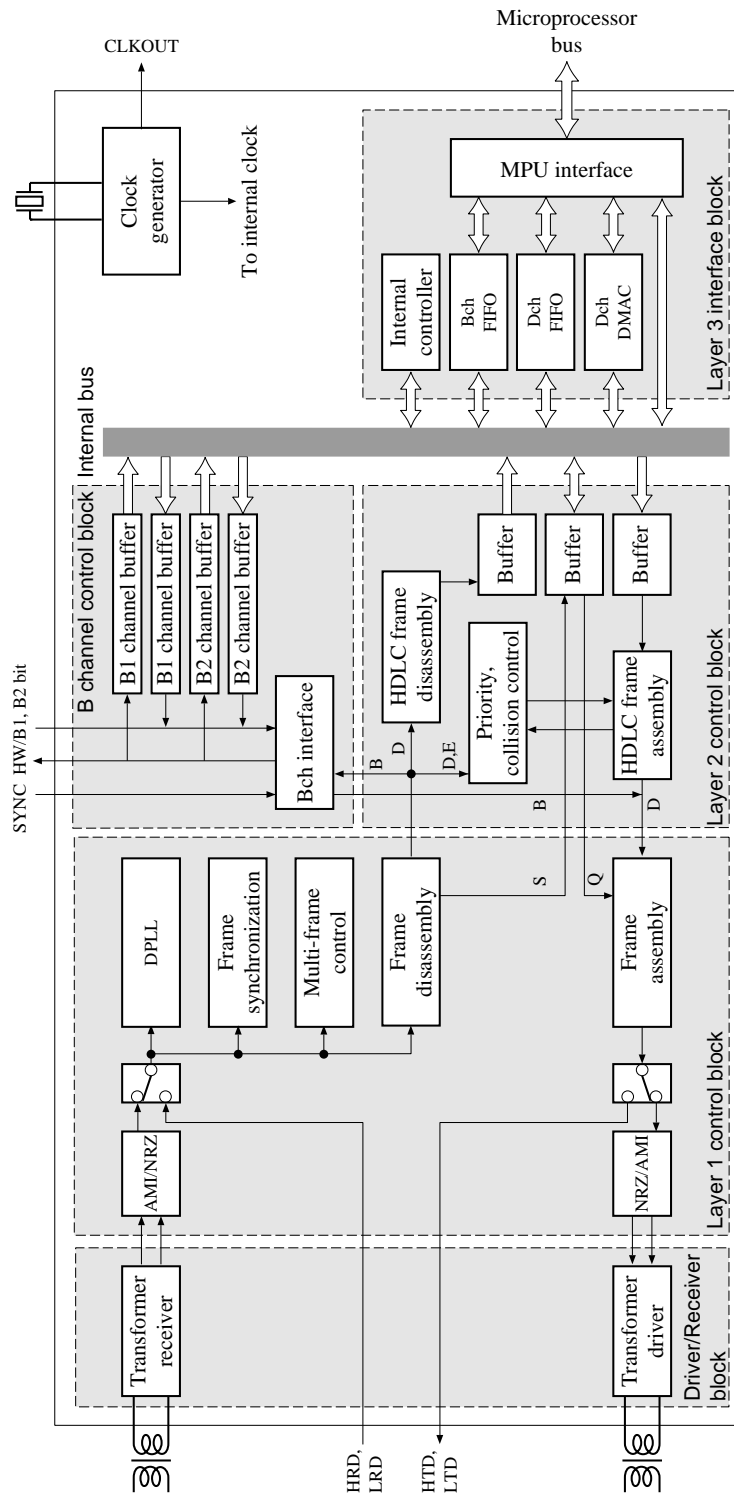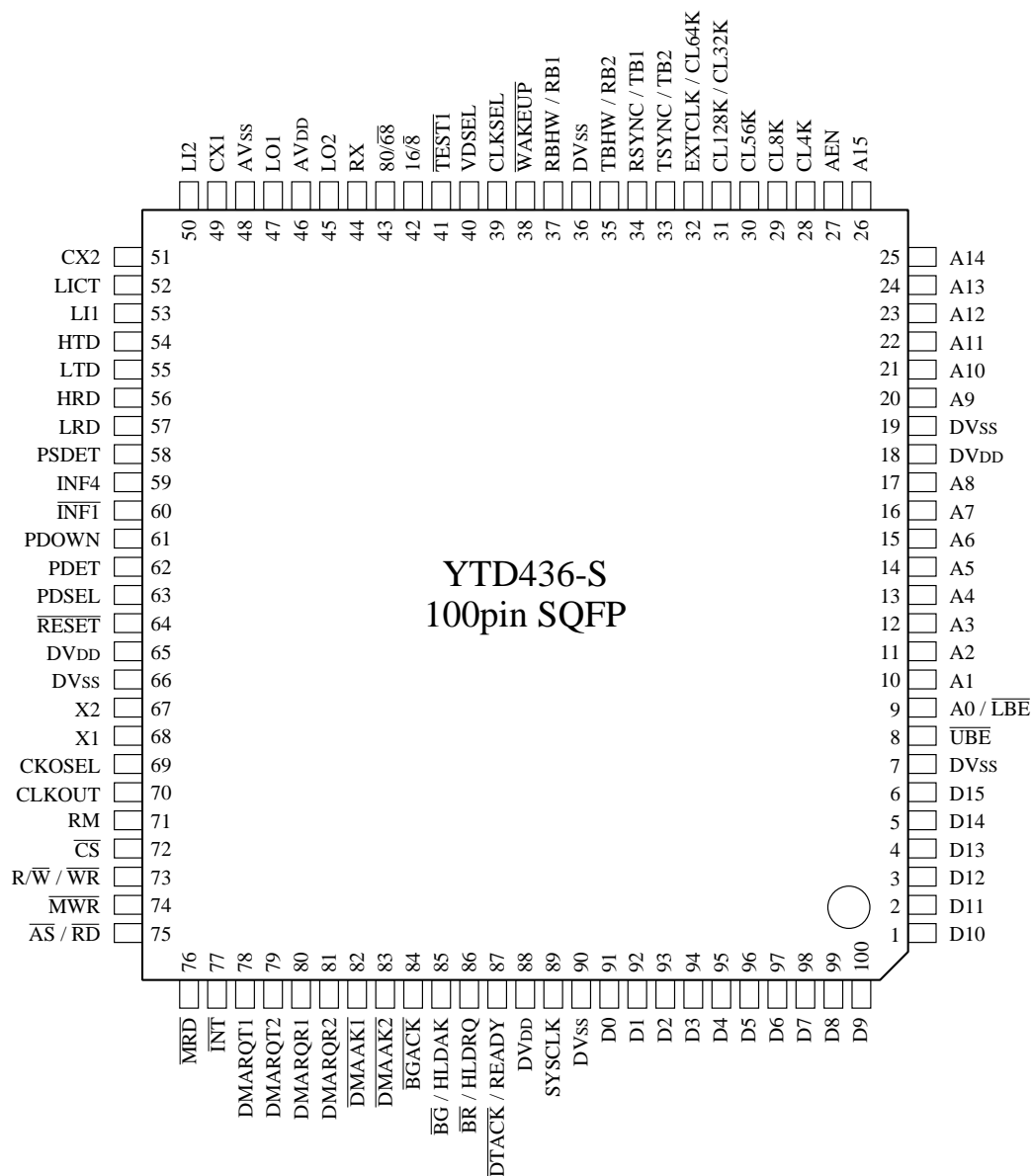| Pin	Signal
51	CX2
52	LICT
53	LI1
54	HTD
55	LTD
56	HRD
57	LRD
58	PSDET
59	INF4
60	$\overline{INF1}$
61	PDOWN
62	PDET
63	PDSEL
64	$\overline{RESET}$
65	DVDD
66	DVss
67	X2
68	X1
69	CKOSEL
70	CLKOUT
71	RM
72	$\overline{CS}$
73	R/$\overline{W}$ / $\overline{WR}$
74	$\overline{MWR}$
75	$\overline{AS}$ / $\overline{RD}$

Right pins (top to bottom, 25 to 1):

Pin	Signal
25	A14
24	A13
23	A12
22	A11
21	A10
20	A9
19	DVss
18	DVDD
17	A8
16	A7
15	A6
14	A5
13	A4
12	A3
11	A2
10	A1
9	A0 / $\overline{LBE}$
8	$\overline{UBE}$
7	DVss
6	D15
5	D14
4	D13
3	D12
2	D11
1	D10

Center label: YTD436-S 100pin SQFP

Bottom pins (left to right, 76 to 100):
$\overline{MRD}$, $\overline{INT}$, DMARQT1, DMARQT2, DMARQR1, DMARQR2, $\overline{DMAAK1}$, $\overline{DMAAK2}$, $\overline{BGACK}$, $\overline{BG}$ / HLDAK, $\overline{BR}$ / HLDRQ, $\overline{DTACK}$ / READY, DVDD, SYSCLK, DVss, D0, D1, D2, D3, D4, D5, D6, D7, D8, D9

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	- 0.3	+ 7.0	V
Input Voltage	DV_I	- 0.3	$DV_{DD} + 0.3$	V
	AV_I	- 0.3	$AV_{DD} + 0.3$	V
Storage Temperature	T_{stg}	- 50	+ 125	℃

(Based on $DV_{SS} = AV_{SS} = 0.0$ V)

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	DV_{DD}	VDSEL="H"	4.75	5.25	V
		VDSEL="L"	3.0	3.6	V
	AV_{DD}		4.75	5.25	V
Operating Temperature	T_{op}		- 30	85	℃

(Based on $DV_{SS} = AV_{SS} = 0.0$ V)

DC Characteristics

When DVDD = 5 V $\pm$ 5 %, AVDD = 5 V $\pm$ 5 % (VDSEL="H", Top = - 30 to + 85 ºC)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage	(CMOS)	V_{DIH}	(**Note 1**)	$0.8DV_{DD}$			V
Low-Level Input Voltage	(CMOS)	V_{DIL}	(**Note 1**)			$0.2DV_{DD}$	V
High-Level Input Voltage	(TTL)	V_{DIH}	(**Note 2**)	2.2			V
Low-Level Input Voltage	(TTL)	V_{DIL}	(**Note 2**)			0.8	V
High-Level Output Voltage	(CMOS)	V_{DOH}	$|I_{DOH}| < 10\ \mu A$	DV_{DD} - 0.4			V
Low-Level Output Voltage	(CMOS)	V_{DOL}	$|I_{DOL}| < 10\ \mu A$			DV_{SS} + 0.4	V
High-Level Output Voltage	(TTL)	V_{DOH}	(**Note 3**)	2.7			V
Low-Level Output Voltage	(TTL)	V_{DOL}	(**Note 3**)			0.4	V
Low-Level Output Voltage	(Open-D)	V_{DOL}	(**Note 4**)			0.4	V
Leakage Current		I_L		-10		10	μA
Off-State Leakage Current		I_{LZ}	(**Note 5**)	-10		10	μA
Power Supply Current (Digital block)		DI_{DD}	(**Note 6**)		10.2		mA
			(**Note 7, 9**)		0.1		mA
Power Supply Current (Analog block)		AI_{DD}	(**Note 6, 10**)		4.8		mA
			(**Note 7, 10**)		0.4		mA
			(**Note 8, 10**)		0.1		mA

Note 1: With respect to X1, PSDET, PDET, PDSEL, $\overline{WAKEUP}$, $\overline{RESET}$, CLKSEL, $\overline{TEST1}$, VDSEL pins (except for the analog pins).

Note 2: With respect to other pins (except for the analog pins).

Note 3: CLKOUT pin   Test condition: I_{DOH} = - 1.0 mA, I_{DOL} = 2.0 mA

other output pins   Test condition: I_{DOH} = - 0.4 mA, I_{DOL} = 1.2 mA

Note 4: HTD, LTD, $\overline{INT}$ pin   Test condition : I_{DOL} = 1.2 mA

$\overline{INF1}$ pin   Test condition : I_{DOL} = 3 mA

RBHW pin   Test condition : R_L = 500 Ω

Note 5: With respect to cases in which D0 - D15, and A0 - A15 pins are in the input state and $\overline{MWR}$ and $\overline{MRD}$ pins are in Hi-Z state.

Note 6: RUN state (connecting with a B channel, transferring all "0", SYSCLK = 8 MHz, using internal driver/receiver, assuming as V_{DIH} = DV_{DD}, V_{DIL} = DV_{SS})

Note 7: SLEEP state

Note 8: SLEEP state + Line interface disconnection

Note 9: When SYSCLK is stopped.

Note 10: When using internal driver/receiver

When DVDD = 3.3 V $\pm$ 0.3 V, AVDD = 5 V $\pm$ 5 % (VDSEL="L", Top = - 30 to + 85 ºC)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage	V_{DIH}		$0.8DV_{DD}$			V
Low-Level Input Voltage	V_{DIL}				$0.2DV_{DD}$	V
High-Level Output Voltage	V_{DOH}	$|I_{DOH}| < 0.4$ mA	$DV_{DD} - 0.4$			V
Low-Level Output Voltage	V_{DOL}	$|I_{DOL}| < 1.2$ mA			$DV_{SS} + 0.4$	V
Low-Level Output Voltage　　(Open-D)	V_{DOL}	(**Note 1**)			0.4	V
Leakage Current	I_L		-10		10	µA
Off-State Leakage Current	I_{LZ}	(**Note 2**)	-10		10	µA
Power Supply Current (Digital block)	DI_{DD}	(**Note 3**)		4.9		mA
		(**Note 4**, **6**)		0.1		mA
Power Supply Current (Analog block)	AI_{DD}	(**Note 3**, **7**)		4.8		mA
		(**Note 4**, **7**)		0.4		mA
		(**Note 5**, **7**)		0.1		mA

Note 1: HTD, LTD, $\overline{INT}$, $\overline{INF1}$ pin Test condition : I_{DOL} = 1.2 mA

　　　　　　RBHW pin　　　　　　　　　Test condition : R_L = 500 Ω

Note 2: With respect to cases in which D0 - D15, and A0 - A15 pins are in the input state and $\overline{MWR}$ and $\overline{MRD}$ pins are in Hi-Z state.

Note 3: RUN state (connecting with a B channel, transferring all "0", SYSCLK = 8 MHz, using internal driver/receiver, assuming as V_{DIH} = DV_{DD}, V_{DIL} = DV_{SS})
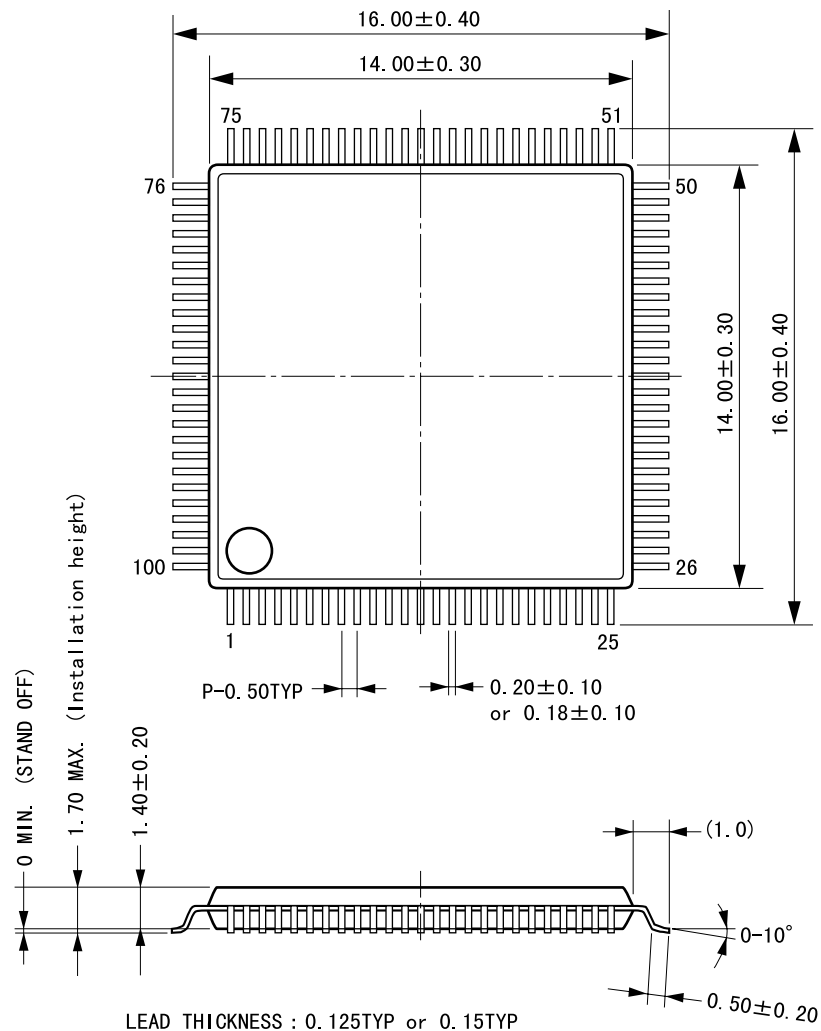
Note 4: SLEEP state

Note 5: SLEEP state + Line interface disconnection

Note 6: When SYSCLK is stopped.

Note 7: When using internal driver/receiver

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PACKAGE OUTLINE

C-PK100SP-1

16.00±0.40

14.00±0.30

75   51

76   50

14.00±0.30

16.00±0.40

100   26

1   25

P-0.50TYP   0.20±0.10
or 0.18±0.10

0 MIN. (STAND OFF)

1.70 MAX. (Installation height)

1.40±0.20

(1.0)

0-10°

0.50±0.20

LEAD THICKNESS : 0.125TYP or 0.15TYP

(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape
in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

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