

CCD linear image sensors

S11155-2048 S11156-2048

Back-thinned CCD image sensors with electronic shutter function

The S11155-2048 and S11156-2048 are back-thinned CCD linear image sensors with an internal electronic shutter for spectrometers. These image sensors use a resistive gate structure that allows high-speed transfer. Each pixel has a lengthwise size needed by spectrometers but ensures readout with low image lag.

Features

- ➔ Built-in electronic shutter
- ➔ Minimum integration time: 30 μ s
- ➔ High sensitivity from the ultraviolet region (spectral response range: 200 to 1100 nm)
- ➔ Readout speed: 10 MHz max.
- ➔ Image lag: 0.1% typ.

Applications

- ➔ Spectrometers
- ➔ Image readout

General ratings

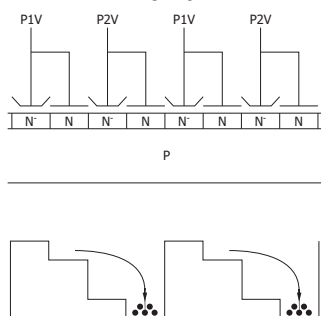
Parameter	S11155-2048	S11156-2048
Pixel size	14 (H) $\times$ 500 (V) μ m	14 (H) $\times$ 1000 (V) μ m
Number of total pixels	2068 (H) $\times$ 1 (V)	
Number of active pixels	2048 (H) $\times$ 1 (V)	
Active area	28.672 (H) $\times$ 0.500 (V) mm	28.672 (H) $\times$ 1.000 (V) mm
Horizontal clock phase	2-phase	
Output circuit	Two-stage MOSFET source follower	
Package	24-pin ceramic DIP (refer to dimensional outline)	
Window ^{*1}	Quartz glass	

*1: Temporary window type (ex. S11155-2048N) is available upon request.

Resistive gate structure

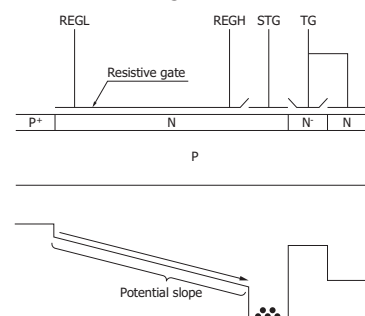
In ordinary CCDs, one pixel contains multiple electrodes and a signal charge is transferred by applying different clock pulses to those electrodes [Figure 1]. In resistive gate structures, a single high-resistance electrode is formed in the active area, and a signal charge is transferred by means of a potential slope that is created by applying different voltages across the electrode [Figure 2]. Compared to a CCD area image sensor which is used as a linear sensor by line binning, a one-dimensional CCD having a resistive gate structure in the active area offers higher speed transfer, allowing readout with low image lag even if the pixel height is large.

[Figure 1] Schematic diagram and potential of ordinary 2-phase CCD



KMPDC0320EA

[Figure 2] Schematic diagram and potential of resistive gate structure



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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*2 *3	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
Vret voltage	Vret	-0.5	-	+18	V
ARD voltage	VARD	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
ARG voltage	VARG	-10	-	+15	V
STG voltage	VSTG	-10	-	+15	V
IGH voltage	VIG1H, VIG2H	-10	-	+15	V
SG voltage	VSG	-10	-	+15	V
OG voltage	VOG	-10	-	+15	V
RG voltage	VRG	-10	-	+15	V
TG voltage	VTG	-10	-	+15	V
Resistive gate voltage	High	VREGH	-10	+15	V
	Low	VREGL			
Horizontal clock voltage	VP1H, VP2H	-10	-	+15	V

*2: Chip temperature

*3: The chip temperature may increase due to heating in high-speed operation. We recommend taking measures to dissipate heat as needed. For more details, refer to the technical information.

■ Operating conditions (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage	VOD	12	15	18	V
Reset drain voltage	VRD	14	15	16	V
All reset drain voltage	VARD	11	12	13	V
All reset gate voltage	High*4	VARGH	7	8	V
	Low*5	VARGL	-2	-1.5	
Output gate voltage	VOG	4.5	5	5.5	V
Storage gate voltage	VSTG	-	0	-	V
Substrate voltage	VSS	-	0	-	V
Resistive gate high voltage	High	VREGHH	-3.5	-3	V
	Low	VREGHL	-9	-8	
Resistive gate low voltage	High	VREGLH	-	VREGHH - 2.5	V
	Low	VREGLL	-9	-8	
Output amplifier return voltage	Vret	-	1	2	V
Test point	Horizontal input source	VISH	-	VRD	V
	Horizontal input gate	VIG1H, VIG2H	-9	-8	V
Horizontal shift register clock voltage	High	VP1HH, VP2HH	5	6	V
	Low	VP1HL, VP2HL	-6	-5	
Summing gate voltage	High	VSGH	5	6	V
	Low	VSGL	-6	-5	
Reset gate voltage	High	VRGH	7	8	V
	Low	VRGL	-6	-5	
Transfer gate voltage	High	VTGH	8.5	9	V
	Low	VTGL	-7.5	-7	
External load resistance	RL	2.0	2.2	2.4	kΩ

*4: All reset on

*5: All reset off

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	5	10	MHz
Line rate	LR	-	2	4	kHz
Horizontal shift register capacitance	CP1H, CP2H	-	200	-	pF
All reset gate capacitance	CARG	-	100	-	pF
Resistive gate capacitance	S11155-2048	-	1000	-	pF
	S11156-2048	-	2000	-	
Summing gate capacitance	CSG	-	10	-	pF
Reset gate capacitance	CRG	-	10	-	pF
Transfer gate capacitance	CTG	-	100	-	pF
Charge transfer efficiency*6	CTE	0.99995	0.99999	-	-
DC output level	Vout	7	8	9	V
Output impedance	Zo	-	300	-	Ω
Output amplifier return current	Iret	-	0.4	-	mA
Power consumption	S11155-2048	PAMP*7	75	-	mW
		PREG*8	2.5	12.5	
	S11156-2048	PAMP*7	75	-	
		PREG*8	1.3	6.3	
Resistive gate resistance*9	S11155-2048	RREG	0.5	2.5	kΩ
	S11156-2048		1	5	

*6: Charge transfer efficiency per pixel of CCD shift register, measured at half of the full well capacity

*7: Power consumption of the on-chip amplifier plus load resistance

*8: Power consumption at REG

*9: Resistance value between REGH and REGL

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	S11155-2048			S11156-2048			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Saturation output voltage	Vsat	-	Fw x Sv	-	-	Fw x Sv	-	V
Full well capacity	Fw	-	200	-	-	200	-	ke ⁻
CCD node sensitivity	Sv	7	8	9	7	8	9	μV/e ⁻
Dark current*10	Non-MPP operation	DS	-	50	-	100	600	ke ⁻ /pixel/s
	MPP operation		-	4		8	32	
Readout noise*11	Nr	-	30	45	-	30	45	e ⁻ rms
Dynamic range*12	DR	-	6670	-	-	6670	-	-
Spectral response range	λ	-	200 to 1100	-	-	200 to 1100	-	nm
Photo response non-uniformity*13, *14	PRNU	-	±3	±10	-	±3	±10	%
Image lag*13	L	-	0.1	1	-	0.1	1	%

*10: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.

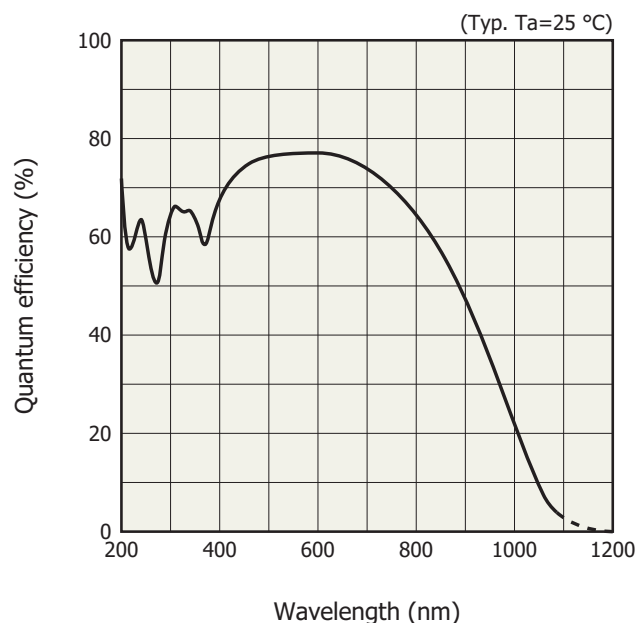
*11: Readout frequency is 2 MHz

*12: Dynamic range (DR) = Full well capacity / Readout noise

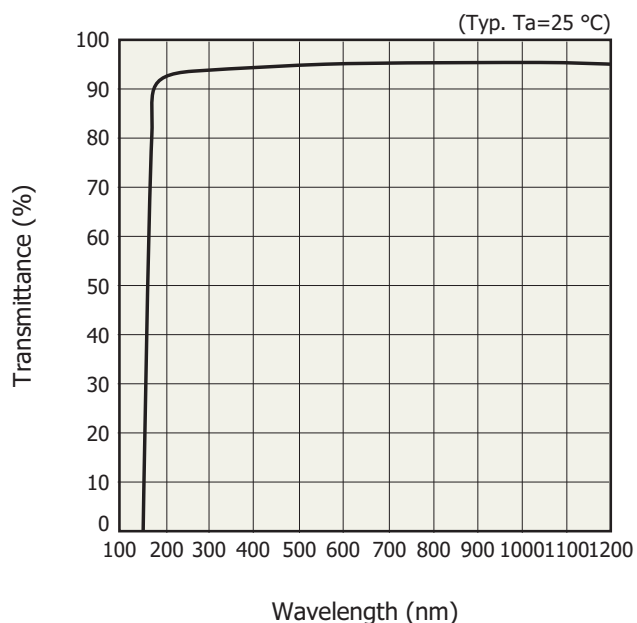
*13: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)

*14: Photo response non-uniformity = $\frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$ [%]

▣ Spectral response (without window)*15



▣ Spectral transmittance characteristic of window material



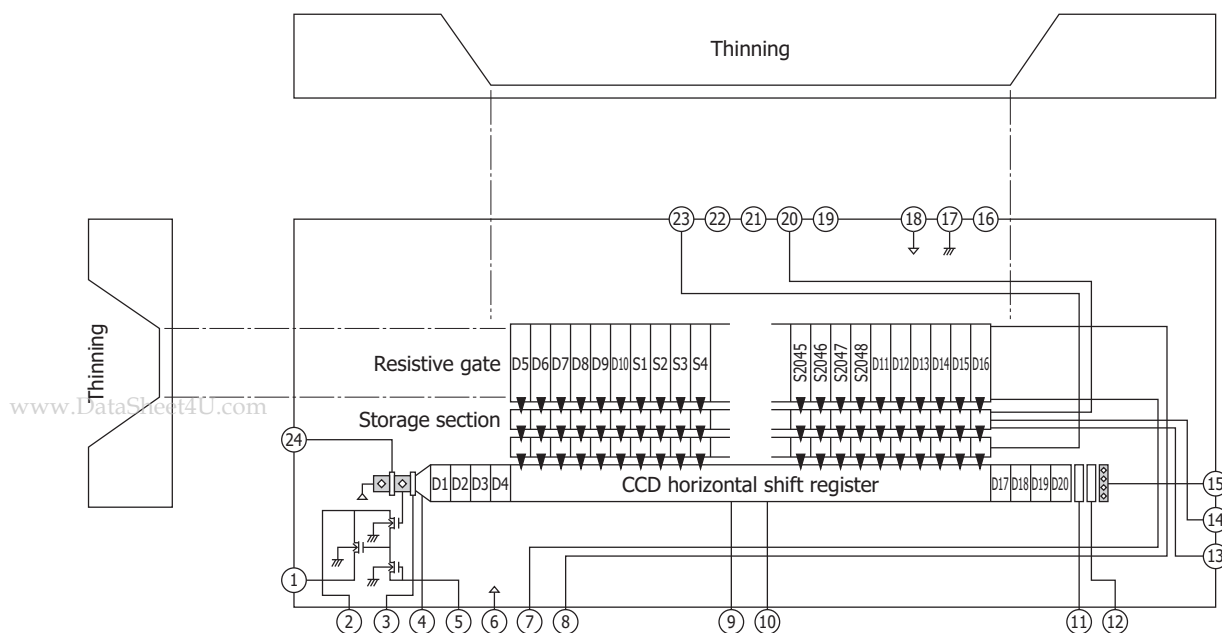
*15: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

▣ Window material

Type No.	Window material
S11155-2048 S11156-2048	Quartz glass*16 (option: window-less)

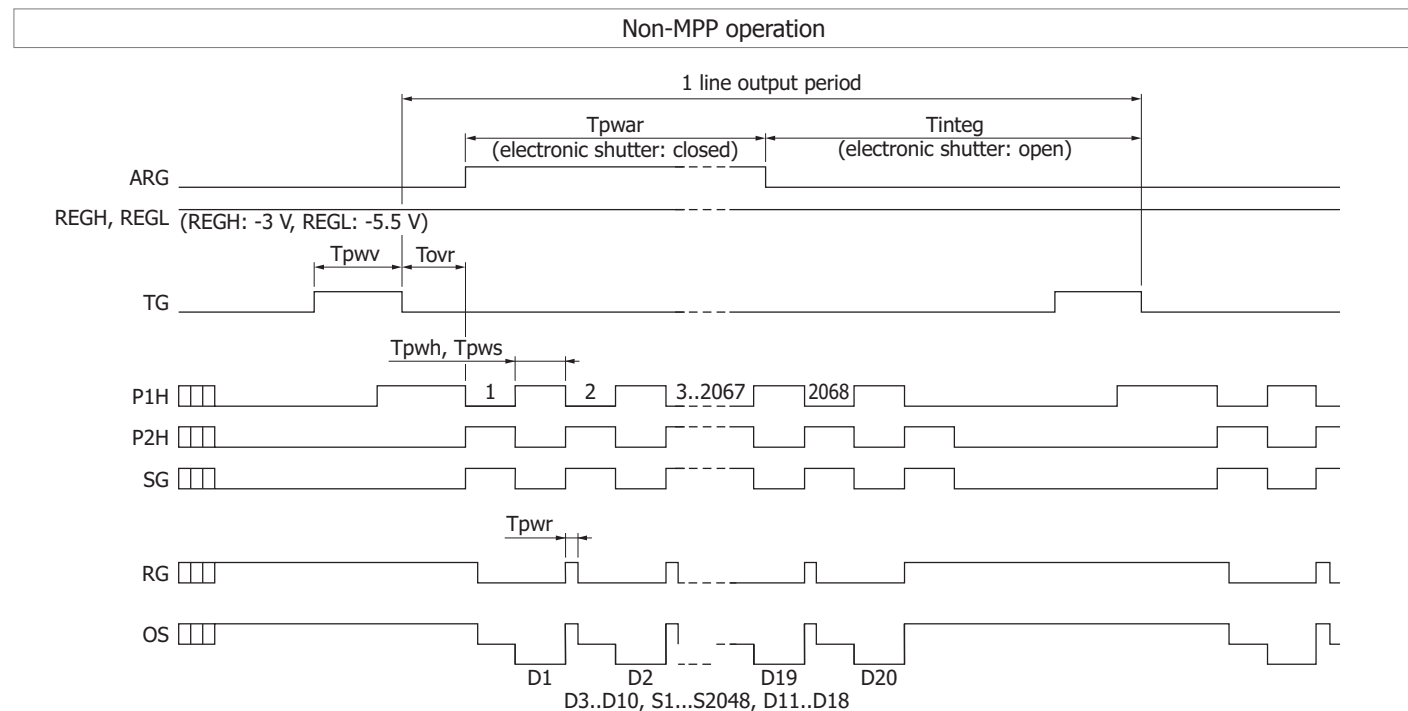
*16: Resin sealing

▣ Device structure (conceptual drawing of top view in dimensional outline)



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Timing chart

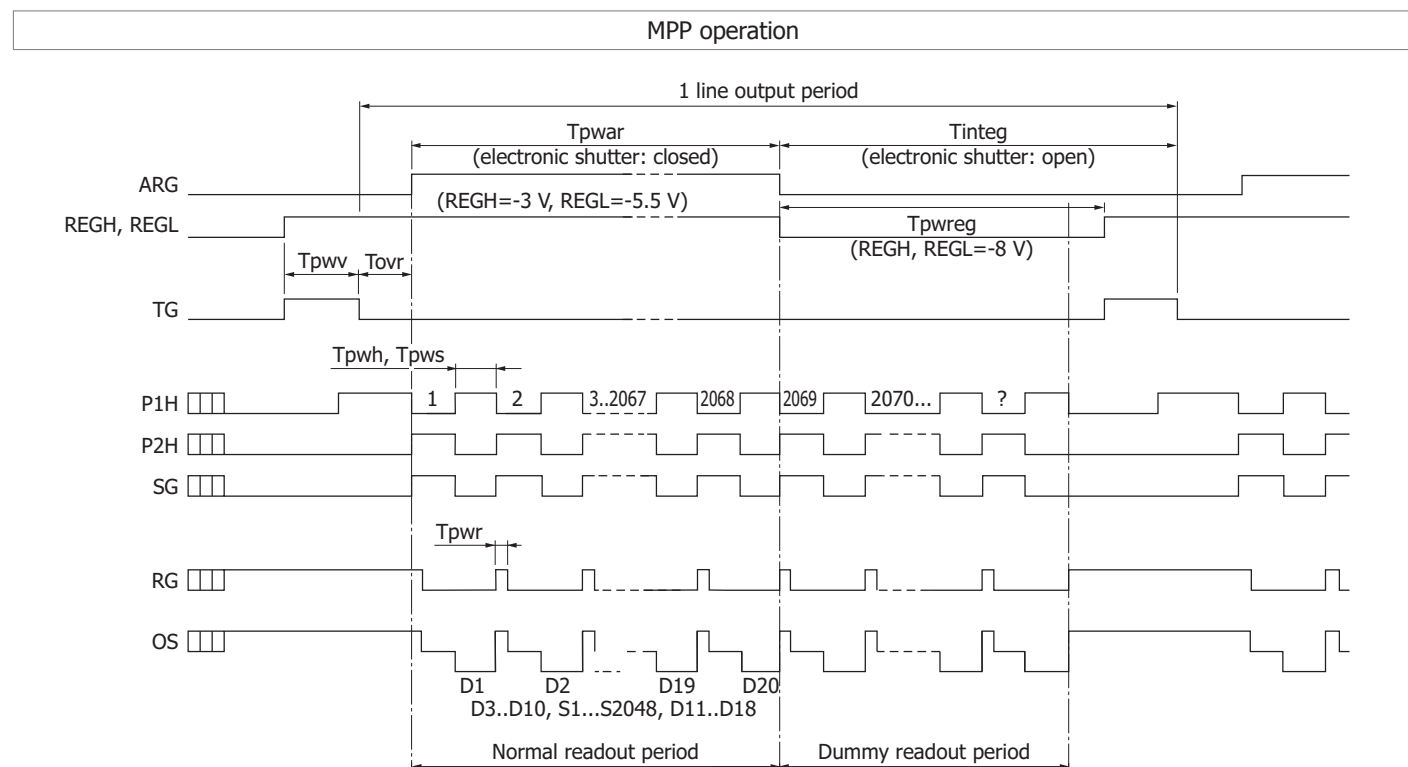


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Parameter		Symbol	Min.	Typ.	Max.	Unit
ARG	Pulse width	Tpwar	1	-	-	µs
	Rise and fall times	Tprar, Tpfar	200	-	-	ns
TG	Pulse width	Tpww	30	-	-	µs
	Rise and fall time	Tprv, Tpfv	20	-	-	ns
P1H, P2H*17	Pulse width	Tpwh	50	100	-	ns
	Rise and fall time	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	50	100	-	ns
	Rise and fall time	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	5	15	-	ns
	Rise and fall time	Tprf, Tpfrr	5	-	-	ns
TG - P1H	Overlap time	Tovr	1	2	-	µs
Integration time		Tinteg	30	-	-	µs

*17: Symmetrical clock pulses should be overlapped at 50% of maximum amplitude.

Timing chart



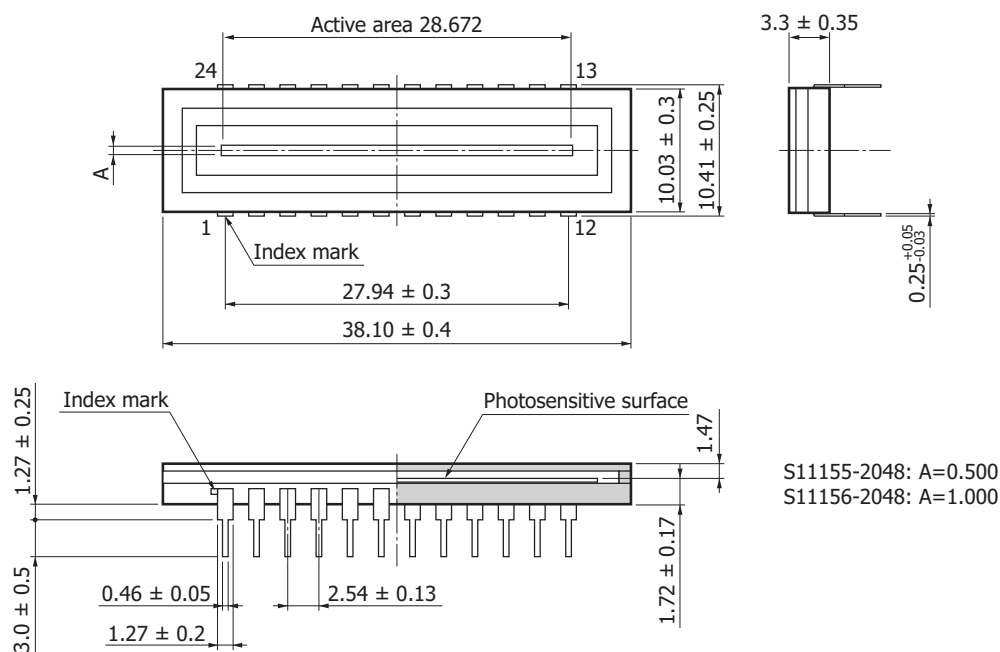
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Parameter		Symbol	Min.	Typ.	Max.	Unit
ARG	Pulse width	Tpwar	*18	-	-	μs
	Rise and fall times	Tprar, Tpfar	200	-	-	ns
REGH, REGL	Pulse width	Tpwreg	-	Tinteg - Tpwv	-	μs
	Rise and fall times	Tprreg, Tpfreg	100	-	-	ns
TG	Pulse width	Tpwv	30	-	-	μs
	Rise and fall times	Tprv, Tpfv	20	-	-	ns
P1H, P2H*19	Pulse width	Tpwh	50	100	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	50	100	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	5	15	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG - P1H	Overlap time	Tovr	1	2	-	μs
Integration time		Tinteg	30	-	-	μs

*18: The Min. value of T_{pwar} is equal to the normal readout period.

*19: Symmetrical clock pulses should be overlapped at 50% of maximum amplitude.

Dimensional outline (unit: mm)



KMPDA0262EB

Pin connections

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	$R_L=2.2\text{ k}\Omega$
2	OD	Output transistor drain	+15 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P2H
5	Vret	Output amplifier return	+1 V
6	RD	Reset drain	+15 V
7	REGL	Resistive gate (low)	-5.5 V (Non-MPP operation)
8	REGH	Resistive gate (high)	-3 V (Non-MPP operation)
9	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	-8 V
12	IG1H	Test point (horizontal input gate-1)	-8 V
13	ARG	All reset gate	
14	ARD	All reset drain	+12 V
15	ISH	Test point (horizontal input source)	Connect to RD
16	-		
17	SS	Substrate	GND
18	RD	Reset drain	+15 V
19	-		
20	STG	Storage gate	0 V
21	-		
22	-		
23	TG	Transfer gate	
24	RG	Reset gate	

Related information

http://jp.hamamatsu.com/sp/ssd/CCD_e.html

- Characteristics and use of resistive gate type CCD linear image sensors with electronic shutter

Driver circuits for CCD linear image sensor (S11155-2048, S11156-2048) C11165 [sold separately]

The C11165 is a driver circuit designed for HAMAMATSU CCD linear image sensors S11155-2048, S11156-2048. The C11165 can be used in spectrometer when combined with the CCD linear image sensor.

Features

- Built-in 16-bit A/D converter
- Interface of computer: USB 2.0
- Operates by DC+5 V



Information furnished by HAMAMATSU is believed to be reliable. However, no responsibility is assumed for possible inaccuracies or omissions.

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Type numbers of products listed in the specification sheets or supplied as samples may have a suffix "(X)" which means tentative specifications or a suffix "(Z)" which means developmental specifications. ©2010 Hamamatsu Photonics K.K.

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