

# VSC9118

# VITESSE

## 10 Gb/s / Quad 2.5 Gb/s Multi-Service SONET/SDH Mapper Device with Virtual Concatenation



### FEATURES:

- ( 64 STS-1/VC-3, 48 TU-3/VC-3, or 16 STS-3c/VC-4 Virtual Concatenation Groups
- ( Link Capacity Adjustment Scheme (LCAS) with Hitless Adds and Removes and Fault Isolation
- ( External DDR 64 bit SDRAM for Diverse Routing Applications. Differential Delays of up to 108 ms
- ( Flexible Payload Processing for Generic Framing Procedure (GFP). Support for Several Interfacing Formats including Ethernet Frames
- ( Supports HDLC-like framing: PoS - RFC2615, LAPS - X.85, and X.86
- ( System Packet Interface Level 4 (SPI-4), Phase 2, 16-bit Interface
- ( Dual 4x 2.5 Gb/s Serial STS-48/STM-16-like Backplane Interfaces or Dual 4 x 622 Mb/s Serial STS-12/STM-4-like Backplane Interfaces with Performance Monitoring for Connection to Working and Protection TSIs
- ( SerDes Framer Interface Level 4 (SFI-4) 16-bit Interface
- ( Full Access to SONET/SDH Section and Line-Overhead Bytes via Dedicated Ports
- ( Access to Selected Section and Line Overhead Bytes via Special Purpose Ports
- ( Complete STS-192/VC-4-64 Section, Line, and Path Termination and Generation
- ( Two-Level Pointer Generation and Interpretation for SDH Mapping of TU-3/VC-3 into AU-4
- ( Channelized Payload Mapping into AU-4/TU-3/VC-3, STS-1/VC-3, STS-3c/VC-4, STS-12c/VC-4-4c, STS-48c/VC-4-16c or Virtual Groups Composed of AU-4/TU-3/VC-3s, STS-1/VC-3s, or STS-3c/VC-4s
- ( Extensive Performance Monitoring Features

### BENEFITS:

- ( Allocated bandwidth for each data channel can be dynamically changed without interrupting the traffic utilizing the Link Capacity Adjustment Scheme (LCAS) to signal bandwidth changes to the receiving end. This makes the VSC9118 well suited for carrying multiple varying data flows from different customers with excellent bandwidth allocation granularity and efficiency.
- ( Available data channels or payloads can be shared among any number of the possible maximum 48 transport channels by utilizing contiguous concatenation and/or virtual concatenation at AU-4/TU-3/VC-3, STS-1/VC-3, or STS-3c/VC-4 levels.

### APPLICATIONS:

- ( Point-to-Point Linear Configurations Such as a Multi-Service Router/Switch or Point-to-Point Transport
- ( SONET/SDH ADM and TSI Switching Systems
- ( Gigabit Ethernet Transport Applications Utilizing LAPS or GFP Frame Encapsulations
- ( Point-to-point Packet-Over-SONET (PoS) Router Applications
- ( Data Channels or Payloads can be Shared Among up to 192 Transport Channels by Using Contiguous Concatenation and/or Virtual Concatenation

### STANDARDS:

- ( ANSI T1.105, Telcordia GR-253-CORE, and ITU-T G.707 Compliant
- ( HDLC-Like Framing: PoS - RFC2615, LAPS - X.85, and X.86
- ( OIF-SFI4-01.0 (OC-192) SFI-4 16-bit Line Interface
- ( OIF-SPI4-02.0 (OC-192) SPI-4.2 16-bit Packet Interface

### GENERAL DESCRIPTION:



The VSC9118 is a 10 Gb/s multi-service SONET/SDH data mapping device that supports both contiguously concatenated and virtually concatenated transport channels.

The AU-3/TU-3/VC-3, STS-1/VC-3, and STS-3c/VC-4 transport channels may be virtually concatenated to support larger custom transport channels. Up to 64 packet streams can be mapped into these transport channels.

Virtual concatenation of AU-3/TU-3/VC-3, STS-1/VC-3, or STS-3c/VC-4 transport channels into Virtual Groups is supported through SONET/SDH.

Path Overhead H4 byte is processed for payload identifiers, types, and sequencing. Non-contiguous transport channels can be tagged and linked through these overhead bytes to form larger, custom transport channels.

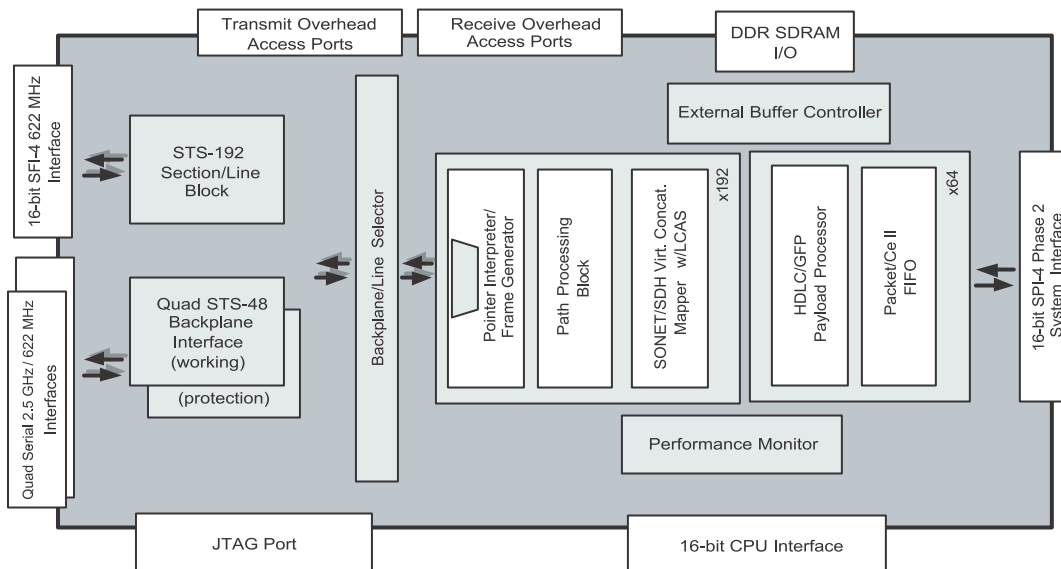
The (LCAS) protocol is supported by processing the H4 byte control packets and reporting back member status.

Flexible Payload Processing for (GFP) is supported for several interfacing formats including Ethernet Frames. It also supports HDLC-like framing: PoS - RFC2615, LAPS - X.85, and X.86

### SPECIFICATIONS:

- ( Line Interface Speed: 622 Mb/s (16 bits), OIF-SFI4-01.0 (OC-192) SFI-4 Interface
- ( Backplane Interface Speed: Dual 4 x 2.5 Gb/s Serial or Dual 4 x 622 Mb/s Serial
- ( Packet Interface Speed Out: 830 Mb/s or 622 Mb/s (16 bits), SPI-4 Phase 2 (or 700 Mb/s w / ext ref)
- ( Packet Interface Speed in: up to 830 Mb/s (16 bits), SPI-4 Phase 2
- ( Virtual Concatenation Groups: up to 48 (up to 16 for STS-3c/AU-4)
- ( CPU Asynchronous Interface: Motorola™ and Intel™
- ( CPU Synchronous Interface: PowerPC™ and Intel™ StrongARM™
- ( Diagnostic Interface: IEEE 1149.1 JTAG
- ( Physical Package Configuration: 728-Pin TBGA
- ( Maximum Power Dissipation: 12 W
- ( Supply Voltages: +1.8 V and +2.5 V
- ( Temperature Range: 0 °C to +85 °C Ambient

### APPLICATION DIAGRAM:



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