Programmable logic arrays (18 × 42 × 10)

PLS153/A

DESCRIPTION

The PLS153 and PLS153A are two-level logic elements, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS153 and PLS153A are field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

FEATURES

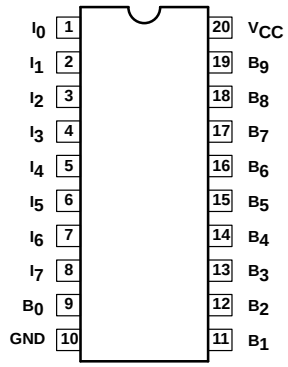
- Field-Programmable (Ni-Cr links)
- 8 inputs
- 42 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active-High or -Low outputs
- 42 product terms:
  - 32 logic terms
  - 10 control terms
- I/O propagation delay:
  - PLS153: 40ns (max)
  - PLS153A: 30ns (max)
- Input loading: –100µA (max)
- Power dissipation: 650mW (typ)
- 3-State outputs
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

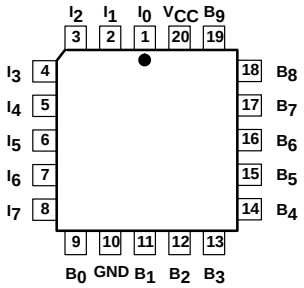
PIN CONFIGURATIONS

N Package



N = Plastic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

SP00274

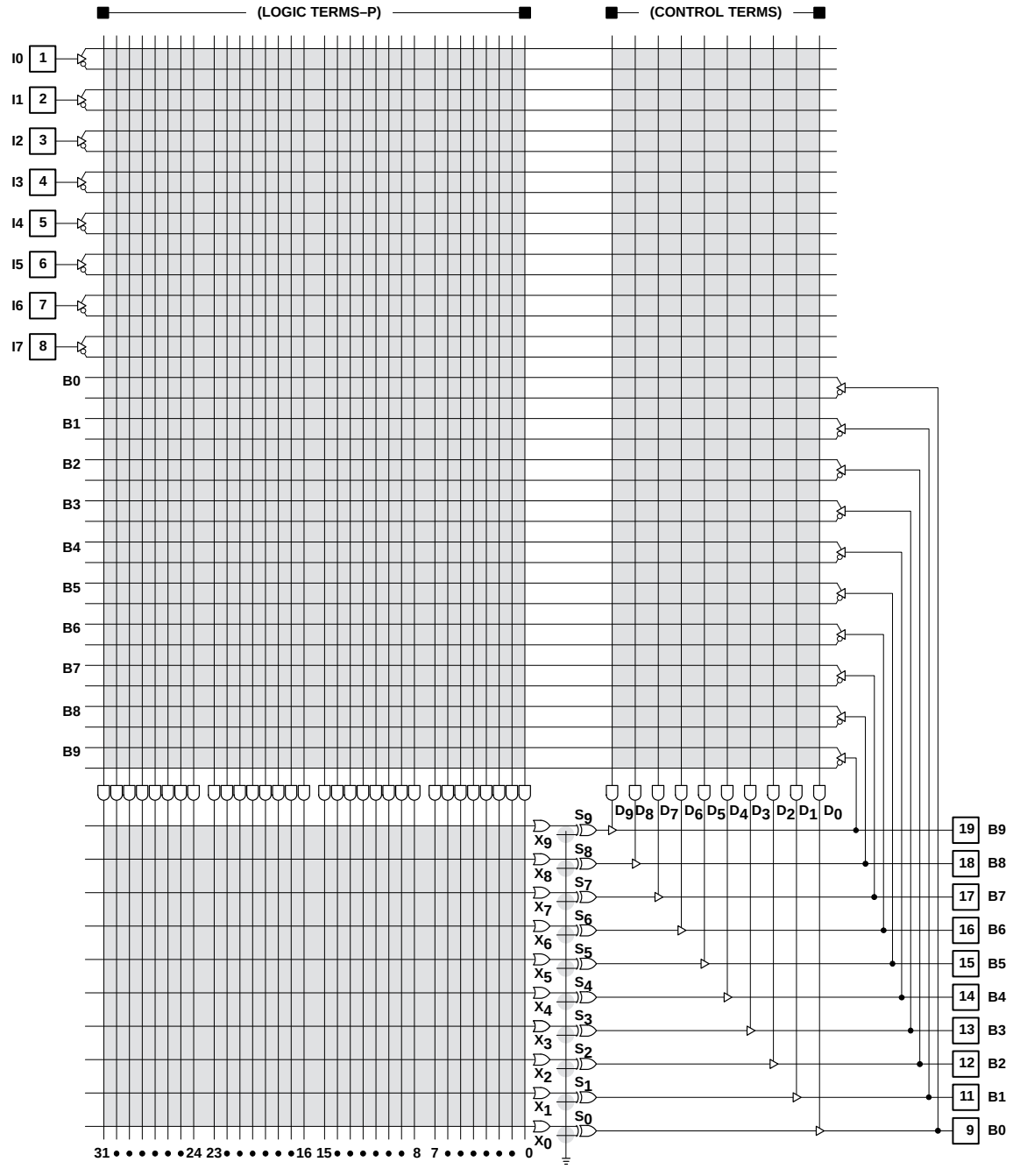
ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
20-Pin Plastic Dual In-Line, 300mil-wide	PLS153N, PLS153AN	0408B
20-Pin Plastic Leaded Chip Carrier	PLS153A, PLS153AA	0400E

Programmable logic arrays ($18 \times 42 \times 10$)

PLS153/A

LOGIC DIAGRAM



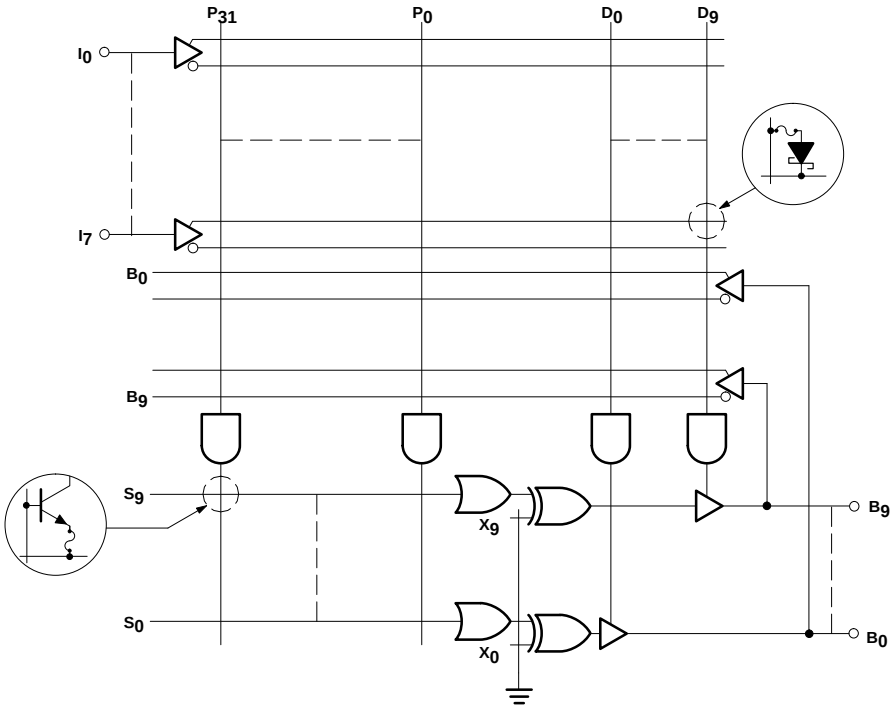
NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ● Programmable connection.

SP00276

Programmable logic arrays ($18 \times 42 \times 10$)

PLS153/A

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \cdot B \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L

$Z = \overline{P0 + P1 + P2 + \ldots}$

$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:
1. For each of the 10 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the Ex-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

SP00275

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150˚C
Maximum ambient	75˚C
Allowable thermal rise ambient to junction	75˚C

The PLS153/A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Philips Semiconductors Military Data Handbook.

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = –2mA	2.4			V
Input current[9]						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = 0.45V			–100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[8]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			–140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		130	155	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with +10V applied to I_7.
5. Measured with +10V applied to $I_{0–7}$. Output sink current is supplied through a resistor to V_{CC}.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with I_0, I_1 at 0V, $I_2 – I_7$ and $B_{0–9}$ at 4.5V.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only ($I_0 – I_7$).

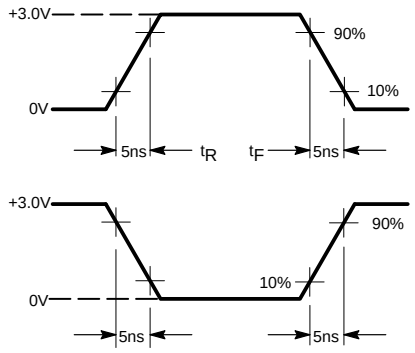
AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 300\Omega$, $R_2 = 390\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS						UNIT
					PLS153			PLS153A			
					MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PD}	Propagation delay	Input ±	Output ±	C_L = 30pF		30	40		20	30	ns
t_{OE}	Output enable[2]	Input ±	Output –	C_L = 30pF		25	35		20	30	ns
t_{OD}	Output disable[2]	Input ±	Output +	C_L = 5pF		25	35		20	30	ns

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} – 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
3. All propagation delays are measured and specified under worst case conditions.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

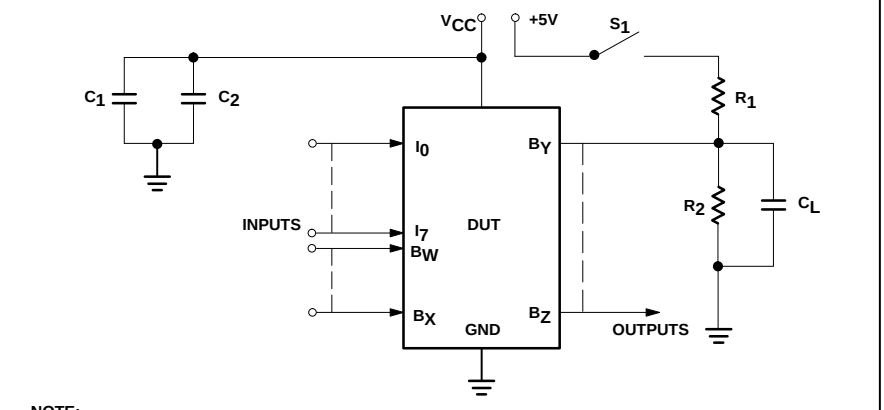
Input Pulses

SP00017

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TEST LOAD CIRCUIT



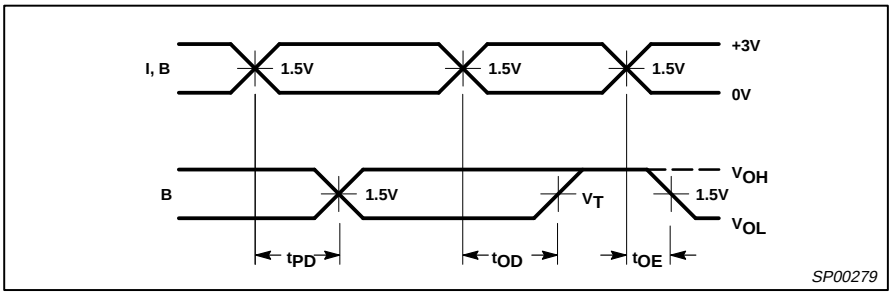
NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

SP00278

Programmable logic arrays ($18 \times 42 \times 10$)

PLS153/A

TIMING DIAGRAM



LOGIC PROGRAMMING

The PLS153/A is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP, Data I/O's ABEL™ and Logical Devices, Inc. CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

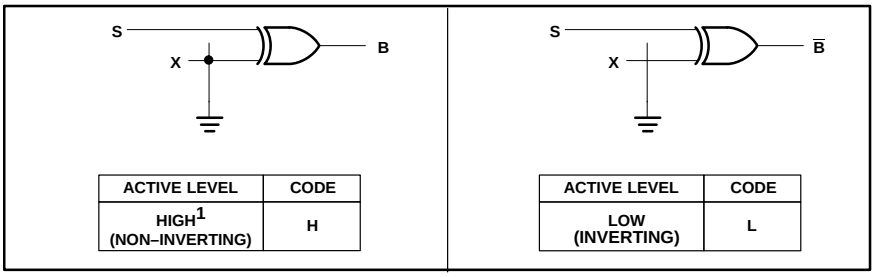
PLS153/A logic designs can also be generated using the program table entry format detailed on the following page. This program table entry format is supported by the Philips Semiconductors SNAP PLD design software package.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-Party Programmer/ Software Support)* of this data handbook for additional information

OUTPUT POLARITY – (B)

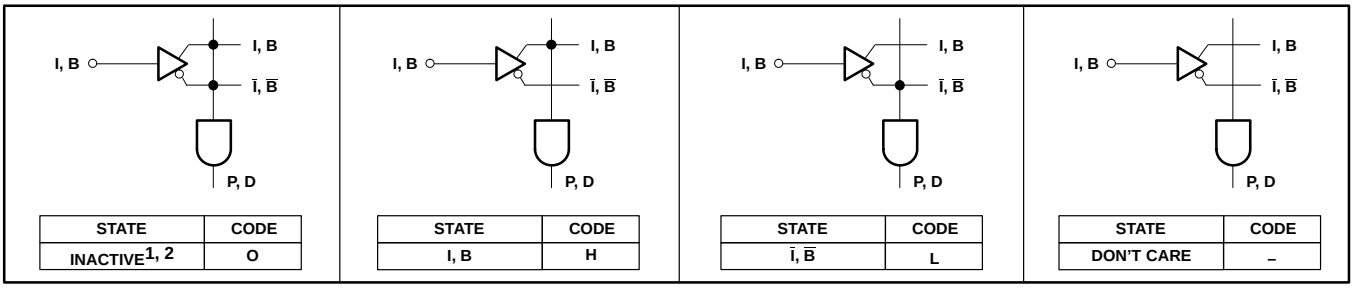


ACTIVE LEVEL	CODE
HIGH[1] (NON–INVERTING)	H

ACTIVE LEVEL	CODE
LOW (INVERTING)	L

SP00280

AND ARRAY – (I, B)



STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

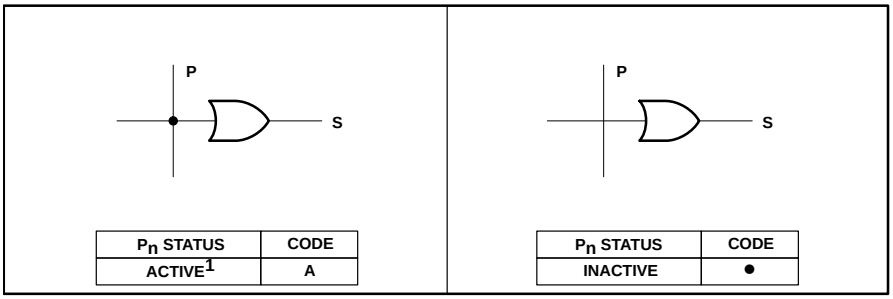
STATE	CODE
Ī, B̄	L

STATE	CODE
DON'T CARE	–

SP00281

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A

P_n STATUS	CODE
INACTIVE	●

SP00282

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditionally inhibited if both the True and Complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:
1. All outputs are at “H” polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

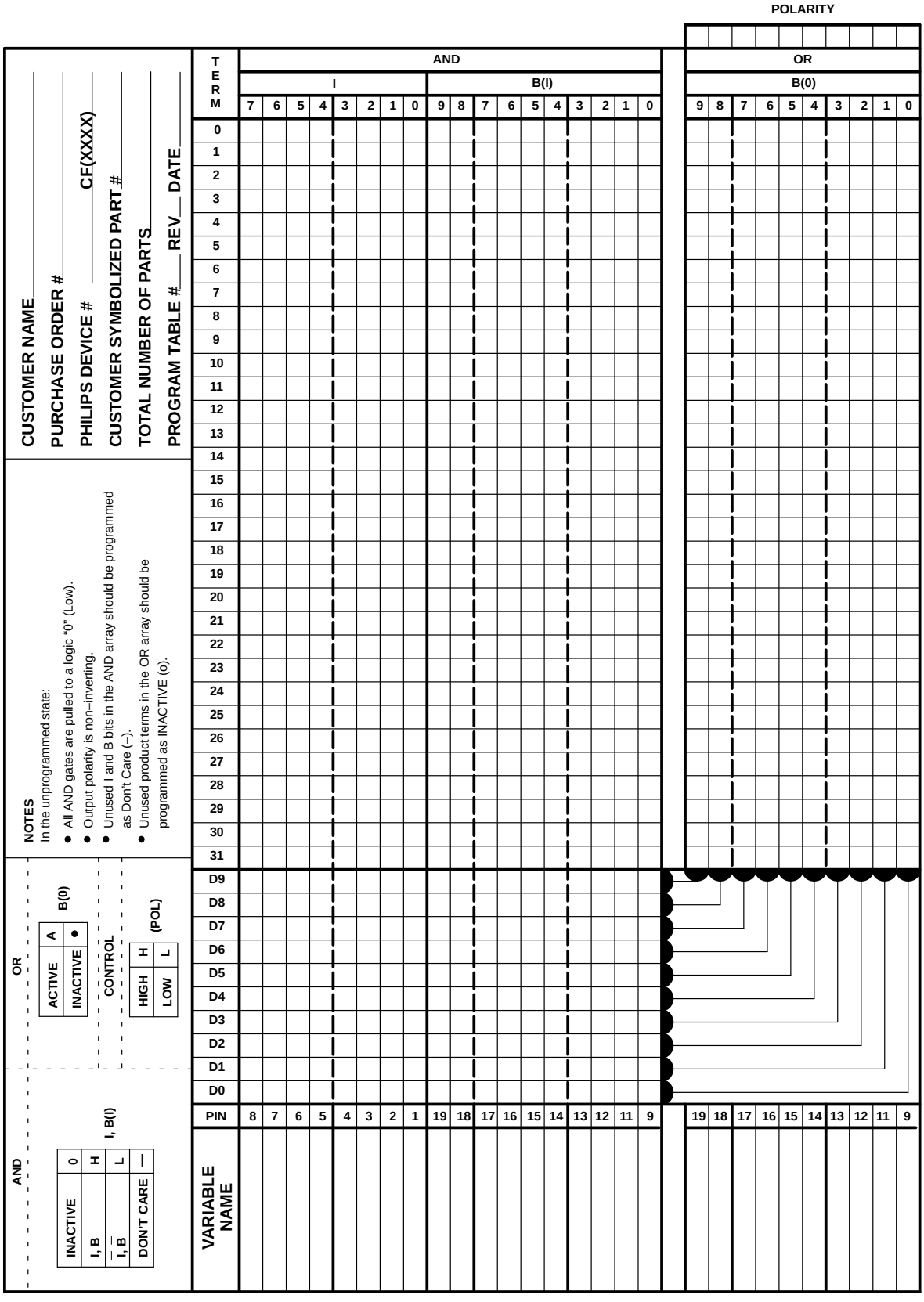
CAUTION: PLS153A TEST COLUMNS

The PLS153A incorporates two columns not shown in the logic block diagram. These columns are used for in-house testing of the device in the unprogrammed state. These columns must be disabled prior to using the PLS153A in your application. If you are using a Philips Semiconductors-approved programmer, the disabling is accomplished during the device programming sequence. If these columns are not disabled, abnormal operation is possible.
Furthermore, because of these test columns, the PLS153A cannot be programmed using the programmer algorithm for the PLS153.

Programmable logic arrays ($18 \times 42 \times 10$)

PLS153/A

PROGRAM TABLE



SP00283

Programmable logic arrays ($18 \times 42 \times 10$) PLS153/A

SNAP RESOURCE SUMMARY DESIGNATIONS