

# DATA SHEET

## **CBT6820**

20-bit bus switch with precharged outputs  
and Schottky undershoot protection for  
live insertion

Product specification  
Supersedes data of 1999 Apr 05

2000 Jun 19

# 20-bit bus switch with precharged outputs and Schottky undershoot protection for live insertion

## CBT6820

### FEATURES

- TTL compatible inputs and outputs
- 5  $\Omega$  switch connection between two port A and port B
- Thin shrink small outline (TSSOP)
- Undershoot protection included to prevent shoot through level changes
- Bias voltage pre-charges the outputs to minimize signal distortion during live insertion
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

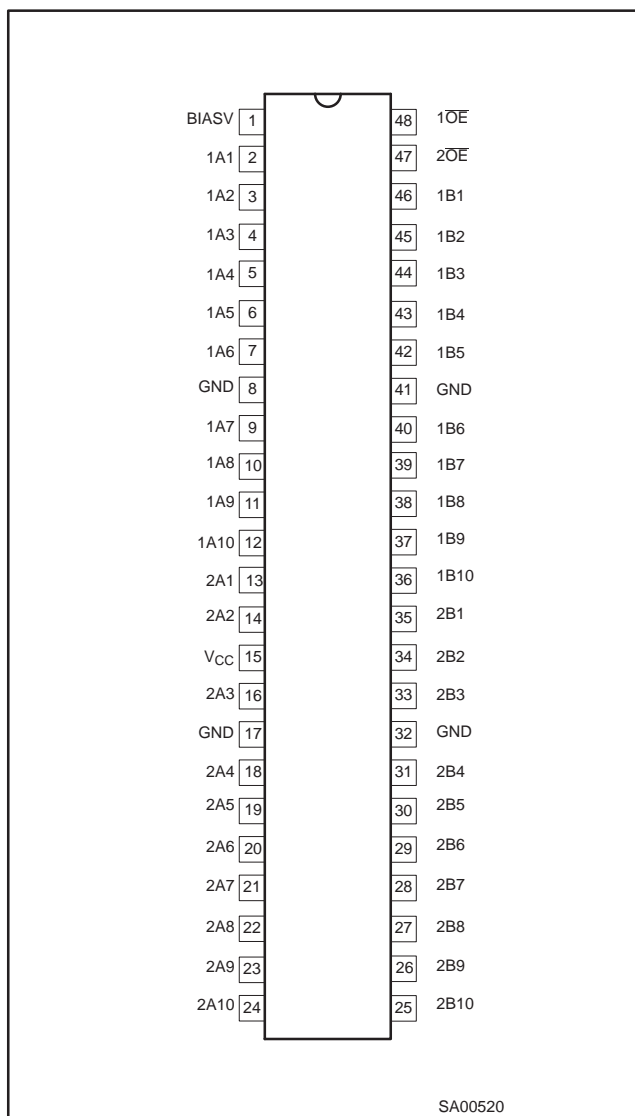
### DESCRIPTION

The CBT6820 provides twenty bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bi-directional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The device is organized as two 10-bit switch with individual enable (OE) input. When OE is low, the switch is on and port A is connected to port B. When OE is high, the switch between port A and port B is open and the B port is precharged to BIASV through the equivalent of a 10 k $\Omega$  resistor.

Special clamp circuitry and Schottky diode clamps to ground are used to prevent an under voltage on the A side ( $V_{in} < GND$ ) from causing the B side precharge voltage to drop below the "1" state.

### PIN CONFIGURATION



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$ ; $GND = 0V$	TYPICAL	UNIT
$t_{PLH}/t_{PHL}$	Propagation delay An to Bn or Bn to An	$C_L = 50 \text{ pF}$ , $V_{CC} = 5 \text{ V}$	0.25	ns
$C_{IN}$	Input capacitance		4.5	pF
$C_{I/O}$	Input/output capacitance	Outputs disabled; $V_O = 0 \text{ V}$ or $V_{CC}$	9.5	pF

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	CBT6820 DGG	SOT362-1

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## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	BIASV	Precharge bias voltage input
2, 3, 4, 5, 6, 7, 9, 10, 11, 12	1A1–1A10	Port 1A1 to Port 1A10
8, 17, 32, 41	GND	Ground (V)
13, 14, 16, 18, 19, 20, 21, 22, 23, 24	2A1–2A10	Port 2A1 to Port 2A10
15	V <sub>CC</sub>	Positive supply voltage
35, 34, 33, 31, 30, 29, 28, 27, 26, 25	2B1–2B10	Port 2B1 to Port 2B10
46, 45, 44, 43, 42, 40, 39, 38, 37, 36	1B1–1B10	Port 1B1 to Port 1B10
48, 47	1OE, 2OE	Switch enables

## FUNCTION TABLE

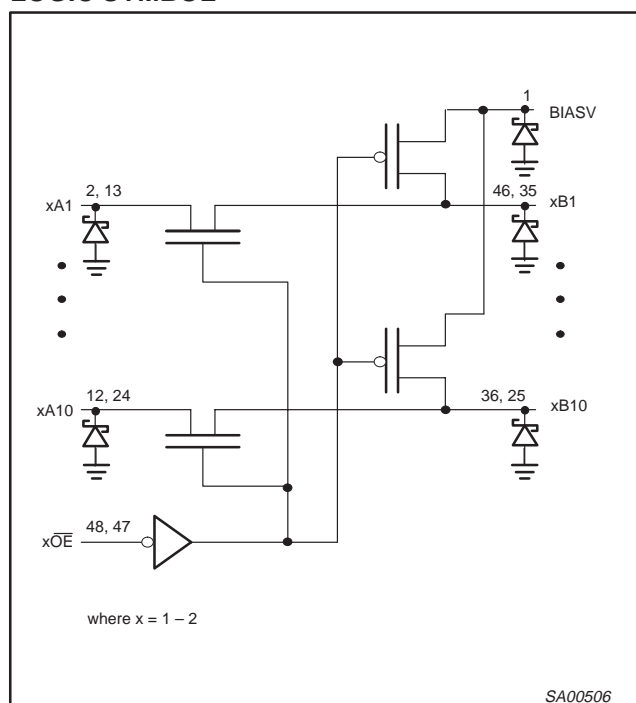
OE	STATE
L	A Port = B Port
H	A Port = Z
H	B Port = BIASV

H = High voltage level

L = Low voltage level

Z = High impedance "off" state

## LOGIC SYMBOL



## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		–0.5 to +7.0	V
I <sub>IK</sub>	DC clamp diode current	V <sub>I</sub> < 0	–50	mA
V <sub>I</sub>	DC input voltage <sup>1</sup>		–0.5 to +7.0	V
I <sub>SW</sub>	DC continuous channel current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±128	mA
V <sub>BIASV</sub>	DC bias voltage		–0.5 to +7.0	V
T <sub>stg</sub>	Storage temperature range		–65 to 150	°C
øJA	Plastic thin shrink small outline package (TSSOP)		104	°C/W

### NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V <sub>CC</sub>	DC supply voltage	4.0	5.5	V
BIASV	DC supply voltage	1.3	V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage (control pin)	2.0		V
V <sub>IL</sub>	Low-level Input voltage (control pin)		0.8	V
T <sub>amb</sub>	Operating free-air temperature range	–40	+85	°C

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T <sub>amb</sub> = −40°C to +85°C			
			Min	Typ <sup>1</sup>	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>I</sub> = −18mA			−1.2	V
I <sub>I</sub>	Input leakage current (control pin)	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V			±5	μA
I <sub>O</sub>	Output bias current (B pins)	V <sub>CC</sub> = 4.5V; BiasV = 2.4V; V <sub>O</sub> = 0, $\overline{\text{OE}}$ = V <sub>CC</sub>			−0.25	mA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			2.5	mA
ΔI <sub>CC</sub>	Control pins <sup>2</sup>	V <sub>CC</sub> = 5.5V, one input at 3.4V, other inputs at V <sub>CC</sub> or GND			2.5	mA
C <sub>I</sub>	Input capacitance per $\overline{\text{OE}}$ pin	V <sub>I</sub> = 3V or 0		4.5		pF
C <sub>O(OFF)</sub>	Capacitance per port (OFF-state)	V <sub>O</sub> = 3V or 0; switch off		9.5		pF
r <sub>on</sub> <sup>3</sup>	On-resistance	V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0V; I <sub>I</sub> = 64mA		5	7	Ω
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0V; I <sub>I</sub> = 30mA		5	7	
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 2.4V; I <sub>I</sub> = −15mA		10	15	
V <sub>P</sub>	Pass voltage	V <sub>IN</sub> = V <sub>CC</sub> = 4.5V; I <sub>out</sub> = −100μA	3.4	3.6	3.9	V
I <sub>USP</sub>	Undershoot static current protection <sup>4</sup>	V <sub>CC</sub> = 5.0V, V <sub>Bias</sub> = V <sub>CC</sub> I <sub>B</sub> = −5μA, V <sub>B</sub> ≥ 3.0V		−10		mA

### NOTES:

1. All typical values are at  $V_{\text{CC}} = 5\text{V}$ ,  $T_{\text{A}} = 25^{\circ}\text{C}$
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{\text{CC}}$  or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.
4. Force  $I_{\text{USP}}$ , measure  $V_{\text{B}} \geq 3\text{V}$

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AC CHARACTERISTICS FOR  $V_{CC} = 5.0V \pm 0.5V$  RANGE

GND = 0V;  $t_r = t_f \leq 2.5ns$ ;  $C_L = 50pF$ .

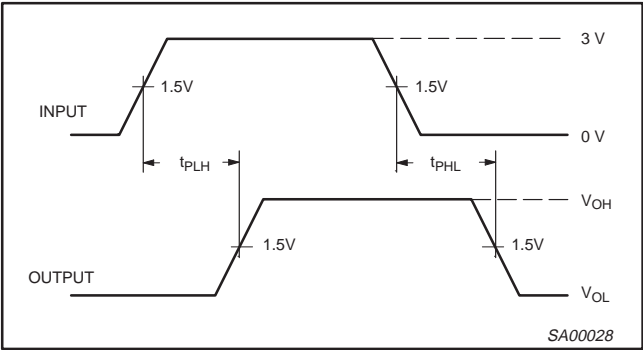
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T <sub>amb</sub> = −40 to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
t <sub>pd</sub>	Propagation delay; An to Bn; Bn to An <sup>2</sup>	1			0.25	ns
t <sub>PZH</sub>	3-State output enable time OE to An; OE to Bn; BIASV = GND	2	1.3	3.1	5.3	ns
t <sub>PZL</sub>	3-State output enable time OE to An; OE to Bn; BIASV = 3.0V	2	1.4	2.9	4.6	ns
t <sub>PHZ</sub>	3-State output enable time OE to An; OE to Bn; BIASV = GND	2	1.7	2.8	4.5	ns
t <sub>PLZ</sub>	3-State output enable time OE to An; OE to Bn; BIASV = 3.0V	2	2.8	4.4	6.6	ns

NOTE:

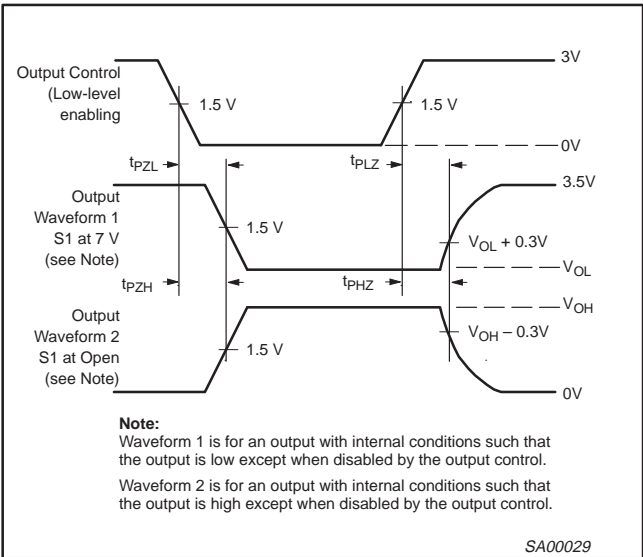
1. All typical values are measured at  $T_{amb} = 25^{\circ}C$  and  $V_{CC} = 5.0V$
2. Warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50pF, when driven by an ideal voltage source (zero output impedance)

AC WAVEFORMS

$V_M = 1.5V$ ,  $V_{IN} = GND \text{ to } 3.0V$



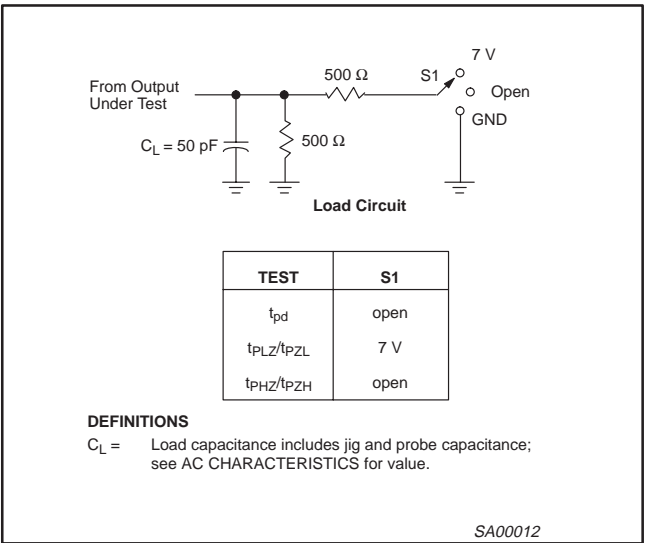
Waveform 1. Waveforms Showing the Input (An) to Output (Bn) Propagation Delays



**Note:**  
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



NOTES:

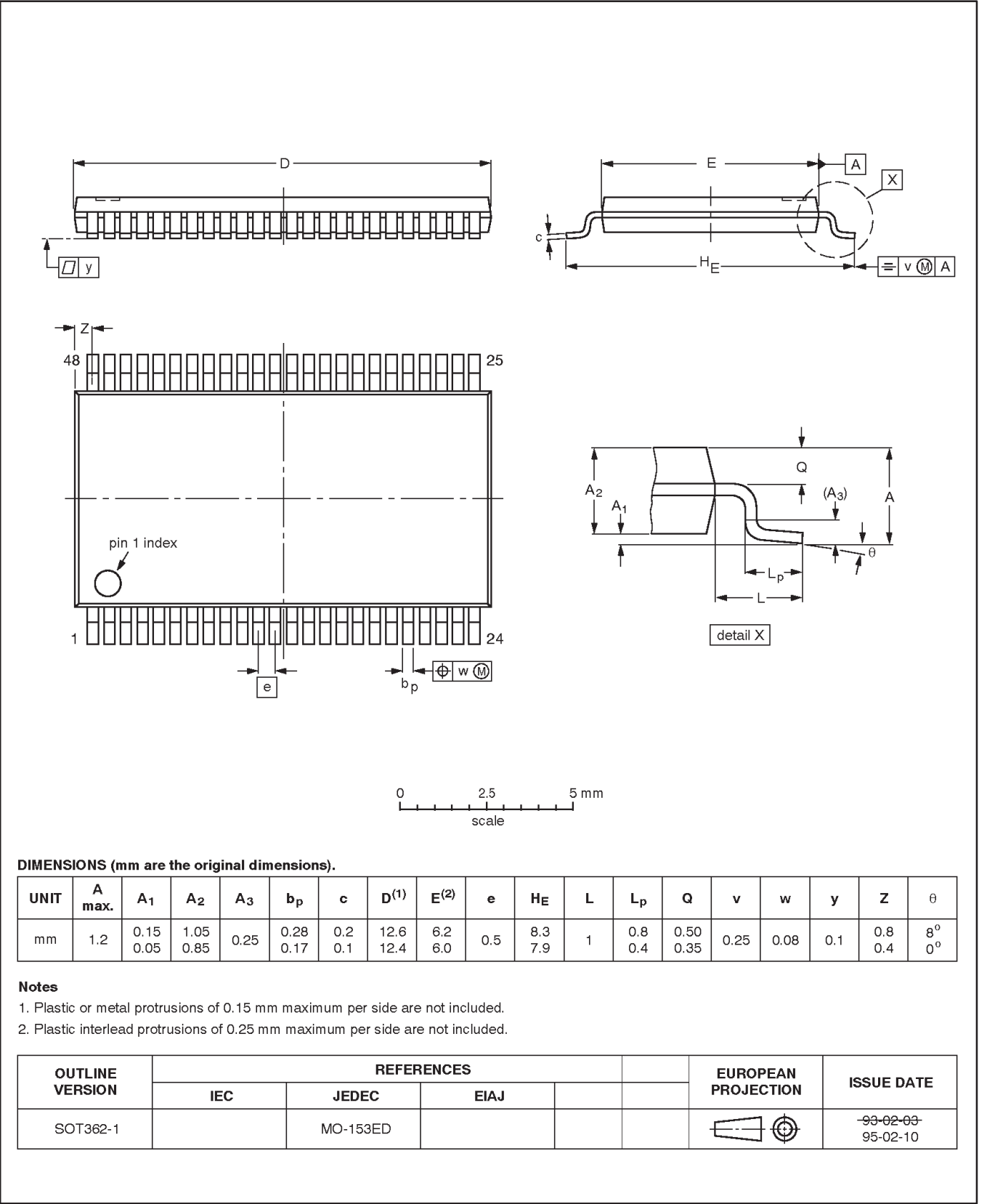
1. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
2. The outputs are measured one at a time with one transition per measurement.

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



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## NOTES

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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print code

Date of release: 06-00

Document order number:

9397 750 07215

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