SPECIFICATION

SPEC. No. A-High-c
D A T E: 2015 Jan.

То

Non-Controlled Copy

CUSTOMER'S PRODUCT NAME

TDK PRODUCT NAME

MULTILAYER CERAMIC CHIP CAPACITORS

CGA Series / Automotive Grade

High Voltage

Please return this specification to TDK representatives.

If orders are placed without returned specification, please allow us to judge that specification is accepted by your side.

RECEIPT CONFIRMATION

DATE: YEAR MONTH DAY

TDK Corporation Sales Electronic Components Sales & Marketing Group TDK-EPC Corporation

Engineering

Ceramic Capacitors Business Group

APPROVED	Person in charge

APPROVED	CHECKED	Person in charge

1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over the other relevant specifications.

Production places defined in this specification shall be TDK-EPC Corporation Japan,

TDK (Suzhou) Co., Ltd and TDK Components U.S.A. Inc.

EXPLANATORY NOTE:

This specification warrants the quality of the ceramic chip capacitors. The chips should be evaluated or confirmed a state of mounted on your product.

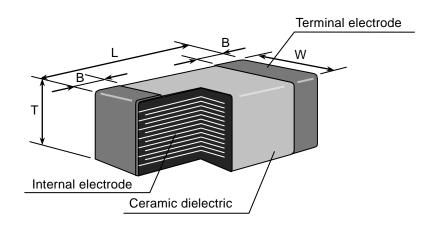
If the use of the chips goes beyond the bounds of the specification, we can not afford to guarantee.

2. CODE CONSTRUCTION

(Example)

Catalog Number : (Web)	<u>CGA8</u> (1)	<u>K</u> (2)	<u>1</u> (3)	X7R (4)	3 D (5)	<u>222</u> (6)	<u>M</u> (7)	130 (8)	<u>K</u> (9)	<u>A</u> (10)
Item Description :	CGA8 (1)	<u>K</u> (2)	<u>1</u> (3)	X7R (4)	3 D (5)	<u>222</u> (6)	<u>M</u> (7)	<u>T</u> (11)	<u>xxxx</u> (12)	

(1) Type



Please refer to product list for the dimension of each product.

(2) Thickness

* As for dimension tolerance, please contact with our sales representative.

Thickness	Dimension(mm)
F	0.85
G	1.10
K	1.30
L	1.60
М	2.00
N	2.30
Р	2.50

(3) Voltage condition in the life test (Max. operating Temp./1000h)

Sign	Condition
1	Rated Voltage x 1

(4) Temperature Characteristics (Details are shown in table 1 No.7 and No.8 at page 5.)



(5) Rated Voltage

Symbol	Rated Voltage
3 A	DC 1 kV
3 D	DC 2 kV
3 F	DC 3 kV

(6) Rated Capacitance

Stated in three digits and in units of pico farads (pF).

The first and Second digits identify the first and second significant figures of the capacitance, the third digit identifies the multiplier.

R is designated for a decimal point.

Example 222 \rightarrow 2,200pF

(7) Capacitance tolerance

Symbol	Tolerance	Capacitance		
F	±1pF	10pF		
K	± 10 %	Over 10pE		
М	± 20 %	Over 10pF		

- (8) Thickness code (Only Catalog Number)
- (9) Package code (Only Catalog Number)
- (10) Special code (Only Catalog Number)
- (11) Packaging

Symbol	Packaging
В	Bulk
Т	Taping

(12) Internal code (Only Item Description)

3. RATED CAPACITANCE AND CAPACITANCE TOLERANCE

3.1 Standard combination of rated capacitance and tolerances

Class	Temperature Characteristics	Capacitano	ce tolerance	Rated capacitance
1	606	10pF	F (±1pF)	10
1	C0G	Over 10pF	K (± 10 %)	E – 12 series
2	X7R X7S		10 %) 20 %)	E –3 series

3.2 Capacitance Step in E series

 E series	Capacitance Step											
 E- 3	1.0				1.0 2.2				4.7			
 E- 12	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2

4. OPERATING TEMPERATURE RANGE

T.C.	Min. operating	Max. operating	Reference		
	Temperature	Temperature	Temperature		
C0G X7R X7S	-55°C	125°C	25°C		

5. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH

6 months Max.

6. P.C. BOARD

When mounting on an aluminum substrate, large case sizes such as CGA6, CGA7, CGA8 and CGA9 types are more likely to be affected by heat stress from the substrate. Please inquire separate specification for the large case sizes when mounted on the substrate.

7. INDUSTRIAL WASTE DISPOSAL

Dispose this product as industrial waste in accordance with the Industrial Waste Law.



8. PERFORMANCE

table 1

			table i	•			
No.	Item	Perfo	rmance	Te	st or inspectio	n method	
1	External Appearance	No defects which performance.	n may affect	Inspect with magnifying glass (3x)			
2	Insulation Resistance	10,000MΩ min.		Apply 500V DC for 60s.			
3	Voltage Proof	Withstand test voinsulation breakd damage.	-	above DC	ischarge curre	oe applied for 1s.	
4	Capacitance	Within the specif	ied tolerance.	Class	Measuring frequency	Measuring voltage	
				Class1	1MHz±10%	0.5 - 5 Vrms.	
				Class2	1kHz±10%	1.0±0.2 Vrms.	
5	Q			See No 4 i	n this table fo	r measuring	
Ü	(Class1)	Rated Capacitance	Q	condition.	Trans table for	measumg	
		30pF and over	1,000 min.				
		Under 30pF 400+20xC min. C : Rated capacitance (pF)					
6	Dissipation Factor				n this table for	r measuring	
	(Class2)	T.C.	0.03 max.	condition.			
		X7\$					
	I	I					

(conti	nued)	T		1		
No.	Item	Performance			Test or inspection method	
7	of Capacitance (Class1) $COG = 0 \pm 30 \text{ (p)}$ Capacitance drift with		Temperature Coefficient 0 ± 30 (ppm/°C) nce drift within ± 0.2% or , whichever larger.	Temperature coefficient shall be calculated based on values at 25°C and 85°C temperature. Measuring temperature below 20°C shall be -10°C and -25°C.		
8	Temperature Characteristics of Capacitance (Class2)	Cap	vacitance Change (%) No voltage applied X7R: ± 15 X7S: ± 22	steps therr step.	s shown i nal equilil	shall be measured by the on the following table after brium is obtained for each sted ref. STEP3 reading Temperature(°C) 25 ± 2 -55 ± 3 25 ± 2 125 ± 2
9	Robustness of Terminations	No sign of termination coming off, breakage of ceramic, or other abnormal signs.		P.C.E	Board sho y a pushir s.	the capacitors on a own in Appendix 1 and ng force of 17.7N with Pushing force P.C.Board
10	Solderability	New solder to cover over 75% of termination. 25% may have pin holes or rough spots but not concentrated in one spot. Ceramic surface of A sections shall not be exposed due to melting or shifting of termination material. A section		solde	er at 235± er : H63A : Isoprop	pak both terminations in 25°C for 2±0.5s. (JIS Z 3282) yl alcohol (JIS K 8839) IS K 5902) 25% solid

(continued)

(cont	inued)		1					
No.	Ite	em		Perfo	rmance	Test or inspection method		
11	Resistance to solder heat	External appearance	termination	ons shal	owed and Il be covered at ew solder.	Completely soak both terminations in solder at 260±5°C for 5±1s.		
		Capacitance				Preheating condition Temp. : 150±10°C		
			Charact	teristics	Change from the value before test	Time : 1 to 2min.		
			Class 1	C0G	± 2.5 %	Flux : Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution.		
			Class 2	X7R X7S	± 7.5 %	Solder : H63A (JIS Z 3282)		
		Q				Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24±2h		
		(Class1)	Rat Capac		Q	(Class2) before measurement.		
			30pF ar	nd over	1,000 min.			
			Under 3	80pF	400+20×C min.			
			C : Rated capacitance (pF)					
		D.F. (Class2)	Meet the					
		Insulation Resistance	Meet the	initial sp	Dec.			
		Voltage proof	No insula other dan		akdown or			
12	Vibration	External appearance	No mechanical damage.			Reflow solder the capacitors on a P.C.Board shown in Appendix 1 before testing.		
		Capacitance	Charac	teristics	Change from the value before test	Vibrate the capacitor with following		
			Class 1	COG	± 2.5 %	conditions. Applied force : 5G max.		
			Class 2	X7R X7S	± 7.5 %	Frequency: 10-2000Hz Duration: 20 min.		
		Q				Cycle: 12 cycles in each 3 mutually perpendicular directions.		
		(Class1)	Rat Capac		Q			
			30pF ar	nd over	1,000 min.			
			Under 3	0pF	400+20×C min.			
			C : Rated capacitance (pF)					
		D.F. (Class2)	Meet the	initial sp	Dec.			

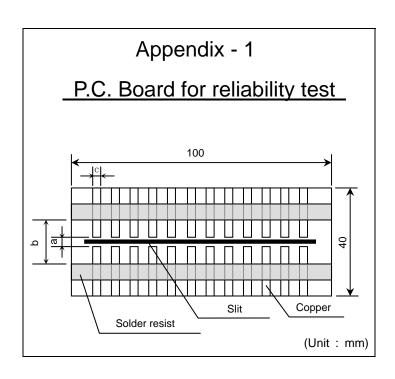
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(con	tinued)		T						
No.	Ite	m	Performance				Test or inspection method		
13	Temperature cycle	External appearance	No mecha	anical da	amage.	P.C.Bo	Reflow solder the capacitors on a P.C.Board shown in Appendix 1 before testing. Expose the capacitors in the condition step1 through step 4 and repeat 1,000		
		Capacitance		eristics	Change from the value before test	Expose			
			Class 1	C0G	±2.5 %		consecutively.		
			Class X7R 2 X7S		±7.5 %	conditi	Leave the capacitors in ambient condition for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.		
		Q (Class1)	Ra	ted		Step	Temperature(°C)	Time (min.)	
				citance	Q	1	-55 ± 3	30 ± 3	
			30pF a	nd over	1,000 min.	2	25 ± 2	2 - 5	
			Under		400+20×C min.	3	125 ± 2	30 ± 2	
			C : Rated	d capacit	ance (pF)	4	25 ± 2	2 - 5	
		D.F. (Class2)	Meet the initial spec.] <u> </u>			
		Insulation Resistance	Meet the	Meet the initial spec.					
		Voltage proof	No insulated		akdown or				
14	Moisture Resistance	External appearance	No mechanical damage.			P.C.Bo	Reflow solder the capacitors on a P.C.Board shown in Appendix 1 before		
	(Steady State)	Capacitance	Characteristics		Change from the value before test	Leave	testing. Leave at temperature 40±2°C, 90 to		
			Class 1	COG	± 5 %	95%RI	95%RH for 500 +24,0h.		
			Class X7R 2 X7S		±12.5 %	conditi	Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24±2h (Class2) before measurement.		
		Q				_	,		
		(Class1)		ited citance	Q				
			30pF a	nd over	350 min.				
			to und	nd over er 30pF	2/5+5/2×C min.				
			C : Rated capacitance (pF)						
		D.F. (Class2)	Character 200% of		oec. max.				
		Insulation Resistance	1,000ΜΩ	min.					

(continued)

No.	lte	em		Perfor	rmance	Test or inspection method											
15	Life	External appearance	No mechanical damage.			Reflow solder the capacitors on a P.C.Board shown in Appendix 1 before											
		Capacitance	Characteristics		Change from the value before test	testing. Apply rated voltage at maximum											
			Class 1	COG	± 3 %	operating temperature ±2°C for 1,000 +48, 0h.											
			Class 2	X7R X7S	±15 %	Charge/discharge current shall not exceed 50mA.											
		Q				1											
		(Class1)	Rated Capacitance 30pF and over		Q	Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24±2h (Class2) before measurement.											
					350 min.	24±211 (Glass2) before measurement.											
														10pF ar to unde		275+5/2×C min.	Voltage conditioning (only for class 2)
			C : Rated capacitance (pF)		ance (pF)	Voltage treat the capacitors under testing temperature and voltage for 1											
		D.F. (Class2)	Characteri 200% of		pec. max.	hour. Leave the capacitors in ambient condition for 24±2h before											
		Insulation Resistance	1,000MΩ min.			measurement. Use this measurement for initial value.											

^{*}As for the initial measurement of capacitors (Class2) on number 8, 11, 12, 13 and 14, leave capacitors at 150 –10,0°C for 1 hour and measure the value after leaving capacitors for 24±2h in ambient condition.



Material: Glass Epoxy (As per JIS C6484 GE4)

P.C. Board thickness: 1.6mm

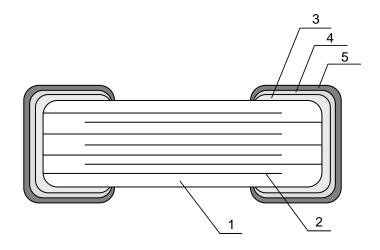
Copper (thickness 0.035mm)

Solder resist

TDK (EIA style)	Dimensions (mm)					
	а	b	С			
CGA5 (CC1206)	2.2	5.0	2.0			
CGA6 (CC1210)	2.2	5.0	2.9			
CGA7 (CC1808)	3.5	7.0	2.5			
CGA8 (CC1812)	3.5	7.0	3.7			
CGA9 (CC2220)	4.5	8.0	5.6			



9. INSIDE STRUCTURE AND MATERIAL



No.	NAME	MATERIAL			
NO.	INAIVIE	Class1	Class2		
1	Dielectric	CaZrO ₃	BaTiO ₃		
2	Electrode	Nickel (Ni)			
3		Copper (Cu)			
4	Termination	Nickel (Ni)			
5		Tin (Sn)			

10. RECOMMENDATION

It is recommended to provide a slit (about 1mm wide) in the board under the components to improve washing Flux. And please make sure to dry detergent up completely before.

11. SOLDERING CONDITION

Reflow soldering only.



12. Caution

	Oddilon				
No.	Process	Condition			
1	Operating Condition (Storage,	1-1. Storage1) The capacitors must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The products should be used within 6 months upon receipt.			
	Transportation) 2) The capacitors must be operated and stored in an environment free of condensation and these gases such as Hydrogen Sulphide, Hydrogen Chlorine, Ammonia and sulfur.				
		3) Avoid storing in sun light and falling of dew.			
		4) Do not use capacitors under high humidity and high and low atmospheric pressure which may affect capacitors reliability.			
		5) Capacitors should be tested for the solderability when they are stored for long time.			
		1-2. Handling in transportation			
		In case of the transportation of the capacitors, the performance of the capacitors may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 Handling in transportation)			
2	Circuit design	2-1. Operating temperature			
		Operating temperature should be followed strictly within this specification, especially be careful with maximum temperature.			
		Do not use capacitors above the maximum allowable operating temperature.			
		2) Surface temperature including self heating should be below maximum operating temperature.			
		(Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at			
		high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product mounted on. Please design the circuit so that the maximum			
		temperature of the capacitors including the self heating to be below the maximum			
		allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C)			
		The electrical characteristics of the capacitors will vary depending on the			
		temperature. The capacitors should be selected and designed in taking the			
		temperature into consideration. 2-2. Operating voltage			
		1) Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V _{0-P} must be below the rated voltage.			
		AC or pulse with overshooting, V_{P-P} must be below the rated voltage. (1) and (2)			
		When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitors within rated voltage containing these Irregular voltage.			
		Voltage (1) DC voltage (2) DC+AC voltage (3) AC voltage			
		Positional L. L. L. L. L. L. L. L.			
		Measurement $ V_{0-P} $			
		(Rated voltage) 0 0 0			
		Voltage (4) Pulse voltage (A) (5) Pulse voltage (B)			
		Positional Neasurement V _{P-P}			
		Measurement (Rated voltage)			

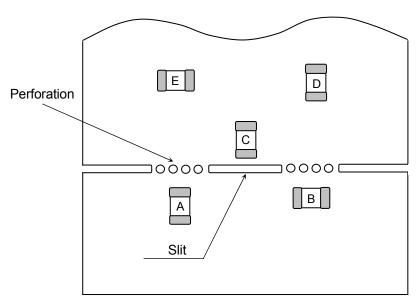


No.	Process			Con	dition			
2	Circuit design A Caution				itive high frequ	uency AC or p	oulse is applied,	
	<u> </u>	The capacit	3) The effective capacitance will vary depending on applied DC and AC voltages The capacitors should be selected and designed in taking the voltages into consideration.					
		When the	2-3. Frequency When the capacitors (Class 2) are used in AC and/or pulse voltages, the capacitors may vibrate themselves and generate audible sound.					
3	Designing P.C.board	The amount of solder at the terminations has a direct effect on the reliability of the capacitors. 1) The greater the amount of solder, the higher the stress on the chip capacitors, and the more likely that it will break. When designing a P.C.board, determine the shape and size of the solder lands to have proper amount of solder on the terminations. 2) Avoid using common solder land for multiple terminations and provide individual solder land for each terminations. 3) Size and recommended land dimensions.						
			\xrightarrow{B} \xrightarrow{A}					
		Reflow sole	dering				(mm)	
		Type Symbol	CGA5 (CC1206)	CGA6 (CC1210)	CGA7 (CC1808)	CGA8 (CC1812)	CGA9 (CC2220)	
		A	2.0 - 2.4	2.0 - 2.4	3.1 - 3.7	3.1 - 3.7	4.1 - 4.8	
		В	1.0 - 1.2	1.0 - 1.2	1.2 - 1.4	1.2 - 1.4	1.2 - 1.4	
		С	1.1 - 1.6	1.9 - 2.5	1.5 - 2.0	2.4 - 3.2	4.0 - 5.0	
		D	1.0 - 1.3	1.0 - 1.3	1.0 - 1.3	1.0 - 1.3	1.0 - 1.3	
		componen completely It is recom	nts to improve before.	ovide a slit (at washing flux. se low activate ch Rosin due t	And please m	ake sure to dr	d under the ry detergent up	

No.	Process		Condition				
3	Designing P.C.board	5) Recommended	Recommended chip capacitors layout is as following.				
			Disadvantage against bending stress	Advantage against bending stress			
		Mounting face	Perforation or slit	Perforation or slit			
			Break P.C.board with mounted side up.	Break P.C.board with mounted side down.			
			Mount perpendicularly to perforation or slit	Mount in parallel with perforation or slit			
		Chip arrangement (Direction)	Perforation or slit	Perforation or slit			
		Distance from slit	Closer to slit is higher stress $ \begin{pmatrix} \ell_1 \\ \ell_2 \end{pmatrix} $	Away from slit is less stress			

No. Process Condition

3 Designing P.C.board 6) Mechanical stress varies according to location of chip capacitors on the P.C.board.



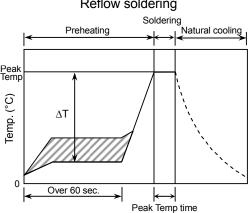
The stress in capacitors is in the following order. A > B = C > D > E

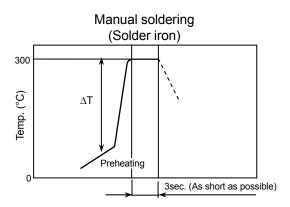
7) Layout recommendation

Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD
Need to avoid	Lead wire Chip Solder PCB Adhesive Solder land	Chassis Excessive solder	Solder land Excessive solder Missing solder Solder land
Recommen- dation	Solder resist	Solder resist $\ell^2 > \ell^1$	Solder resist

No.	Process		Condition				
4	Mounting	 4-1. Stress from mounting head If the mounting head is adjusted too low, it may induce excessive stress in the chip capacitors to result in cracking. Please take following precautions. 1) Adjust the bottom dead center of the mounting head to reach on the P.C.board surface and not press it. 2) Adjust the mounting head pressure to be 1 to 3N of static weight. 3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C.board. See following examples. 					
			Not recommended	Recommended			
		Single sided mounting	Crack	Support pin			
		Double-sides mounting	Solder peeling Crack	Support pin			
		to cause crack. P	ng jaw is worn out, it may give me lease control the close up dimens preventive maintenance and repla	ion of the centering jaw and			

No.	Process	Condition
5	Soldering	5-1. Flux selection Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended following.
		It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). Strong flux is not recommended.
2) Excessive flu		Excessive flux must be avoided. Please provide proper amount of flux.
		3) When water-soluble flux is used, enough washing is necessary.
		5-2. Recommended soldering profile by various methods
		Reflow soldering





5-3. Recommended soldering peak temp and peak temp duration

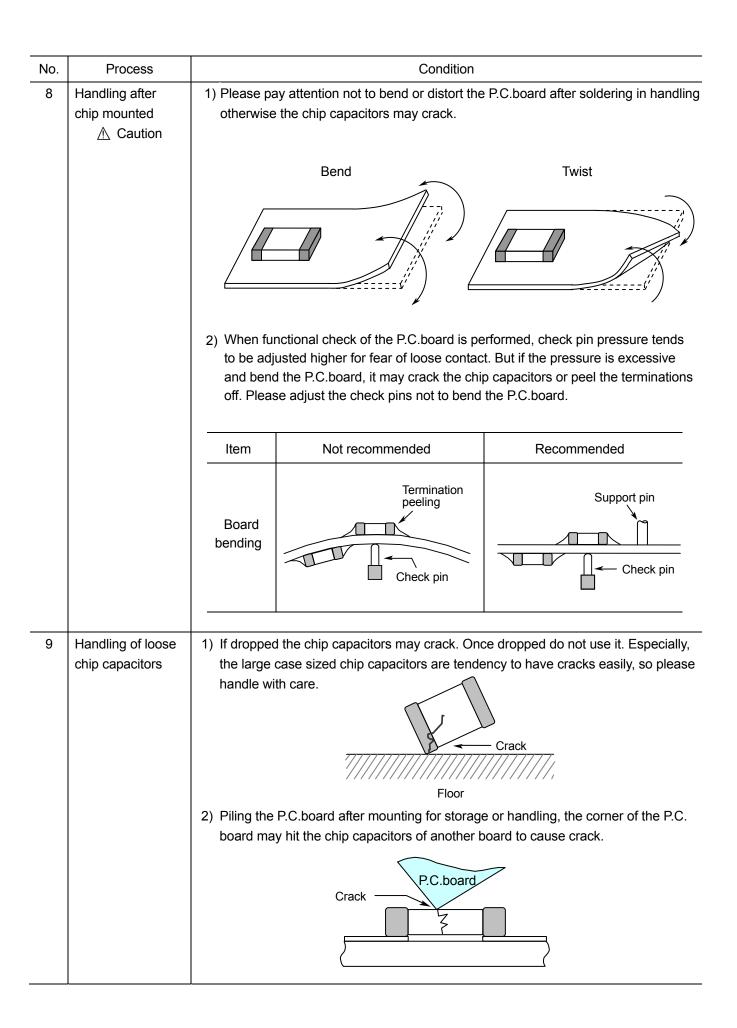
Temp./Duration	Reflow soldering			
Solder	Peak temp(°C)	Duration(sec.)		
Sn-Pb Solder	230 max.	20 max.		
Lead Free Solder	260 max.	10 max.		

Recommended solder compositions Sn-37Pb (Sn-Pb solder) Sn-3.0Ag-0.5Cu (Lead Free Solder)



No.	Process		Condi	ition			
5	Soldering	5-4. Avoiding thermal shock					
		Preheating condition	1) Preheating condition				
		Soldering	Т	уре	Temp. (°C)		
			CGA5(CC1206)		ΔT ≤ 150		
		Reflow soldering	CGA6(CC1210), CGA8(CC1812),		ΔT ≤ 130		
				ΔT ≤ 150			
		Manual soldering	CGA6(CC1210), CGA8(CC1812),		ΔT ≤ 130		
		Cooling condition Natural cooling using ai cleaning, the temperatu 5-5. Amount of solder		•	dipped into a solvent for in 100°C.		
			s and it may resu	ılt in chip cracking	n chip capacitors when g. In sufficient solder may		
		Excessive solder			her tensile force in capacitors to cause ck		
		Adequate		Maximum Minimum			
		Insufficient solder		cau chip	v robustness may se contact failure or capacitors come off P.C.board.		
		5-6. Solder repair by solder 1) Selection of the solderin Tip temperature of sold land size. The higher the heat shock may cause Please make sure the time in accordance with chip capacitors with the Recommended solder Temp. (°C)	ng iron tip der iron varies by the tip temperature a crack in the ch tip temp. before s th following recome e condition in 5-4	e, the quicker the ip capacitors. soldering and keep mended condition to avoid the thern	operation. However, of the peak temp and n. (Please preheat the nal shock.)		
		300 max.	3 max.	20 max.	Ø 3.0 max.		

No.	Process	Condition
5	Soldering	 Direct contact of the soldering iron with ceramic dielectric of chip capacitors may cause crack. Do not touch the ceramic dielectric and the terminations by solder iron. 5-7. Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder. 5-8. Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex 1 (Informative) Recommendations to prevent the tombstone phenomenon)
6	Cleaning	 If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to chip capacitors surface to deteriorate especially the insulation resistance. If cleaning condition is not suitable, it may damage the chip capacitors. Insufficient washing Terminal electrodes may corrode by Halogen in the flux. Halogen in the flux may adhere on the surface of capacitors, and lower the insulation resistance. Water soluble flux has higher tendency to have above mentioned problems (1) and (2). Excessive washing When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, following is the recommended condition.
7	Coating and molding of the P.C.board	 When the P.C.board is coated, please verify the quality influence on the product. Please verify carefully that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitors. Please verify the curing temperature.



No.	Process	Condition
10	Capacitance aging	The capacitors (Class 2) have aging in the capacitance. They may not be used in precision time constant circuit. In case of the time constant circuit, the evaluation should be done well.
11	Estimated life and estimated failure rate of capacitors	As per the estimated life and the estimated failure rate depend on the temperature and the voltage. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 (Informative) Calculation of the estimated lifetime and the estimated failure rate (Voltage acceleration coefficient: 3 multiplication rule, Temperature acceleration coefficient: 10°C rule) The failure rate can be decreased by reducing the temperature and the voltage but they will not be guaranteed.
12	Others A Caution	The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition.
		The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet. If you intend to use the products in the applications listed below or if you have special requirements exceeding the range or conditions set forth in this specification, please contact us.
		 (1) Aerospace/Aviation equipment (2) Transportation equipment (electric trains, ships, etc.) (3) Medical equipment (4) Power-generation control equipment (5) Atomic energy-related equipment (6) Seabed equipment (7) Transportation control equipment (8) Public information-processing equipment (9) Military equipment (10) Electric heating apparatus, burning equipment (11) Disaster prevention/crime prevention equipment (12) Safety equipment (13) Other applications that are not considered general-purpose applications
		When designing your equipment even for general-purpose applications, you are kindly requested to take into consideration securing protection circuit/device or providing backup circuits in your equipment.



13. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

- 1) Inspection No.
- 2) TDK P/N
- 3) Customer's P/N
- 4) Quantity

*Composition of Inspection No.

Example
$$\underline{F}$$
 $\underline{2}$ \underline{A} \underline{OO} \underline{OOO} (a) (b) (c) (d) (e)

- a) Line code
- b) Last digit of the year
- c) Month and A for January and B for February and so on. (Skip I)
- d) Inspection Date of the month.
- e) Serial No. of the day

14. Bulk packaging quantity

Total number of components in a plastic bag for bulk packaging: 1,000pcs.

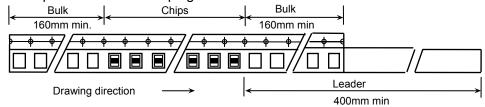
15. TAPE PACKAGING SPECIFICATION

1. CONSTRUCTION AND DIMENSION OF TAPING

1-1. Dimensions of carrier tape

Dimensions of paper tape shall be according to Appendix 2. Dimensions of plastic tape shall be according to Appendix 3, 4.

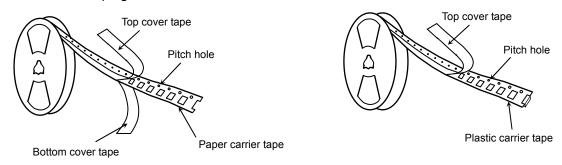
1-2. Bulk part and leader of taping



1-3. Dimensions of reel

Dimensions of Ø178 reel shall be according to Appendix 5, 6. Dimensions of Ø330 reel shall be according to Appendix 7, 8.

1-4. Structure of taping



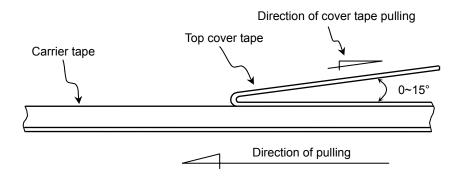
2. CHIP QUANTITY

Tuno	Thickness	Taping	Chip quantity(pcs.)	Chip quantity(pcs.)	
Type	of chip	Material	φ178mm reel	φ330mm reel	
CGA5	CGA5 0.85 mm paper 4,000		4,000	10.000	
(CC1206)	1.30 mm	plastic	2,000	10,000	
CCA6	1.60 mm		2,000	8,000	
CGA6 (CC1210)	2.00 mm	plastic	1,000	5,000	
	2.50 mm		1,000	5,000	
CGA7 (CC1808)	0.85 mm				
	1.10 mm	plastic	1,000	5,000	
	1.30 mm				
(CC 1000)	1.60 mm				3,000
	2.00 mm			3,000	
	1.30 mm		1,000	5,000	
CGA8	1.60 mm				
(CC1812)	2.00 mm	plastic		3,000	
(001012)	2.30 mm		500	3,000	
	2.50 mm		300		
CGA9	1.60 mm		1,000		
(CC2220)	2.00 mm	plastic	500	3,000	
(002220)	2.50 mm		300		

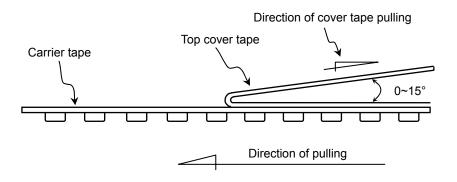
3. PERFORMANCE SPECIFICATIONS

3-1. Fixing peeling strength (top tape)0.05-0.7N. (See the following figure.)

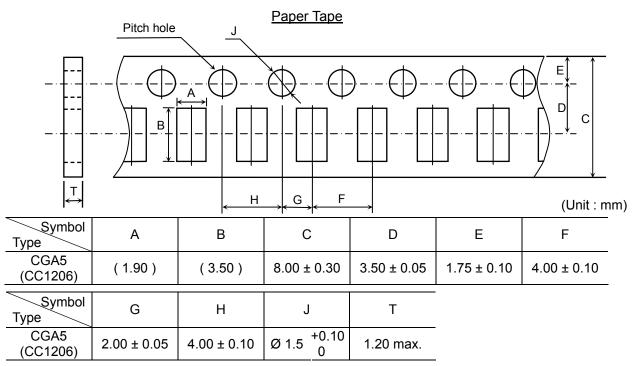
TYPE 1 (Paper)



TYPE 2 (Plastic)

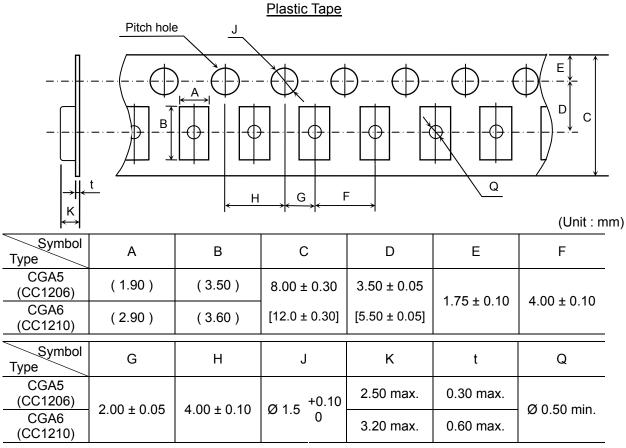


- 3-2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.
- 3-3. The missing of components shall be less than 0.1%
- 3-4. Components shall not stick to fixing tape.
- 3-5. The fixing tapes shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.



^{*} The values in the parentheses () are for reference.

Appendix 3

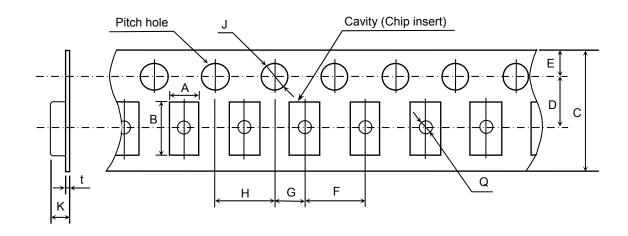


^{*} The values in the parentheses () are for reference.

^{*} As for 2.5mm thickness products, apply values in the brackets [].



Plastic Tape

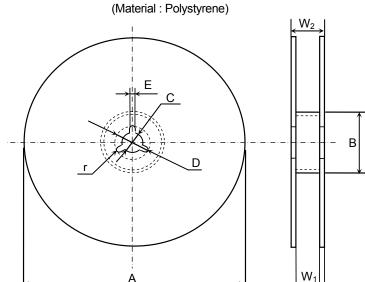


(Unit:mm)

						-
Symbol Type	Α	В	С	D	E	F
CGA7 (CC1808)	(2.50)	(5.10)				
CGA8 (CC1812)	(3.60)	(4.90)	12.0 ± 0.30	5.50 ± 0.05	1.75 ± 0.10	8.00 ± 0.10
CGA9 (CC2220)	(5.40)	(6.10)				
Symbol Type	G	Н	J	К	t	Q
CGA7 (CC1808)						
CGA8 (CC1812)	2.00 ± 0.05	4.00 ± 0.10	Ø 1.5 ^{+0.10}	6.50 max.	0.60 max.	Ø 1.50 min.
CGA9 (CC2220)						

^{*} The values in the parentheses () are for reference.

CGA5, CGA6 (As for CGA6 type, any thickness of the item except 2.5mm)



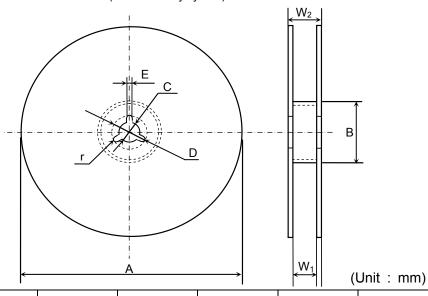
 Symbol
 A
 B
 C
 D
 E
 W_1

 Dimension
 Ø178 ± 2.0
 Ø60 ± 2.0
 Ø13 ± 0.5
 Ø21 ± 0.8
 2.0 ± 0.5 9.0 ± 0.3

Symbol	W_2	r	
Dimension	13.0 ± 1.4	1.0	

Appendix 6

CGA6, CGA7, CGA8, CGA9 (As for CGA6 type, applied to 2.5mm thickness products)
(Material: Polystyrene)

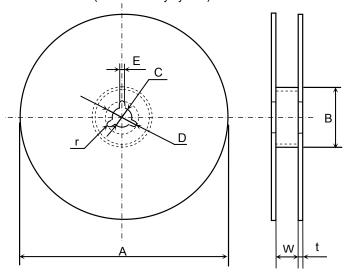


Symbol	А	В	С	D	E	W ₁
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	13.0 ± 0.3

Symbol	W_2	r
Dimension	17.0 ± 1.4	1.0

CGA5, CGA6 $\,$ (As for CGA6 type, any thickness of the item except 2.5mm)

(Material : Polystyrene)



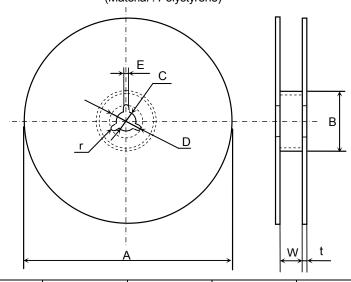
(Unit: mm)

Symbol	Α	В	С	D	Е	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	10.0 ± 1.5

Symbol	t	r	
Dimension	2.0 ± 0.5	1.0	

Appendix 8

CGA6, CGA7, CGA8, CGA9 (As for CGA6 type, applied to 2.5mm thickness products) (Material : Polystyrene)



(Unit: mm)

Symbol	Α	В	С	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	14.0 ± 1.5

Symbol	t	r
Dimension	2.0 ± 0.5	1.0