

**CY7C374**

## UltraLogic™ 128-Macrocell Flash CPLD

### Features

- 128 macrocells in eight logic blocks
- 64 I/O pins
- 6 dedicated inputs including 4 clock pins
- No hidden delays
- High speed
  - $f_{MAX} = 100 \text{ MHz}$
  - $t_{PD} = 12 \text{ ns}$
  - $t_S = 7 \text{ ns}$
  - $t_{CO} = 7 \text{ ns}$
- Electrically Alterable Flash technology
- Available in 84-pin PLCC, 84-pin CLCC, 100-pin TQFP, and 84-pin PGA packages
- Pin compatible with the CY7C373

### Functional Description

The CY7C374 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370t family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C374 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

The 128 macrocells in the CY7C374 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C374 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 64 I/O pins on the CY7C374. In addition, there are two dedicated inputs and four input/clock pins.

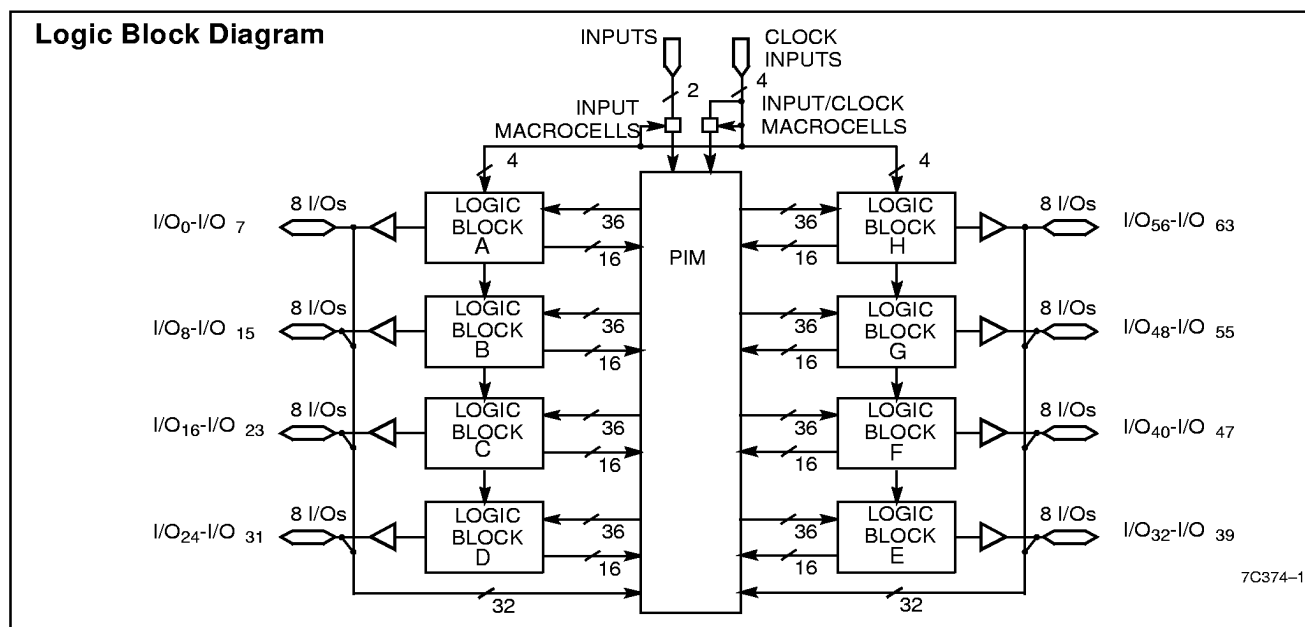
Finally, the CY7C374 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C374 remain the same.

### Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C374 includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

### Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.



## Selection Guide

		7C374-100	7C374-83	7C374-66	7C374L-66
Maximum Propagation Delay $t_{PD}$ (ns)		12	15	20	20
Minimum Set-Up, $t_S$ (ns)		6	8	10	10
Maximum Clock to Output, $t_{CO}$ (ns)		7	8	10	10
Maximum Supply Current, $I_{CC}$ (mA)	Commercial	300	300	300	150
	Military/Industrial		370	370	

Shaded area contains preliminary information.

## Functional Description (continued)

### Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 CPLDs. Note that product term allocation is handled by software and is invisible to the user.

### I/O Macrocell

Half of the macrocells on the CY7C374 have I/O pins associated with them. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The I/O macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

### Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

### Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C374 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM.

There is no speed penalty incurred by signals traversing the PIM.

### Development Tools

Development software for the CY7C374 is available from Cypress's *Warp2™* and *Warp3™* software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™ CUPL™, and LOG/iC™. Please refer to third-party tool support data sheets for further information.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -0.5V to +7.0V

DC Program Voltage ..... 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

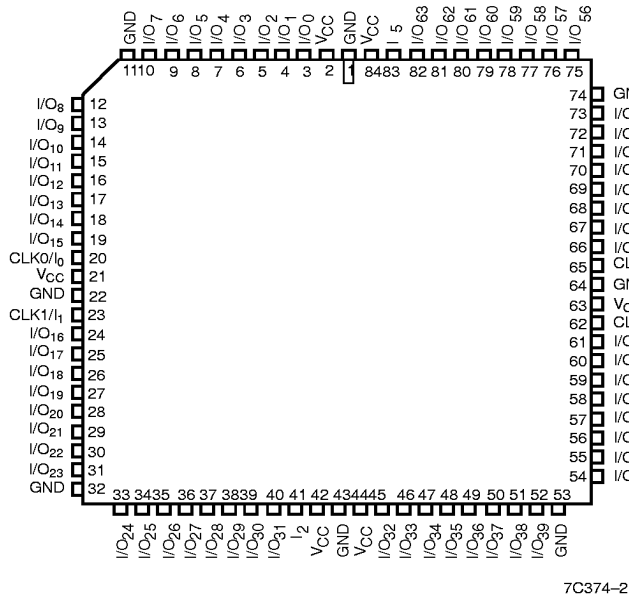
Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 5%
Industrial	-40°C to +85°C	5V ± 5%
Military <sup>[1]</sup>	-55°C to +125°C	5V ± 10%

### Notes:

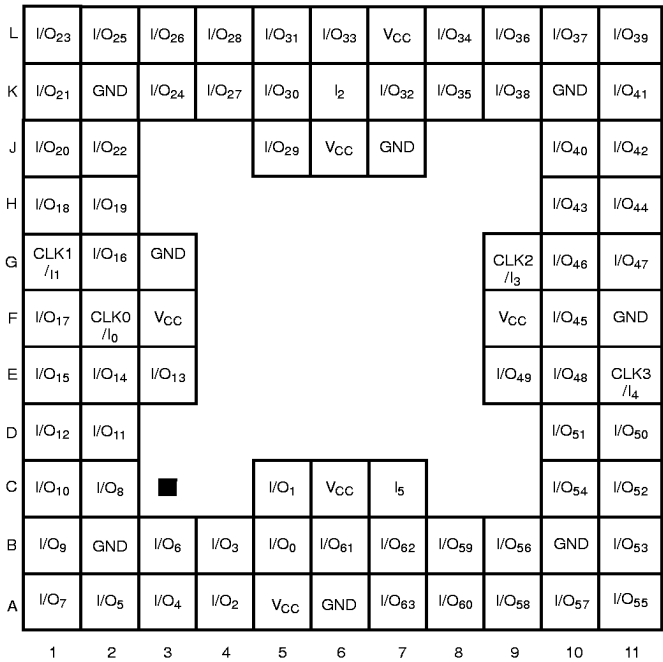
1.  $T_A$  is the "instant on" case temperature.

## Pin Configurations

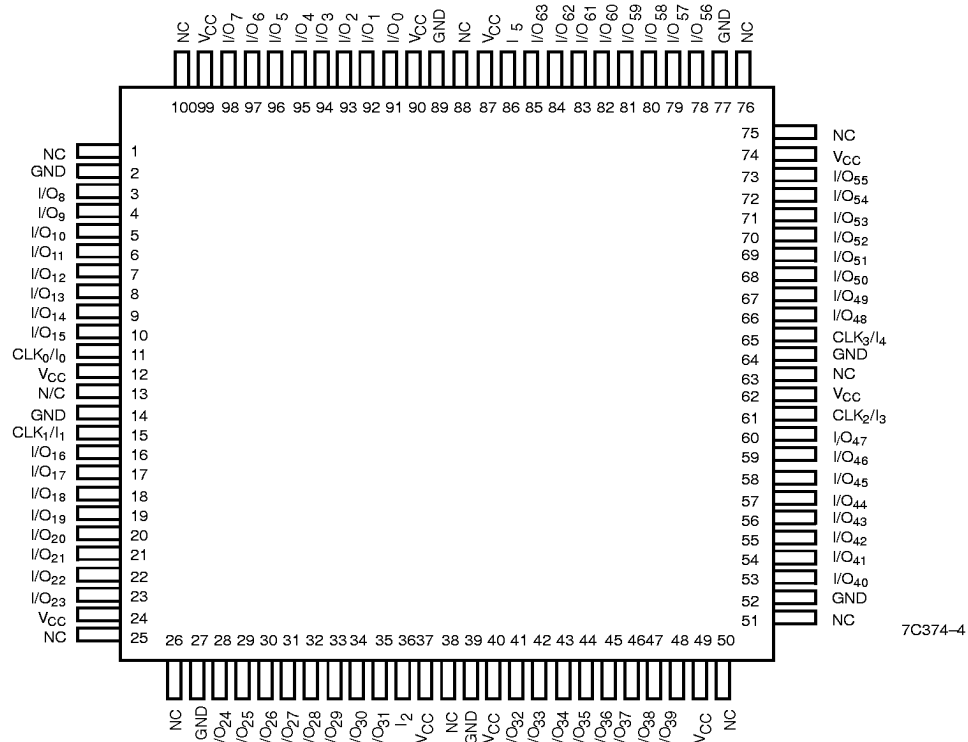
PLCC/CLCC  
Top View



PGA  
Bottom View



TQFP  
Top View



**Electrical Characteristics** Over the Operating Range<sup>[2]</sup>

Parameter	Description	Test Conditions		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min.	I <sub>OH</sub> = -3.2 mA (Com'l/Ind)	2.4		V
			I <sub>OH</sub> = -2.0 mA (Mil)			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min.	I <sub>OL</sub> = 16 mA (Com'l/Ind)		0.5	V
			I <sub>OL</sub> = 12 mA (Mil)			V
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs <sup>[3]</sup>		2.0	7.0	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs <sup>[3]</sup>		-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	V <sub>I</sub> = Internal GND, V <sub>I</sub> = V <sub>CC</sub>		-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	V <sub>O</sub> = Internal GND, V <sub>O</sub> = V <sub>CC</sub>		-50	+50	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4, 5]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V		-30	-160	mA
I <sub>CC</sub>	Power Supply Current <sup>[6]</sup>	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA f = 1 MHz, V <sub>IN</sub> = GND, V <sub>CC</sub>	Com'l		300	mA
			Com'l "L" -66		150	mA
			Mil./Ind.		370	mA

Shaded area contains preliminary information.

**Capacitance**<sup>[5]</sup>

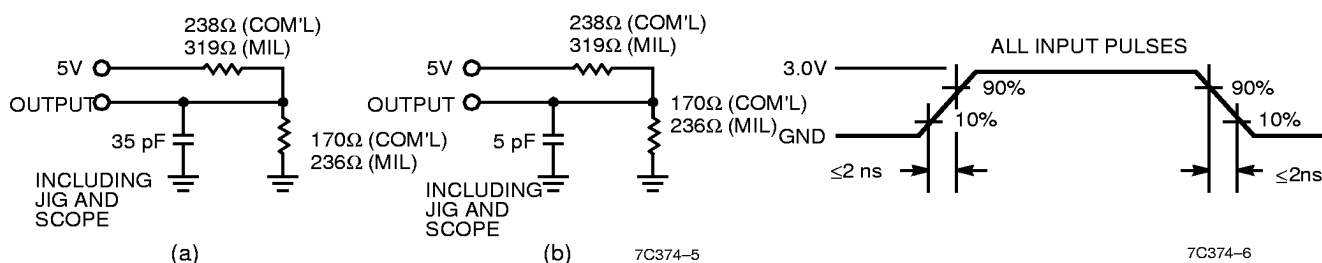
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 5.0V at f = 1 MHz	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 5.0V at f = 1 MHz	12	pF

**Endurance Characteristics**<sup>[5]</sup>

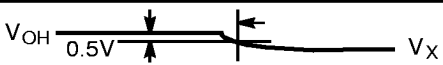

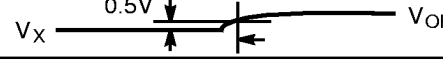
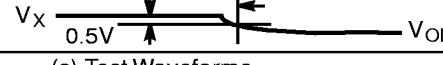
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

**Notes:**

- See the last page of this specification for Group A subgroup testing information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Measured with 16-bit counter programmed into each logic block.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  
 99Ω (COM'L)  
 136Ω (MIL) 2.08V (COM'L)  
 OUTPUT 2.13V (MIL)

Parameter <sup>[7]</sup>	V <sub>X</sub>	Output Waveform Measurement Level
t <sub>ER</sub> (-)	1.5V	
t <sub>ER</sub> (+)	2.6V	
t <sub>EA</sub> (+)	1.5V	
t <sub>EA</sub> (-)	V <sub>thc</sub>	

(c) Test Waveforms

### Switching Characteristics Over the Operating Range<sup>[8]</sup>

Parameter	Description	7C374-100		7C374-83		7C374-66		Unit
		7C374-100		7C374-83		7C374L-66		
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t <sub>PD</sub>	Input to Combinatorial Output		12		15		20	ns
t <sub>PDL</sub>	Input to Output Through Transparent Input or Output Latch		15		18		22	ns
t <sub>PDLL</sub>	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t <sub>EA</sub>	Input to Output Enable		16		19		24	ns
t <sub>ER</sub>	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t <sub>WL</sub>	Clock or Latch Enable Input LOW Time <sup>[5]</sup>	3		4		5		ns
t <sub>WH</sub>	Clock or Latch Enable Input HIGH Time <sup>[5]</sup>	3		4		5		ns
t <sub>IS</sub>	Input Register or Latch Set-Up Time	2		3		4		ns
t <sub>IH</sub>	Input Register or Latch Hold Time	2		3		4		ns
t <sub>ICO</sub>	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t <sub>ICOL</sub>	Input Register Clock or Latch Enable to Output Through Trans- parent Output Latch		18		21		26	ns
Output Registered/Latched Mode Parameters								
t <sub>CO</sub>	Clock or Latch Enable to Output		7		8		10	ns
t <sub>S</sub>	Set-Up Time from Input to Clock or Latch Enable	6		8		10		ns
t <sub>H</sub>	Register or Latch Data Hold Time	0		0		0		ns
t <sub>CO2</sub>	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t <sub>SCS</sub>	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t <sub>SL</sub>	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t <sub>HL</sub>	Hold Time for Input Through Transparent Latch from Output Reg- ister Clock or Latch Enable	0		0		0		ns
f <sub>MAX1</sub>	Maximum Frequency with Internal Feedback (Least of 1/t <sub>SCS</sub> , 1/(t <sub>S</sub> + t <sub>H</sub> ), or 1/t <sub>CO</sub> ) <sup>[5]</sup>	100		83		66		MHz

**Notes:**

7. t<sub>ER</sub> is measured with 5-pF AC Test Load and t<sub>EA</sub> is measured with 35-pF AC Test Load.
8. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.

**Switching Characteristics** Over the Operating Range<sup>[8]</sup> (continued)

Parameter	Description	7C374-100		7C374-83		7C374-66		Unit
		7C374-100		7C374-83		7C374L-66		
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>MAX2</sub>	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t <sub>WL</sub> + t <sub>WH</sub> ), 1/(t <sub>S</sub> + t <sub>H</sub> ), or 1/t <sub>CO</sub> )	143		125		100		MHz
f <sub>MAX3</sub>	Maximum Frequency with External Feedback (Lesser of 1/(t <sub>CO</sub> + t <sub>S</sub> ) and 1/(t <sub>WL</sub> + t <sub>WH</sub> ))	76.9		67.5		50		MHz
t <sub>OH</sub> -t <sub>IH</sub> 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x <sup>[5, 9]</sup>	0		0		0		ns
Pipelined Mode Parameters								
t <sub>ICS</sub>	Input Register Clock to Output Register Clock	10		12		15		ns
f <sub>MAX4</sub>	Maximum Frequency in Pipelined Mode (Least of 1/(t <sub>CO</sub> + t <sub>S</sub> ), 1/t <sub>ICS</sub> , 1/(t <sub>WL</sub> + t <sub>WH</sub> ), 1/(t <sub>IS</sub> + t <sub>IH</sub> ), or 1/t <sub>SCS</sub> )	100		83.3		66.6		MHz
Reset/Preset Parameters								
t <sub>RW</sub>	Asynchronous Reset Width <sup>[5]</sup>	12		15		20		ns
t <sub>RR</sub>	Asynchronous Reset Recovery Time <sup>[5]</sup>	14		17		22		ns
t <sub>RO</sub>	Asynchronous Reset to Output		18		21		26	ns
t <sub>PW</sub>	Asynchronous Preset Width <sup>[5]</sup>	12		15		20		ns
t <sub>PR</sub>	Asynchronous Preset Recovery Time <sup>[5]</sup>	14		17		22		ns
t <sub>PO</sub>	Asynchronous Preset to Output		18		21		26	ns
t <sub>POR</sub>	Power-On Reset <sup>[5]</sup>		1		1		1	μs

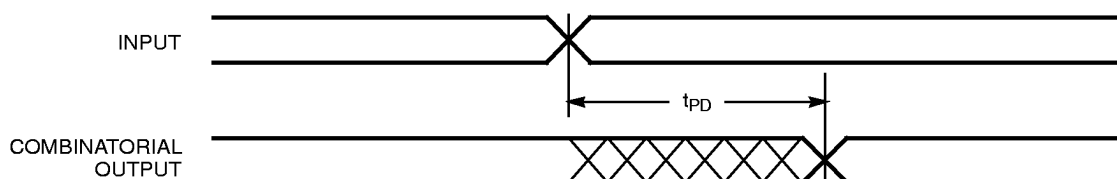
Shaded area contains preliminary information

**Notes:**

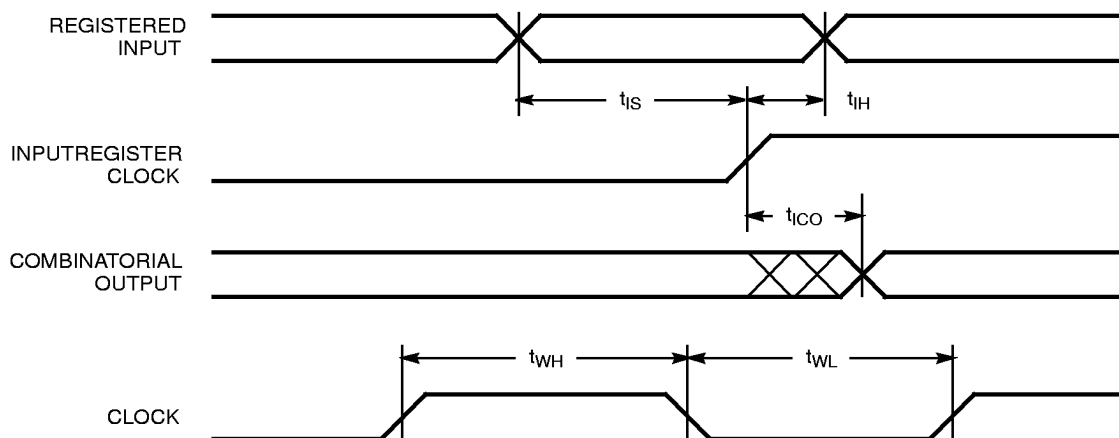
9. This specification is intended to guarantee interface compatibility of the other members of the CY7C370 family with the CY7C374. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

**Switching Waveforms**

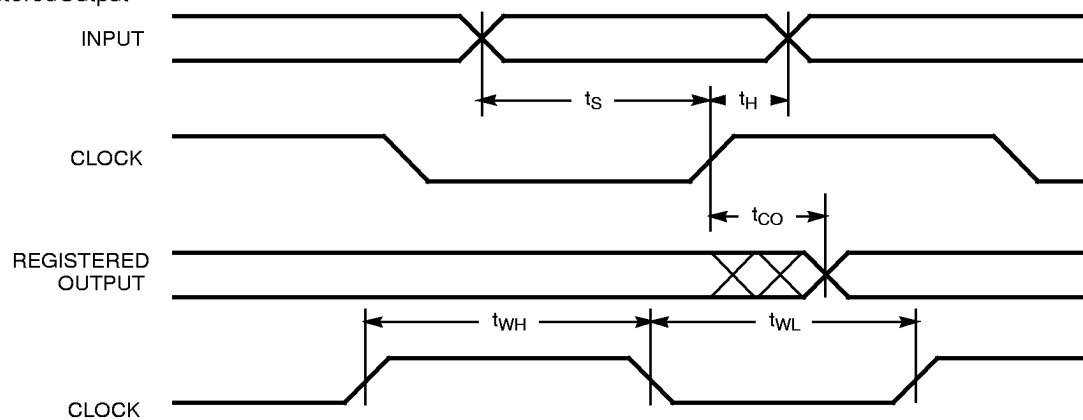
CombinatorialOutput



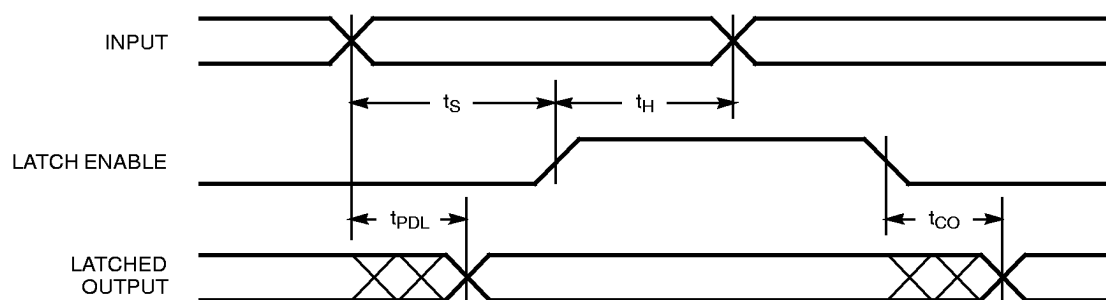
7C374-7

**Switching Waveforms (continued)**
**Registered Input**


7C374-8

**Registered Output**


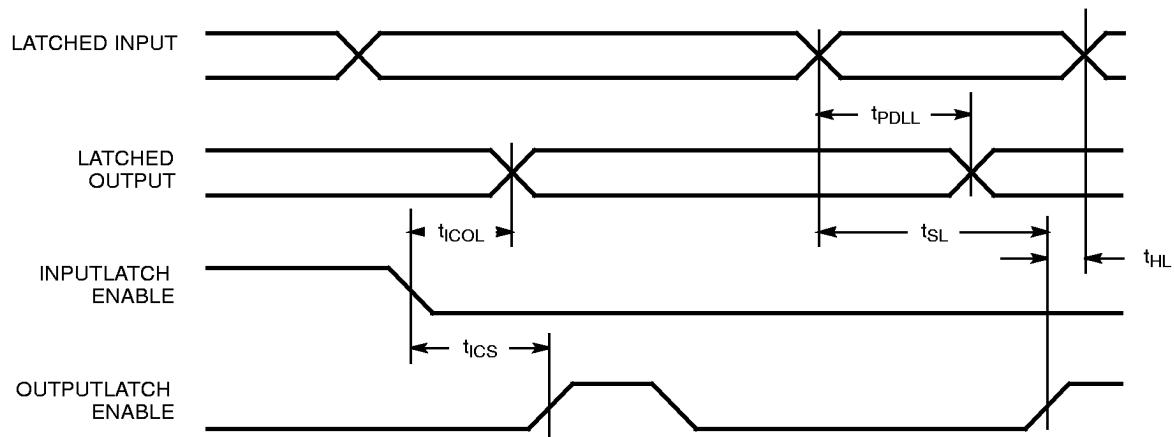
7C374-9

**Latched Output**


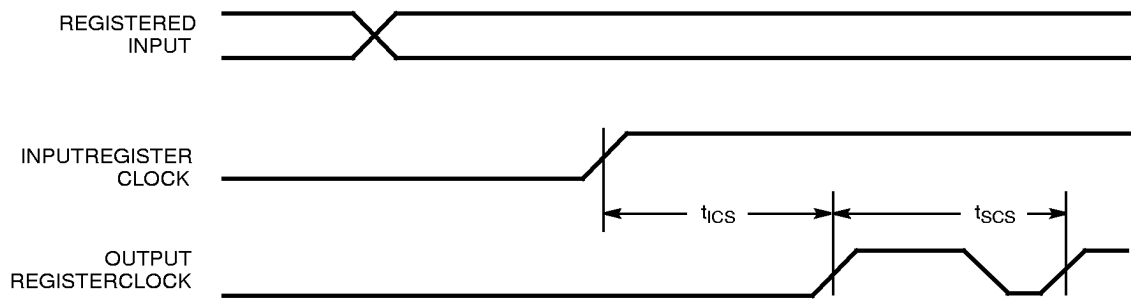
7C374-10

## Switching Waveforms (continued)

### Latched Input and Output

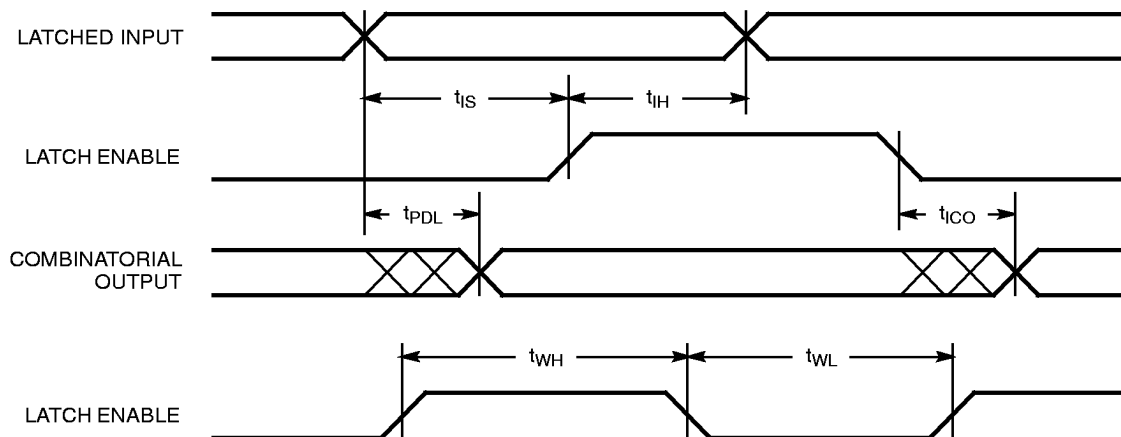


### Clock to Clock



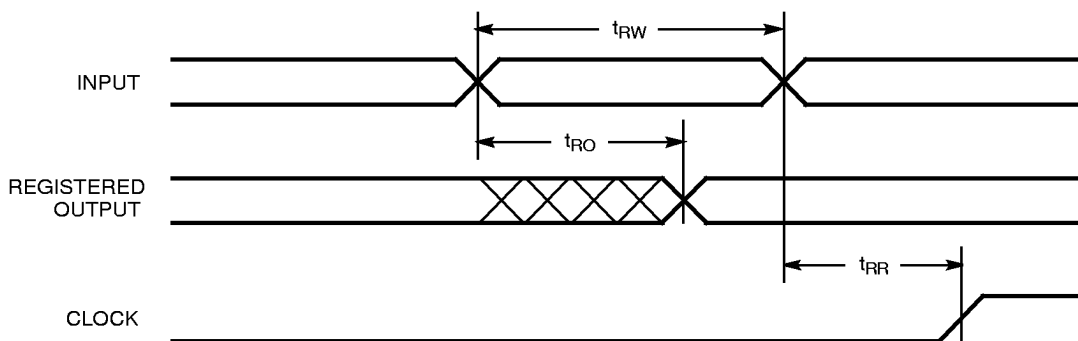
7C374-12

### Latched Input

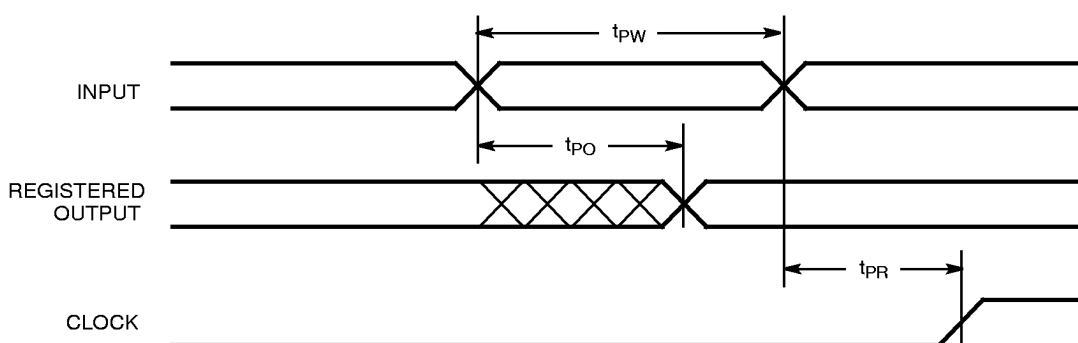


7C374-13

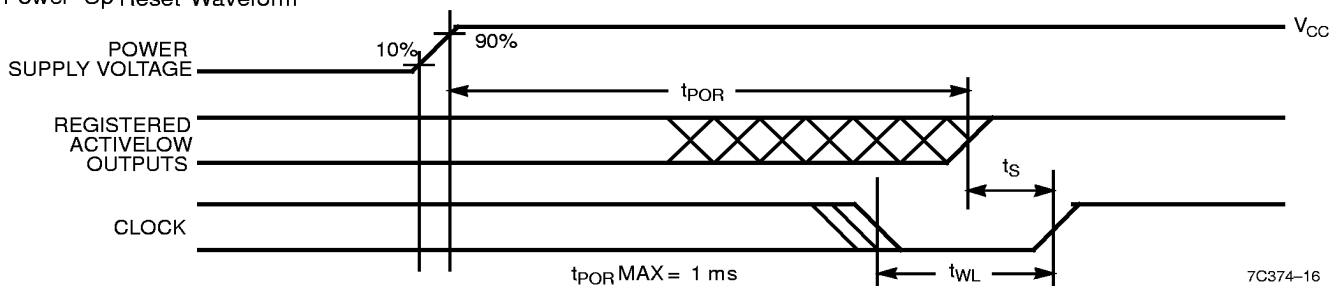


**Switching Waveforms (continued)**
**Asynchronous Reset**


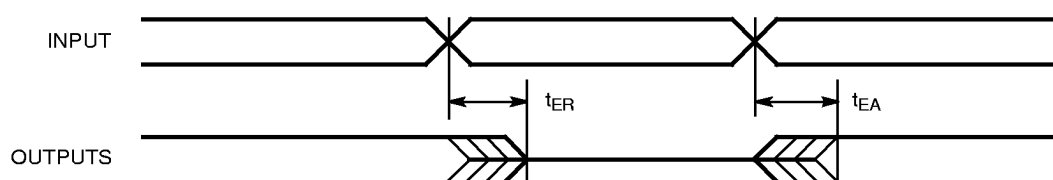
7C374-14

**Asynchronous Preset**


7C374-15

**Power-Up Reset Waveform**


7C374-16

**Output Enable/Disable**


7C374-17

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C374-100AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374-100GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C374-100JC	J83	84-Lead Plastic Leaded Chip Carrier	
83	CY7C374-83AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374-83GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C374-83JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374-83AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374-83JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374-83GMB	G84	84-Pin Grid Array (Cavity Up)	Military
	CY7C374-83YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
66	CY7C374-66AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374-66GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C374-66JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374-66AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374-66JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374-66GMB	G84	84-Pin Grid Array (Cavity Up)	Military
	CY7C374-66YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
	CY7C374L-66AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374L-66JC	J83	84-Lead Plastic Leaded Chip Carrier	

**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**
**DC Characteristics**

Parameter	Subgroups
$V_{OH}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{IH}$	1, 2, 3
$V_{IL}$	1, 2, 3
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{CC1}$	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
$t_{PD}$	9, 10, 11
$t_{PDL}$	9, 10, 11
$t_{PDLL}$	9, 10, 11
$t_{CO}$	9, 10, 11
$t_{ICO}$	9, 10, 11
$t_{ICOL}$	9, 10, 11
$t_S$	9, 10, 11
$t_{SL}$	9, 10, 11
$t_H$	9, 10, 11
$t_{HL}$	9, 10, 11
$t_{IS}$	9, 10, 11
$t_{IH}$	9, 10, 11
$t_{ICS}$	9, 10, 11
$t_{EA}$	9, 10, 11
$t_{ER}$	9, 10, 11

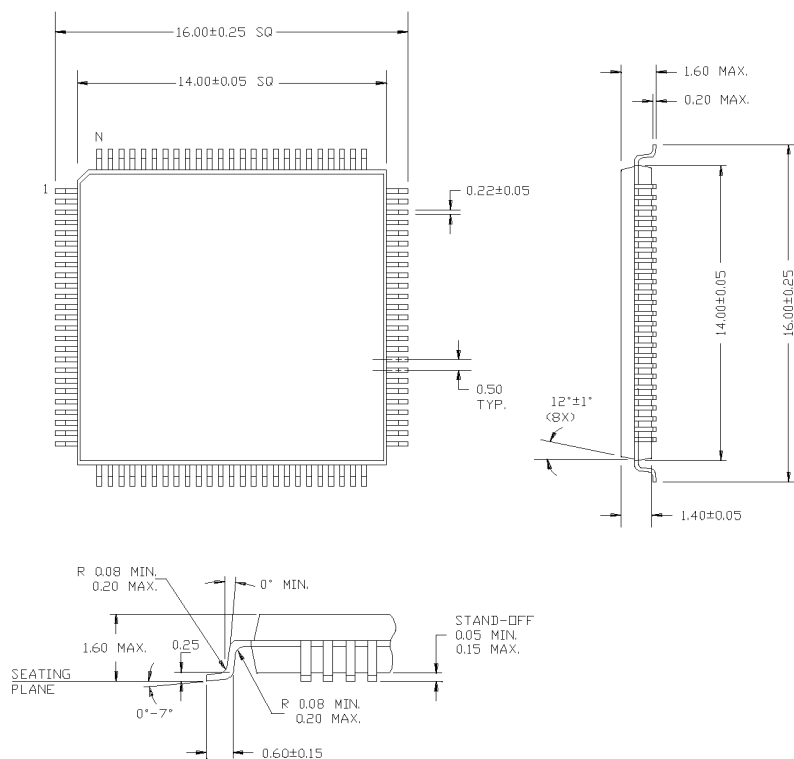
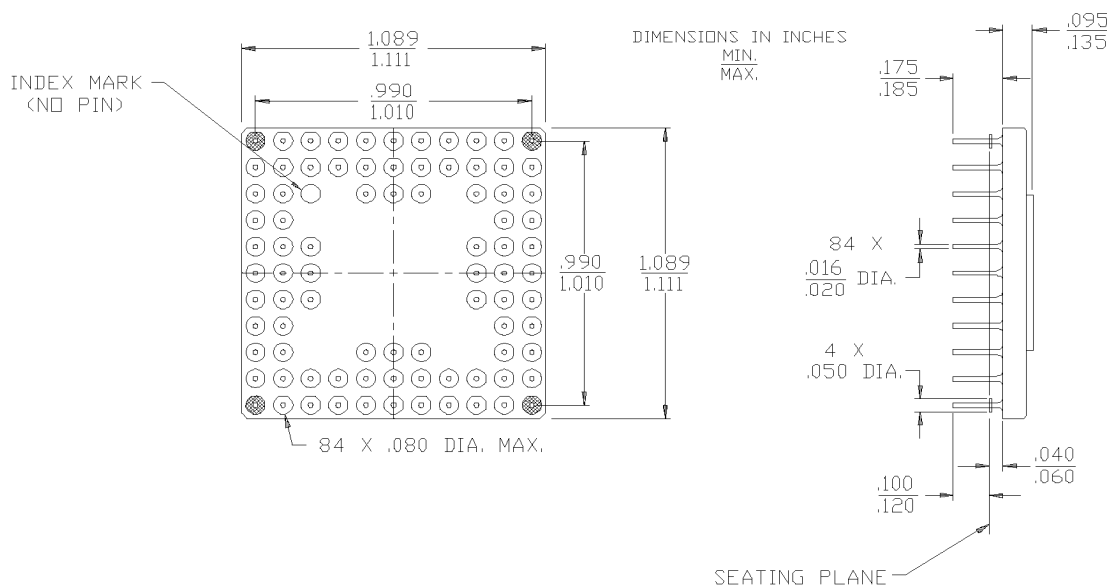
Document #: 38-00214-E

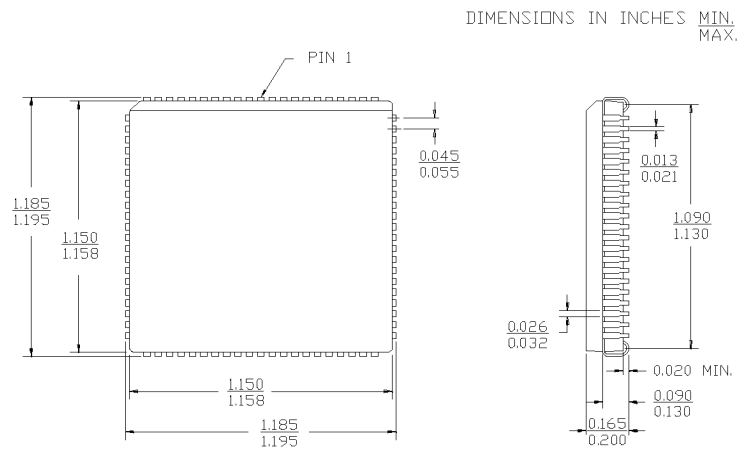
UltraLogic, FLASH370, *Warp2*, and *Warp3* are trademarks of Cypress Semiconductor Corporation.

ABEL is a trademark of Data I/O Corporation.

CUPL is a trademark of Logical Devices Incorporated.

LOG/IC is a trademark of Isdata Corporation.

**Package Diagrams**
**100-Pin Thin Quad Flat Pack A100**

**84-Pin Grid Array (Cavity Up) G84**


**Package Diagrams (continued)**
**84-Lead Plastic Leaded Chip Carrier J83**

**84-pin Ceramic Leaded Chip Carrier Y84**
