

# 2.5 V or 3.3 V 200 MHz 1:15 Clock Distribution Buffer

### **Features**

- 2.5 V or 3.3 V operation
- 200-MHz clock support
- LVPECL or LVCMOS/LVTTL clock input
- LVCMOS/LVTTL compatible outputs
- 15 clock outputs: drive up to 30 clock lines
- 1X and 1/2X configurable outputs
- Output three-state control
- 350 ps maximum output-to-output skew
- Pin compatible with MPC949, MPC9449
- Available in Industrial temperature range
- 52-pin TQFP package

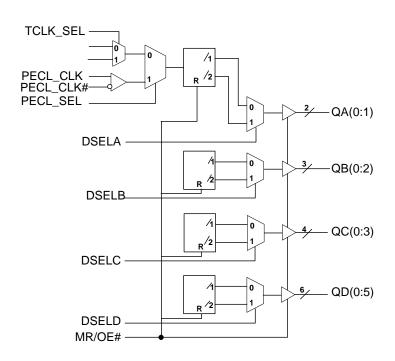
## **Description**

The CY29949 is a low voltage 200 MHz clock distribution buffer with the capability to select either a differential LVPECL or LVCMOS/LVTTL compatible input clocks. These clock sources are used to provide for test clocks and primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 15 outputs are LVCMOS or LVTTL compatible and can drive  $50\Omega$  series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:30.

The CY29949 is capable of generating 1X and 1/2X signals from a 1X source. These signals are generated and retimed internally to ensure minimal skew between the 1X and 1/2X signals. SEL(A:D) inputs allow flexibility in selecting the ratio of 1X to1/2X outputs.

The CY29949 outputs can also be three-stated via the MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

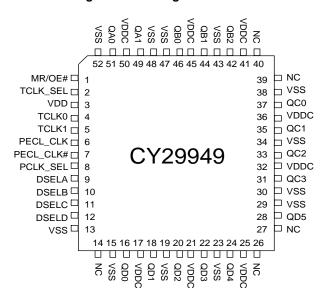
## **Logic Block Diagram**





## **Pin Configuration**

Figure 1. Pin Diagram - CY29949



## **Pin Description**

Pin	Name	PWR	<b>I/O</b> <sup>[1]</sup>	Description
6	PECL_CLK		I, PD	PECL Input Clock
7	PECL_CLK#		I, PU	PECL Input Clock
4, 5	TCLK(0,1)		I, PU	External Reference/Test Clock Input
49, 51	QA(1,0)	VDDC	0	Clock Outputs
42, 44, 46	QB(2:0)	VDDC	0	Clock Outputs
31, 33, 35, 37	QC(3:0)	VDDC	0	Clock Outputs
16, 18, 20, 22, 24, 28	QD(5:0)	VDDC	0	Clock Outputs
9, 10, 11, 12	DSEL(A:D)		I, PD	<b>Divider Select Inputs.</b> When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
2	TCLK_SEL		I, PD	TCLK Select Input. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
8	PCLK_SEL		I, PD	PECL Select Input. When HIGH, PECL clock is selected and when LOW TCLK(0,1) is selected
1	MR/OE#		I, PD	Output Enable Input. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated. If more than one bank is used in /2 mode, a reset must be performed (MR/OE# asserted high) after power up to ensure that all internal flip-flops are set to the same state.
17, 21, 25, 32, 36, 41, 45, 50	VDDC			2.5 V or 3.3 V Power Supply for Output Clock Buffers
3	VDD			2.5 V or 3.3 V Power Supply
13, 15, 19, 23, 29, 30, 34, 38, 43, 47, 48, 52	VSS			Common Ground
14, 26, 27, 39, 40,	NC			Not Connected

#### Note

<sup>1.</sup> PD = internal pull-down, PU = internal pull-up.



## **Maximum Ratings**<sup>[2]</sup>

Maximum Input Voltage Relative to $V_{SS}$ : $V_{SS} - 0.3$	V
Maximum Input Voltage Relative to $V_{DD}$ : $V_{DD}$ + 0.3	٧
Storage Temperature:65°C to + 150°	С
Operating Temperature:40°C to +85°	С
Maximum ESD Protection	V
Maximum Power Supply:5.5	٧
Maximum Input Current: ±20 m	Α

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions must be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>SS</sub> or V<sub>DD</sub>).

## **DC Parameters** (V<sub>DD</sub> = V<sub>DDC</sub> = 3.3 V ±10% or 2.5 V ±5%, over the specified temperature range)

Parameter	Description	Conditions	Min	Тур	Max	Unit
$V_{IL}$	Input Low Voltage	V <sub>DD</sub> = 3.3 V, PECL_CLK single ended	1.49	-	1.825	V
		V <sub>DD</sub> = 2.5 V, PECL_CLK single ended	1.10	1	1.45	
		All other inputs	V <sub>SS</sub>	1	0.8	
V <sub>IH</sub>	Input High Voltage	V <sub>DD</sub> = 3.3 V, PECL_CLK single ended	2.135	-	2.42	V
		V <sub>DD</sub> = 2.5 V, PECL_CLK single ended	1.75	-	2.0	
		All other inputs	2.0	-	$V_{DD}$	
I <sub>IL</sub>	Input Low Current <sup>[3]</sup>		_	-	-100	μΑ
I <sub>IH</sub>	Input High Current <sup>[3]</sup>		_	-	100	
V <sub>PP</sub>	Peak-to-Peak Input Voltage PECL_CLK		300	-	1000	mV
$V_{CMR}$	Common Mode Range <sup>[4]</sup>	V <sub>DD</sub> = 3.3 V	V <sub>DD</sub> – 2.0	_	V <sub>DD</sub> – 0.6	V
	PECL_CLK	V <sub>DD</sub> = 2.5 V	V <sub>DD</sub> – 1.2	1	V <sub>DD</sub> – 0.6	
$V_{OL}$	Output Low Voltage <sup>[5]</sup>	I <sub>OL</sub> = 20 mA	_	-	0.4	V
V <sub>OH</sub>	Output High Voltage <sup>[5]</sup>	$I_{OH} = -20 \text{ mA}, V_{DD} = 3.3 \text{ V}$	2.5	-	-	V
		$I_{OH} = -20 \text{ mA}, V_{DD} = 2.5 \text{ V}$	1.8		-	
$I_{DDQ}$	Quiescent Supply Current		-	5	7	mA
I <sub>DD</sub>	Dynamic Supply Current	V <sub>DD</sub> = 3.3 V, Outputs at 100 MHz, CL = 30 pF	-	200	_	mA
		V <sub>DD</sub> = 3.3 V, Outputs at 160 MHz, CL = 30 pF	-	330	_	
		V <sub>DD</sub> = 2.5 V, Outputs at 100 MHz, CL = 30 pF	-	140	_	
		V <sub>DD</sub> = 2.5 V, Outputs at 160 MHz, CL = 30 pF	-	235	_	
Zout	Output Impedance	V <sub>DD</sub> = 3.3 V	12	15	18	Ω
		V <sub>DD</sub> = 2.5 V	14	18	22	
C <sub>in</sub>	Input Capacitance		_	4	_	pF

- 2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
- Inputs have pull-up/pull-down resistors that effect input current.
   The V<sub>CMR</sub> is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V<sub>CMR</sub> range and the input lies within the V<sub>PP</sub> specification.
   Driving series or parallel terminated 50Ω (or 50Ω to V<sub>DD</sub>/2) transmission lines.



$AOI$ arameter 3 ( $VDD = VDDC = 3.3 \text{ V} \pm 10\% \text{ or } 2.3 \text{ V} \pm 3\%$ , over the specimed temperature range).	<b>AC Parameters</b>	$(V_{DD} = V_{DDC} = 3.3 \text{ V} \pm 10\% \text{ or } 2.5 \text{ V} \pm 5\%, \text{ over the spec}$	ified temperature range)[6
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Parameter	Description	Conditions	Min	Тур	Max	Unit
Fmax	Input Frequency <sup>[7]</sup>	V <sub>DD</sub> = 3.3 V	-	-	200	MHz
		V <sub>DD</sub> = 2.5 V	_	_	170	
Tpd	PECL_CLK to Q Delay <sup>[7]</sup>	V <sub>DD</sub> = 3.3 V	4.0	_	8.6	ns
	TCLK to Q Delay <sup>[7]</sup>	- 	4.2	_	10.5	
	PECL_CLK to Q Delay <sup>[7]</sup>	V <sub>DD</sub> = 2.5 V	6.0	_	10.6	
	TCLK to Q Delay <sup>[7]</sup>	- 	6.2	_	10.5	
FoutDC	Output Duty Cycle <sup>[7, 8]</sup>	Measured at VDD/2	45	_	55	%
tpZL, tpZH	Output Enable Time (all outputs)		2	-	10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2	_	10	ns
Tskew	Output-to-Output Skew <sup>[7, 9]</sup>		-	250	350	ps
Tskew(pp)	Part-to-Part Skew <sup>[10]</sup>	PECL_CLK to Q	_	1.5	2.75	ns
		TCLK to Q	_	2.0	4.0	
Tr/Tf	Output Clocks Rise/Fall Time <sup>[9]</sup>	0.8 V to 2.0 V, V <sub>DD</sub> = 3.3 V	0.10	-	1.0	ns
		0.6 V to 1.8 V, V <sub>DD</sub> = 2.5 V	0.10	-	1.3	

Figure 2. LVCMOS\_CLK CY29949 Test Reference for  $V_{CC}$  = 3.3 V and  $V_{CC}$  = 2.5 V

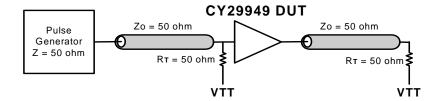
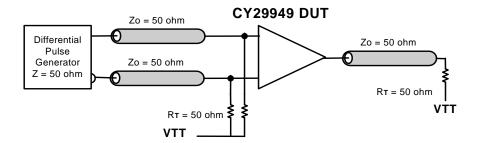


Figure 3. PECL\_CLK CY29949 Test Reference for  $V_{CC}$  = 3.3 V and  $V_{CC}$  = 2.5 V



- Notes
  Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
  Outputs driving 50Ω transmission lines.
  50% input duty cycle.
  See Figure 2 and Figure 3.
  Part-to-part skew at a given temperature and voltage.



Figure 4. Propagation Delay (TPD) Test Reference

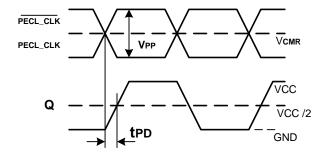


Figure 5. LVCMOS Propagation Delay (TPD) Test Reference

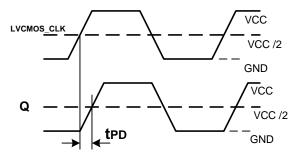


Figure 6. Output Duty Cycle (FoutDC)

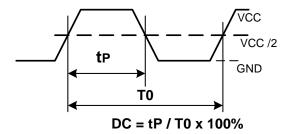
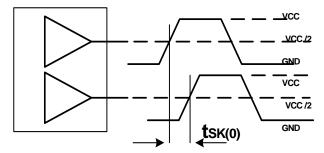


Figure 7. Output-to-Output Skew tsk(0)

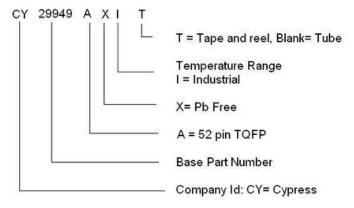




## **Ordering Information**

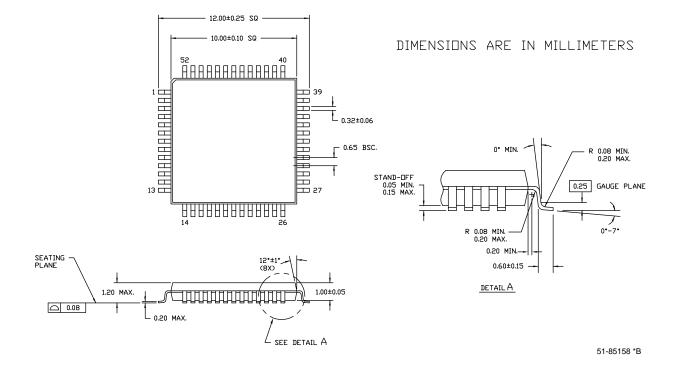
Part Number	Package Type	Production Flow
CY29949AXI	52-Pin TQFP	Industrial, -40°C to +85°C
CY29949AXIT	52-Pin TQFP - Tape and Reel	Industrial, -40°C to +85°C

## **Ordering Code Definitions**



## **Package Drawing and Dimensions**

Figure 8. 52-Pin Thin Plastic Quad Flat Pack (10 x 10 x 1.0 mm) A52B





## **Acronyms**

Table 1. Acronyms Used in this Document

Acronym	Description
LVTTL	low voltage transistor-transistor logic
LVPECL	low voltage pseudo (positive) emitter coupled logic
LVCMOS	low voltage CMOS logic

## **Document Conventions**

## **Units of Measure**

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kv	kiloVolt
MHZ	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt



## **Document History Page**

Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	111100	02/01/02	BRK	New data sheet
*A	116783	08/14/02	HWT	Added commercial temperature range to the Ordering Information table
*B	118463	09/09/02	HWT	Corrected the package diagram from 52 LQFP to 52 TQFP
*C	122881	12/22/02	RBI	Added power-up requirements to Maximum Ratings
*D	130132	11/07/03	RGL	Fixed block diagram and MR/OE# description in the Pin Description table
*E	2595534	10/23/08	CXQ/PYRS	Changed to Pb-Free device code in Ordering Information
*F	3420718	10/24/11	PURU	Removed Commercial Information. Updated template according to current Cypress standards.

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