# CY26121

# PacketClock™ Spread Spectrum Clock Generator

## Features

- Integrated phase-locked loop (PLL)
- Low jitter, high-accuracy outputs
- 3.3V operation
- 25-MHz input frequency
- 66.66-MHz or 33.33-MHz selectable output frequency (orig, -3,-11,-31)
- 33.33-MHz or 25-MHz selectable output frequency (-2,-21)

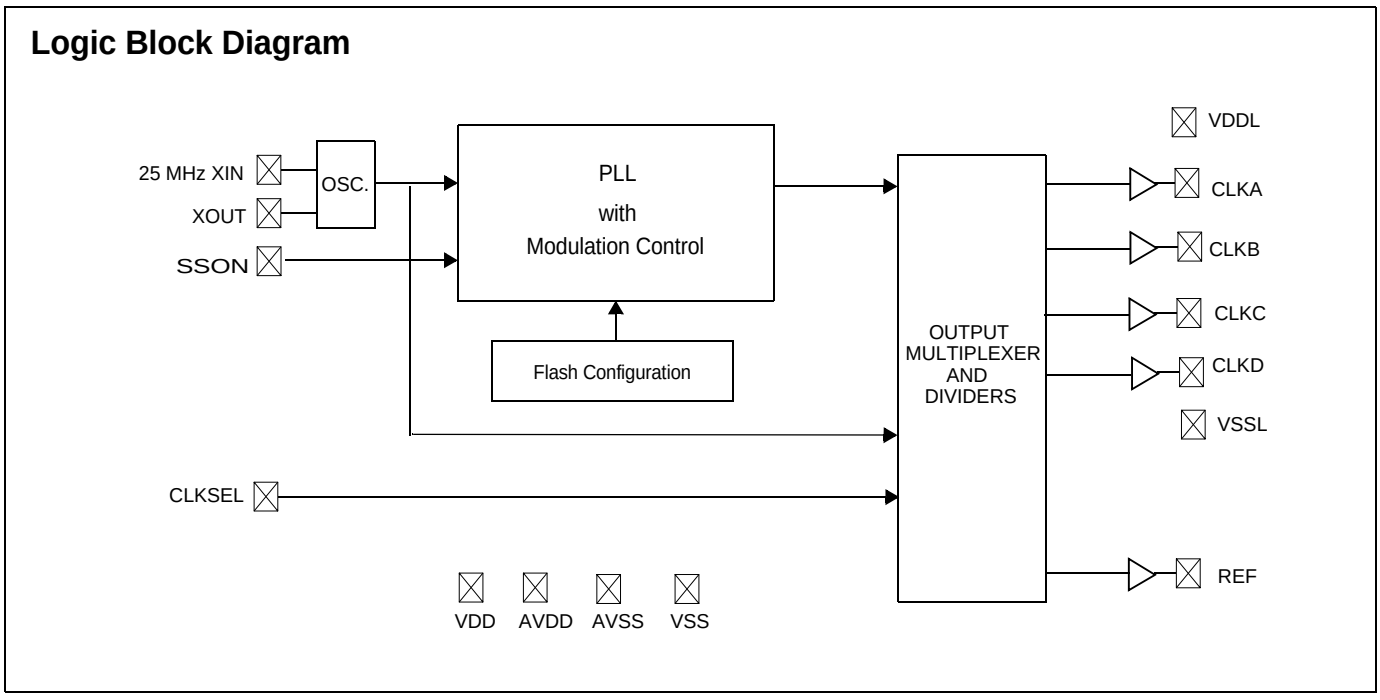
## Benefits

- High-performance PLL tailored for Spread Spectrum application
- Meets critical timing requirements in complex system designs
- Enables application compatibility
- Works with commonly available crystal or driven reference
- Downspread Spread Spectrum with 30-kHz nominal modulation frequency

**Table 1. Frequency Table for CLKA-D**

| Part Number | CLKSEL=0 | CLKSEL=1 | Spread% | Parallel Crystal Load |
|---|---|---|---|---|
| CY26121 | 66.66 MHz | 33.33 | –2.8% | 6 pF |
| CY26121-2 | 33.33 MHz | 25.00 | –2.8% | 6 pF |
| CY26121-3 | 66.66 MHz | 33.33 | –1.4% | 6 pF |
| CY26121-11 | 66.66 MHz | 33.33 | –2.8% | 15 pF |
| CY26121-21 | 33.33 MHz | 25.00 | –2.8% | 15 pF |
| CY26121-31 | 66.66 MHz | 33.33 | –1.4% | 15 pF |

## Logic Block Diagram



## Pin Configuration

**Figure 1. CY26121, 16-pin TSSOP**

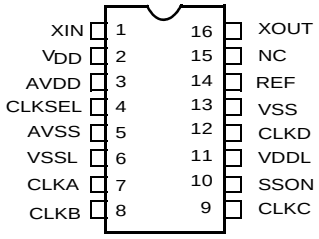



**Table 2. Pin Definitions**

| Name | Pin Number | Description |
|---|---|---|
| XIN | 1 | Reference input Or Crystal Input |
| VDD | 2 | 3.3V Voltage Supply |
| AVDD | 3 | 3.3V Analog Voltage |
| CLKSEL | 4 (orig., -11,-3,-31) | 0 = 66.66MHz out, 1 = 33.33 MHz Out. Weak pull up. |
| CLKSEL | 4 (-2, -21) | 0 = 33.33MHz out, 1 = 25 MHz Out. Weak pull up. |
| AVSS | 5 | Analog Ground |
| VSSL | 6 | CLK Ground |
| CLK(A:D) | 7,8,9,12 | Clock Outputs at $V_{DDL}$ level |
| SSON | 10 | Spread Spectrum Enable pin 0 = SS off; 1 = SS on. Weak pull up. |
| VDDL | 11 | 3.3V Clock Voltage Supply |
| VSS | 13 | Ground |
| REF | 14 | Reference Output at $V_{DD}$ Level |
| NC | 15 | No Connect |
| XOUT[1] | 16 | Crystal Output |

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Supply Voltage ($V_{DD}$, $AV_{DD}$, $V_{DDL}$) ..... –0.5 to +7.0V

DC Input Voltage ..... –0.5V to $V_{DD}$ + 0.5

Storage Temperature (Non-condensing) ..... –55°C to +125°C

Junction Temperature ..... –40°C to +125°C

Data Retention at Tj = 125°C ..... > 10 years

Package Power Dissipation ..... 350 mW

Static Discharge Voltage ..... ≥ 2000V (per MIL-STD-883, Method 3015)

## Recommended Operating Conditions

| Parameter | Description | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$, $AV_{DD}$ | Supply voltage | 3.135 | 3.30 | 3.465 | V |
| $V_{DDL}$ | Supply voltage for CLK (A-D) | 3.135 | 3.30 | 3.465 | V |
| $T_A$ | Ambient temperature (commercial temp. grade) | 0 | | 70 | ° C |
| $T_A$ | Ambient Temperature (industrial temp grade) | -40 | | 85 | ° C |
| $C_{LOAD}$ | Max. output load capacitance | | | 15 | pF |
| $F_{ref}$ | Reference frequency | | 25 | | MHz |

## Crystal Specification[2]

| Parameter | Name | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $CR_{load}$ | Crystal load capacitance (original, -2, -3) | | 6 | | pF |
| $CR_{load}$ | Crystal load capacitance (-11,-21,-31) | | 15 | | pF |
| ESR | Equivalent series resistance | | | 50 | Ω |

## DC Electrical Specifications

| Parameter | Description | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OH}$ | Output High Current | $V_{OH} = V_{DD} – 0.5$, $V_{DD}/V_{DDL}$=3.3V | 12 | 24 | | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.5, $V_{DD}/V_{DDL}$ = 3.3V | 12 | 24 | | mA |
| $I_{IH}$ | Input High Current | $V_{IH} = V_{DD}$ | | 5 | 10 | µA |
| $I_{IL}$ | Input Low Current | $V_{IL}$ = 0V | | | 50 | µA |
| $V_{IH}$ | Input High Voltage | CMOS levels | 0.7 | | | $V_{DD}$ |
| $V_{IL}$ | Input Low Voltage | CMOS levels | | | 0.3 | $V_{DD}$ |
| $C_{IN}$[3] | Input Capacitance | Input pins excluding XIN | | | 7 | pF |
| $R_{UP}$[3] | Pull up resistor on input pins | $V_{DD}$ = 3.14 to 3.47V, measured at $V_{IN}$ = 0V | 80 | 100 | 150 | kΩ |
| $I_{DD}$ | Supply Current | $AV_{DD}/V_{DD}/V_{DDL}$ Current. | | 42 | 60 | mA |

**Notes**
1. Float XOUT if XIN is externally driven.
2. A fundamental parallel resonant crystal must be used

## AC Electrical Specifications [3]

| Parameter | Description | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| DC | Output Duty Cycle | Duty Cycle is defined in Figure 2, 50% of $V_{DD}$ | 45 | 50 | 55 | % |
| ER | Rising Edge Rate | Output Clock Edge Rate, Measured from 20% to 80% of $V_{DD}$, $C_{LOAD}$ = 15 pF See Figure 3. | 0.8 | 1.4 | | V/ns |
| EF | Falling Edge Rate | Output Clock Edge Rate, Measured from 80% to 20% of $V_{DD}$, $C_{LOAD}$ = 15 pF See Figure 3. | 0.8 | 1.4 | | V/ns |
| tj | RMS Clock Cycle-to-Cycle Jitter | RMS cycle-to-cycle jitter with Spread on. Measured at $V_{DD}/2$. | | 15 | 40 | ps |

## Voltage and Timing Definitions

**Figure 2. Duty Cycle Definition**

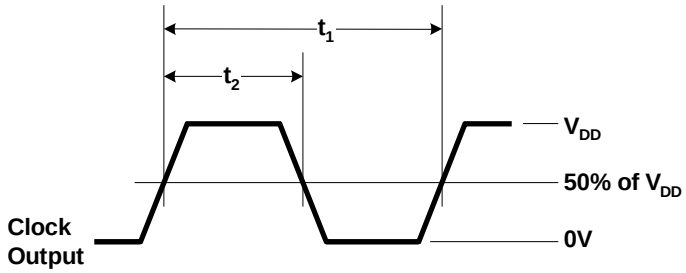
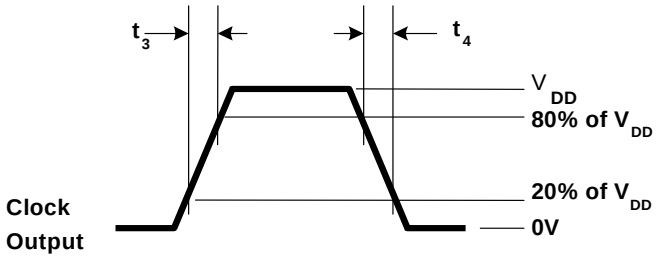



**Figure 3. ER = (0.6 x $V_{DD}$) /t3, EF = (0.6 x $V_{DD}$) /t4**




**Note**
3. Guaranteed by Characterization, not 100% tested.

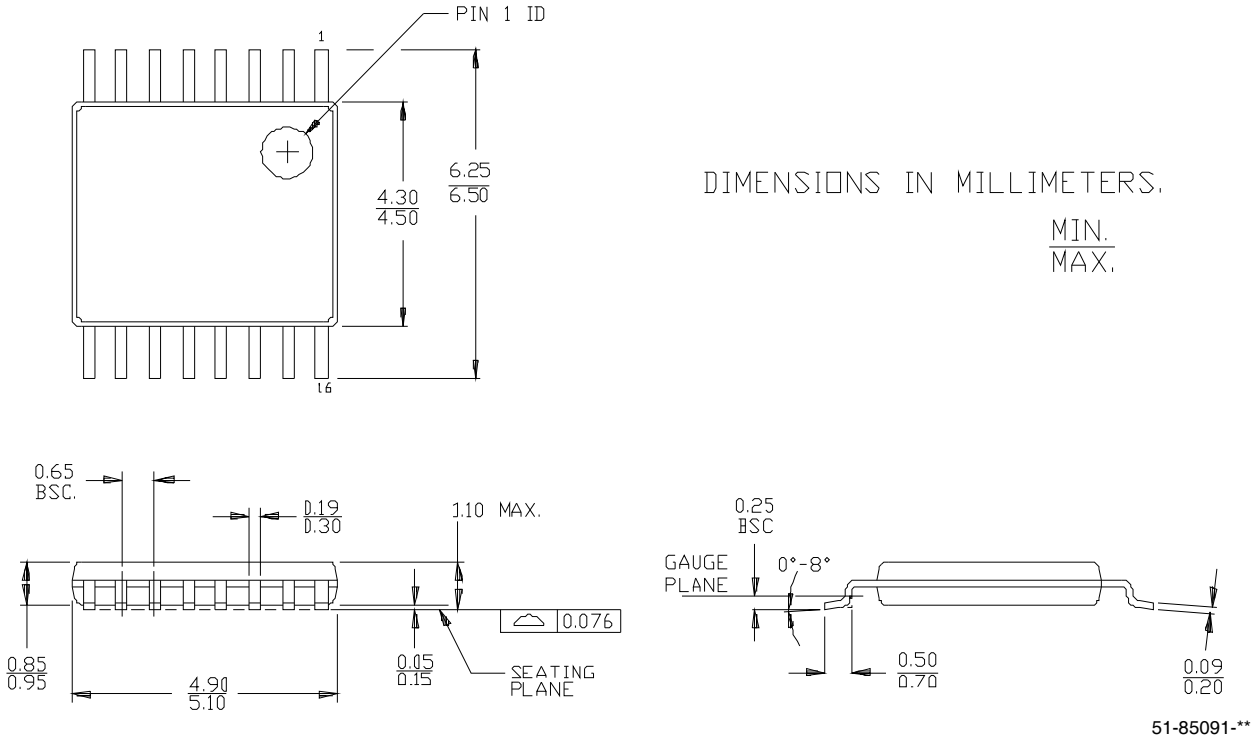
## Ordering Information

| Ordering Code | Package Type | Operating Range |
|---|---|---|
| CY26121ZC[4] | 16-pin TSSOP | Commercial, 0°C to 70°C |
| CY26121ZCT[4] | 16-pin TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY26121ZI[4] | 16-pin TSSOP | Industrial, –40°C to 85°C |
| CY26121ZIT[4] | 16-pin TSSOP – Tape and Reel | Industrial, –40°C to 85°C |
| CY26121ZC-2[4] | 16-pin TSSOP | Commercial, 0°C to 70°C |
| CY26121ZC-2T[4] | 16-pin TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY26121ZI-2[4] | 16-pin TSSOP | Industrial, –40°C to 85°C |
| CY26121ZI-2T[4] | 16-pin TSSOP – Tape and Reel | Industrial, –40°C to 85°C |
| CY26121ZC-3[4] | 16-pin TSSOP | Commercial, 0°C to 70°C |
| CY26121ZC-3T[4] | 16-pin TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY26121ZI-3[4] | 16-pin TSSOP | Industrial, –40°C to 85°C |
| CY26121ZI-3T[4] | 16-pin TSSOP – Tape and Reel | Industrial, –40°C to 85°C |
| CY26121ZC-11[4] | 16-pin TSSOP | Commercial, 0°C to 70°C |
| CY26121ZC-11T[4] | 16-pin TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY26121ZC-21[4] | 16-pin TSSOP | Commercial, 0°C to 70°C |
| CY26121ZC-21T[4] | 16-pin TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY26121ZI-21[4] | 16-pin TSSOP | Industrial, –40°C to 85°C |
| CY26121ZI-21T[4] | 16-pin TSSOP – Tape and Reel | Industrial, –40°C to 85°C |
| CY26121ZC-31[4] | 16-pin TSSOP | Commercial, 0°C to 70°C |
| CY26121ZC-31T[4] | 16-pin TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY26121KZC-21 | 16-pin TSSOP | Commercial, 0°C to 70°C |
| CY26121KZC-21T | 16-pin TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY26121KZI-21 | 16-pin TSSOP | Industrial, –40°C to 85°C |
| CY26121KZI-21T | 16-pin TSSOP – Tape and Reel | Industrial, –40°C to 85°C |
| **Pb-Free** | | |
| CY26121ZXC-21[4] | 16-pin TSSOP | Commercial, 0°C to 70°C |
| CY26121ZXC-21T[4] | 16-pin TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY26121ZXI-21[4] | 16-pin TSSOP | Industrial, –40°C to 85°C |
| CY26121ZXI-21T[4] | 16-pin TSSOP – Tape and Reel | Industrial, –40°C to 85°C |
| CY26121KZXC-21 | 16-pin TSSOP | Commercial, 0°C to 70°C |
| CY26121KZXC-21T | 16-pin TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY26121KZXI-21 | 16-pin TSSOP | Industrial, –40°C to 85°C |
| CY26121KZXI-21T | 16-pin TSSOP – Tape and Reel | Industrial, –40°C to 85°C |

**Note**
4. Not recommended for new designs.

## Package Drawing and Dimensions

**Figure 4. 16-lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16**




| Parameter | Inches | | | Millimeters | | |
|---|---|---|---|---|---|---|
| | Min | Nom. | Max | Min | Nom. | Max. |
| A | – | – | 0.047 | – | – | 1.20 |
| $A_1$ | 0.002 | – | 0.006 | 0.05 | – | 0.15 |
| A2 | 0.031 | 0.039 | 0.041 | 0.80 | 1.00 | 1.05 |
| B | 0.007 | – | 0.012 | 0.19 | – | 0.30 |
| C | 0.004 | – | 0.008 | 0.09 | – | 0.20 |
| D | 0.193 | 0.197 | 0.201 | 4.90 | 5.00 | 5.10 |
| E | 0.169 | 0.173 | 0.177 | 4.30 | 4.40 | 4.50 |
| e | 0.026 BSC | | | 0.65 BSC | | |
| H | 0.244 | 0.252 | 0.260 | 6.20 | 6.40 | 6.60 |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| a | 0° | – | 8° | 0° | – | 8° |

## Document History Page

| Document Title: CY26121 PacketClock™ Spread Spectrum Clock Generator<br>Document Number: 38-07350 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 121669 | 02/11/03 | CKN | New Data Sheet |
| *A | 2440886 | See ECN | KVM/AESA | Updated template. Added Note “Not recommended for new designs.”<br>Added part numbers CY26121ZXC-21, CY26121ZXC-21T, CY26121ZXI-21, and CY26121ZXI-21T in ordering information table.<br>Added part numbers CY26121KZC-21, CY26121KZC-21T, CY26121KZI-21, and CY26121KZI-21T.<br>Added part numbers CY26121KZXC-21, CY26121KZXC-21T, CY26121KZXI-21, and CY26121KZXI-21T.<br>Removed part numbers CY26121ZI-11, CY26121ZI-11T, CY26121ZI-31 and CY26121ZI-31T |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

| **Products** | |
|---|---|
| PSoC | psoc.cypress.com |
| Clocks & Buffers | clocks.cypress.com |
| Wireless | wireless.cypress.com |
| Memories | memory.cypress.com |
| Image Sensors | image.cypress.com |

| **PSoC Solutions** | |
|---|---|
| General | psoc.cypress.com/solutions |
| Low Power/Low Voltage | psoc.cypress.com/low-power |
| Precision Analog | psoc.cypress.com/precision-analog |
| LCD Drive | psoc.cypress.com/lcd-drive |
| CAN 2.0b | psoc.cypress.com/can |
| USB | psoc.cypress.com/usb |