Operational Amplifiers / Comparators

Ultra Low Power CMOS Operational Amplifiers

BU7265G,BU7265SG,BU7205HFV,BU7205SHFV,BU7271G,BU7271SG, BU7245HFV,BU7245SHFV,BU7411G,BU7411SG,BU7421G,BU7421SG, BU7475HFV,BU7475SHFV

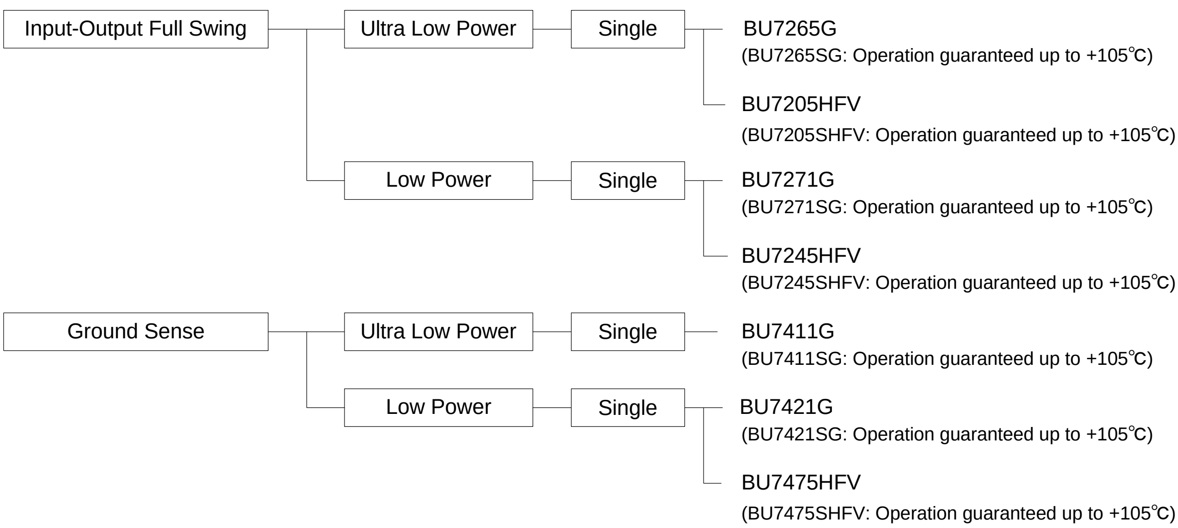
No.10049EAT19

●Description

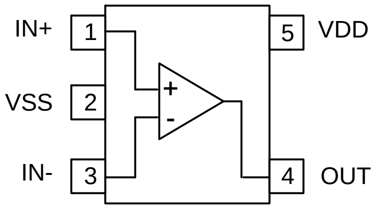
Ultra Low Power CMOS Op-Amp BU7265/BU7205/BU7271/BU7245 family (Input-Output Full Swing) and BU7411 / BU7421 / BU7475 (ground sense) are monolithic IC. Supply current is very small (BU7265/BU7411 family: 0.35[μA], BU7421 family: 8.5[μA], BU7271 family: 8.6[μA]), and VDD range is +1.6[V] ~ +5.5[V] (BU7411 family: single supply), so operable with low voltage. It's suitable for applications of portable equipments and battery movements.

●Features

1) Ultra Low Power
   0.35[μA] : BU7265 family
   : BU7411 family
   8.5[μA] : BU7421 family
   8.6[μA] : BU7271 family
2) High large signal voltage gain
3) Wide temperature range
   -40[℃] ~ +85[℃]
   (BU7265G,BU7271G,BU7411G,BU7421G)
   (BU7205HFV,BU7245HFV,BU7475HFV)
   -40[℃] ~ +105[℃]
   (BU7265SG,BU7271SG,BU7411SG,BU7421SG)
   (BU7205SHFV,BU7245SHFV,BU7475SHFV)
4) Low input bias current 1[pA] (Typ.)
5) Internal ESD protection
   Human body model (HBM) ±4000 [V] (Typ.)
6) Internal phase compensation
7) Low operating supply voltage
   +1.8[V] ~ +5.5[V] (single supply)
   (BU7265 family, BU7271 family)
   (BU7205 family, BU7245 family)
   +1.7[V] ~ +5.5[V] (single supply)
   (BU7421 family, BU7475 family)
   +1.6[V] ~ +5.5[V] (single supply)
   (BU7411 family)



●Pin Assignments



SSOP5 HVSOF5

Input type	Package		Input type	Package	
	SSOP5	HVSOF5		SSOP5	HVSOF5
Input-Output Full Swing	BU7265G BU7265SG BU7271G BU7271SG	BU7205HFV BU7205SHFV BU7245HFV BU7245SHFV	Ground Sense	BU7411G BU7411SG BU7421G BU7421SG	BU7475HFV BU7475SHFV

●Absolute Maximum Ratings(Ta=25[℃])

Parameter	Symbol	Ratings		Unit
		BU7265G, BU7411G BU7271G, BU7421G BU7205HFV, BU7245HFV BU7475HFV	BU7265SG, BU7411SG BU7271SG, BU7421SG BU7205SHFV, BU7245SHFV BU7475SHFV	
Supply Voltage	VDD-VSS	+7		V
Differential Input Voltage (*1)	Vid	VDD-VSS		V
Input Common-mode Voltage Range	Vicm	(VSS-0.3) ~ VDD+0.3		V
Operating Temperature	Topr	-40 ~ +85	-40 ~ +105	℃
Storage Temperature	Tstg	-55 ~ +125		℃
Maximum Junction Temperature	Tjmax	+125		℃

Note: Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out absolute maximum rated temperature environment may cause deterioration of characteristics.

(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input terminal voltage is set to more than VSS.

●Electrical characteristics: Input-Output Full Swing

○BU7265 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7265G, BU7265SG				
			Min.	Typ.	Max.		
Input Offset Voltage (*2)	Vio	25℃	-	1	8.5	mV	VDD=1.8 ~ 5.5[V], VOUT=VDD/2
Input Offset Current (*2)	Iio	25℃	-	1	-	pA	―
Input Bias Current (*2)	Ib	25℃	-	1	-	pA	―
Supply Current (*3)	IDD	25℃	-	0.35	0.9	μA	RL=∞, AV=0[dB], VIN=1.5[V]
		Full range	-	-	1.3		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	60	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	―
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	―
Output Source Current (*4)	IOH	25℃	1	2.4	-	mA	VDD-0.4[V]
Output Sink Current (*4)	IOL	25℃	2	4	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	2.4	-	V/ms	CL=25[pF]
Gain Band width	FT	25℃	-	4	-	kHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	60	-	°	CL=25[pF], AV=40[dB]

(*2) Absolute value
(*3) Full range BU7265: Ta=-40[℃]~+85[℃] BU7265S: Ta=-40[℃]~+105[℃]
(*4) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7271 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7271G, BU7271SG				
			Min.	Typ.	Max.		
Input Offset Voltage (*5)	Vio	25℃	-	1	8	mV	VDD=1.8 ~ 5.5[V], VOUT=VDD/2
Input Offset Current (*5)	Iio	25℃	-	1	-	pA	―
Input Bias Current (*5)	Ib	25℃	-	1	-	pA	―
Supply Current (*6)	IDD	25℃	-	8.6	17	μA	RL=∞, AV=0[dB], VIN=1.5[V]
		Full range	-	-	25		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	70	100	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	―
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	―
Output Source Current (*7)	IOH	25℃	2	4	-	mA	VDD-0.4[V]
Output Sink Current (*7)	IOL	25℃	4	8	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	50	-	V/ms	CL=25[pF]
Gain Band width	FT	25℃	-	90	-	kHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	60	-	°	CL=25[pF], AV=40[dB]

(*5) Absolute value
(*6) Full range BU7271: Ta=-40[℃]~+85[℃] BU7271S: Ta=-40[℃]~+105[℃]
(*7) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7205 family,(Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits BU7205HFV, BU7205SHFV			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*8)	Vio	25℃	-	1	9.5	mV	VDD=1.8 ~ 5.5[V], VOUT=VDD/2
Input Offset Current (*8)	Iio	25℃	-	1	-	pA	─
Input Bias Current (*8)	Ib	25℃	-	1	-	pA	─
Supply Current (*9)	IDD	25℃	-	0.4	0.95	µA	RL=∞, AV=0[dB], VIN=1.5[V]
		Full range	-	-	1.2		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	60	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	─
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	─
Output Source Current (*10)	IOH	25℃	0.5	1.2	-	mA	VDD-0.4[V]
Output Sink Current (*10)	IOL	25℃	1	2	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	2.5	-	V/ms	CL=25[pF]
Gain Band width	FT	25℃	-	2.5	-	kHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	60	-	°	CL=25[pF], AV=40[dB]

(*8) Absolute value
(*9) Full range BU7205: Ta=-40[℃]~+85[℃] BU7205S: Ta=-40[℃]~+105[℃]
(*10) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7245 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits BU7245HFV, BU7245SHFV			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*11)	Vio	25℃	-	1	8.5	mV	VDD=1.8 ~ 5.5[V], VOUT=VDD/2
Input Offset Current (*11)	Iio	25℃	-	1	-	pA	─
Input Bias Current (*11)	Ib	25℃	-	1	-	pA	─
Supply Current (*12)	IDD	25℃	-	5.0	12	µA	RL=∞, AV=0[dB], VIN=1.5[V]
		Full range	-	-	20		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	60	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	3	V	VDD-VSS=3[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	─
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	─
Output Source Current (*13)	IOH	25℃	2	4	-	mA	VDD-0.4[V]
Output Sink Current (*13)	IOL	25℃	4	8	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	35	-	V/ms	CL=25[pF]
Gain Band width	FT	25℃	-	70	-	kHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	60	-	°	CL=25[pF], AV=40[dB]

(*11) Absolute value
(*12) Full range BU7245: Ta=-40[℃]~+85[℃] BU7245S: Ta=-40[℃]~+105[℃]
(*13) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

●Electrical characteristics: Ground Sense

○BU7411 family,(Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7411G, BU7411SG				
			Min.	Typ.	Max.		
Input Offset Voltage (*14)	Vio	25℃	-	1	8	mV	VDD=1.6 ~ 5.5[V], VOUT=VDD/2
Input Offset Current (*14)	Iio	25℃	-	1	-	pA	—
Input Bias Current (*14)	Ib	25℃	-	1	-	pA	—
Supply Current (*15)	IDD	25℃	-	0.35	0.8	μA	RL=∞, AV=0[dB], VIN=1.0[V]
		Full range	-	-	1.3		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	60	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	2	V	VSS ~ VDD-1.0[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	—
Output Source Current (*16)	IOH	25℃	1	2.4	-	mA	VDD-0.4[V]
Output Sink Current (*16)	IOL	25℃	2	4	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	2.4	-	V/ms	CL=25[pF]
Gain Band width	FT	25℃	-	4	-	kHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	60	-	°	CL=25[pF], AV=40[dB]

(*14) Absolute value
(*15) Full range BU7411: Ta=-40[℃]~+85[℃] BU7411S: Ta=-40[℃]~+105[℃]
(*16) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7421 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7421G, BU7421SG				
			Min.	Typ.	Max.		
Input Offset Voltage (*17)	Vio	25℃	-	1	6	mV	VDD=1.7 ~ 5.5[V], VOUT=VDD/2
Input Offset Current (*17)	Iio	25℃	-	1	-	pA	—
Input Bias Current (*17)	Ib	25℃	-	1	-	pA	—
Supply Current (*18)	IDD	25℃	-	8.5	17	μA	RL=∞, AV=0[dB], VIN=0.9[V]
		Full range	-	-	25		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	70	100	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	—
Output Source Current (*19)	IOH	25℃	2	4	-	mA	VDD-0.4[V]
Output Sink Current (*19)	IOL	25℃	4	8	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	50	-	V/ms	CL=25[pF]
Gain Band width	FT	25℃	-	90	-	kHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	60	-	°	CL=25[pF], AV=40[dB]

(*17) Absolute value
(*18) Full range BU7421: Ta=-40[℃]~+85[℃] BU7421S: Ta=-40[℃]~+105[℃]
(*19) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○BU7475 family(Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7475HFV,BU7475SHFV				
			Min.	Typ.	Max.		
Input Offset Voltage (*20)	Vio	25℃	-	1	6.5	mV	VDD=1.7 ~ 5.5[V], VOUT=VDD/2
Input Offset Current (*20)	Iio	25℃	-	1	-	pA	-
Input ias Current (*20)	Ib	25℃	-	1	-	pA	-
Supply Current (*21)	IDD	25℃	-	9	18	µA	RL=∞, AV=0[dB] VIN=0.9[V]
		Full range	-	-	28		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25℃	60	100	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	1.8	V	VSS~VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	-
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	-
Output Source Current (*22)	IOH	25℃	4	7	-	mA	VDD-0.4[V]
Output Sink Current (*22)	IOL	25℃	9	14	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	50	-	V/ms	CL=25[pF]
Gain Band width	FT	25℃	-	100	-	kHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	60	-	°	CL=25[pF], AV=40[dB]

(*20) Absolute value
(*21) Full range BU7475: Ta=-40[℃]~+85[℃] BU7475S: Ta=-40[℃]~+105[℃]
(*22) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

●Reference Data

○BU7265 family

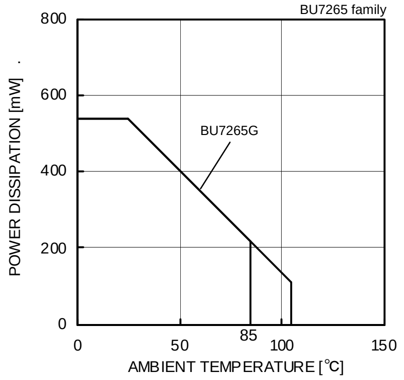


Fig.1
Derating curve

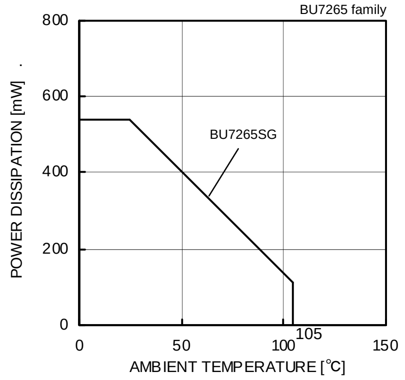


Fig.2
Derating curve

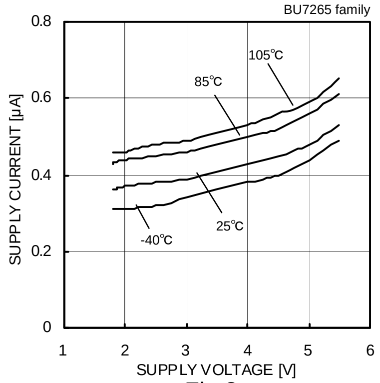


Fig.3
Supply Current – Supply Voltage

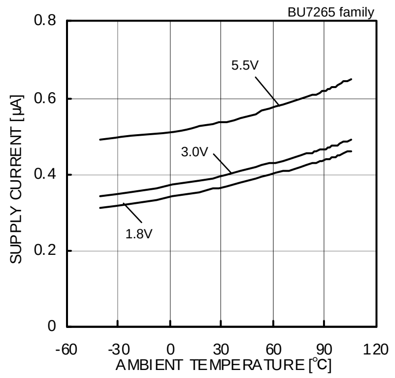


Fig.4
Supply Current – Ambient Temperature

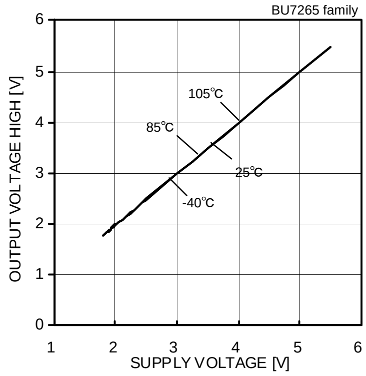


Fig.5
Output Voltage High – Supply Voltage
(RL=10[kΩ])

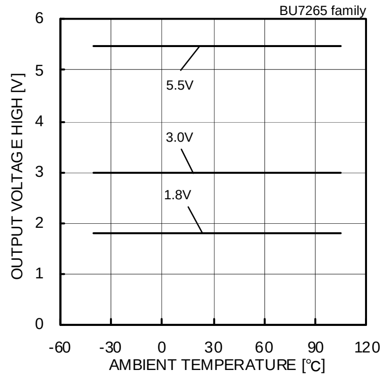


Fig.6
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

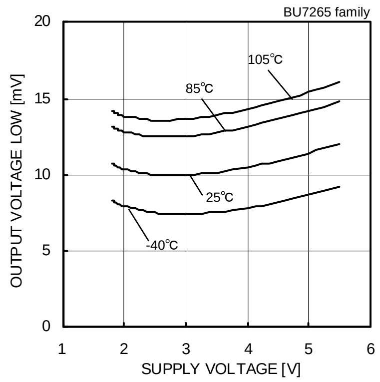


Fig.7
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

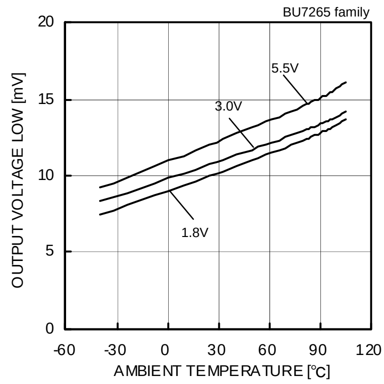


Fig.8
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

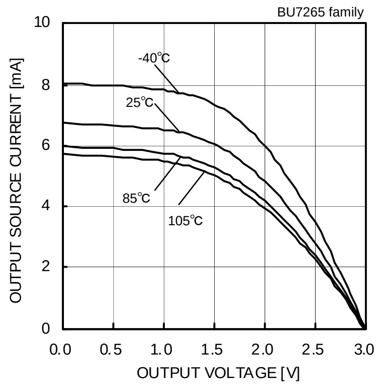


Fig.9
Output Source Current – Output Voltage
(VDD=3[V])

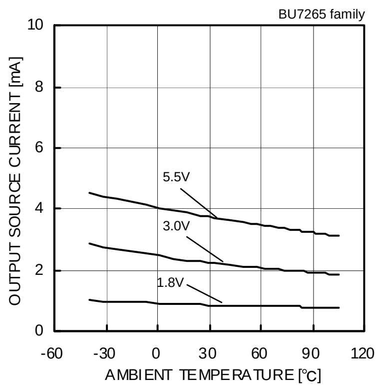


Fig.10
Output Source Current –Ambient Temperature
(VOUT=VDD-0.4[V])

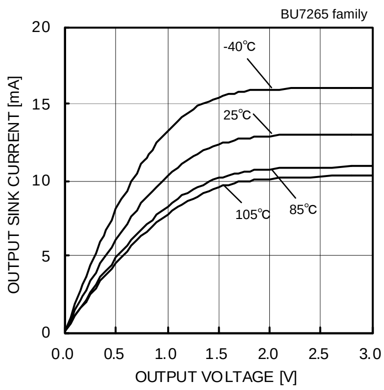


Fig.11
Output Sink Current – Output Voltage
(VDD=3[V])

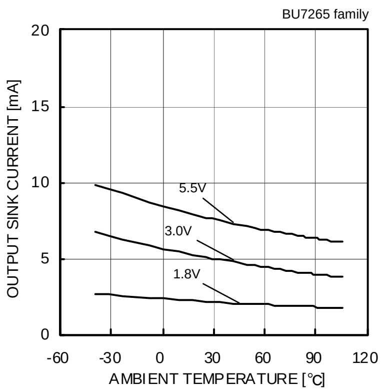


Fig.12
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7265G: -40[℃] ~ +85[℃] BU7265SG: -40[℃] ~ +105[℃]

○BU7265 family

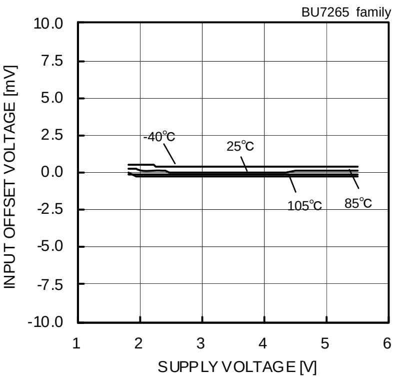


Fig.13
Input Offset Voltage – Supply Voltage
(Vicm=VDD,VOUT=0.1[V])

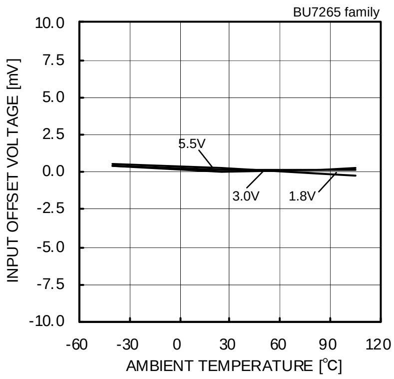


Fig.14
Input Offset Voltage – Ambient Temperature
(Vicm=VDD,VOUT=0.1[V])

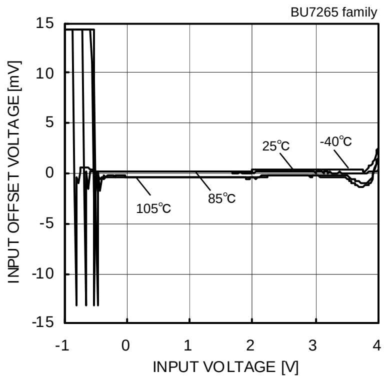


Fig.15
Input Offset Voltage – Input Voltage
(VDD=3[V])

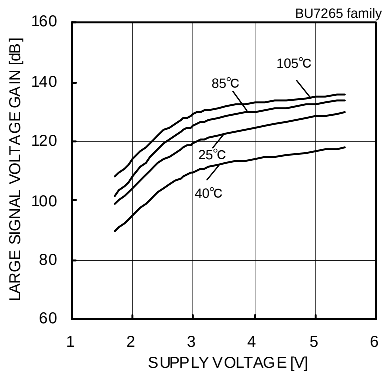


Fig.16
Large Signal Voltage Gain
– Supply Voltage

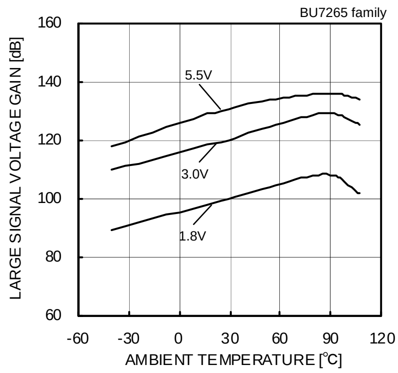


Fig.17
Large Signal Voltage Gain
– Ambient Temperature

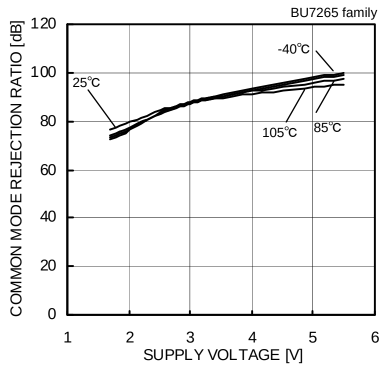


Fig.18
Common Mode Rejection Ratio
– Supply Voltage (VDD=3[V])

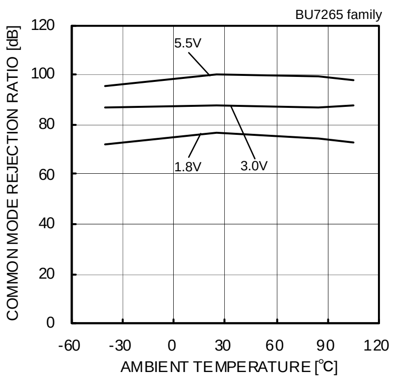


Fig.19
Common Mode Rejection
– Ambient Temperature
(VDD=3[V])

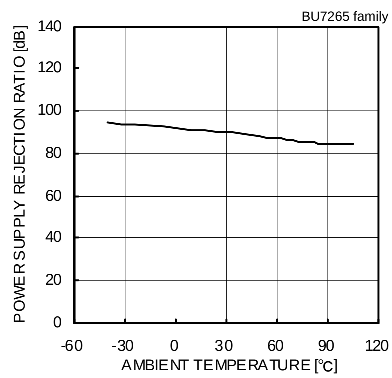


Fig.20
Power Supply Rejection Ratio
– Ambient Temperature

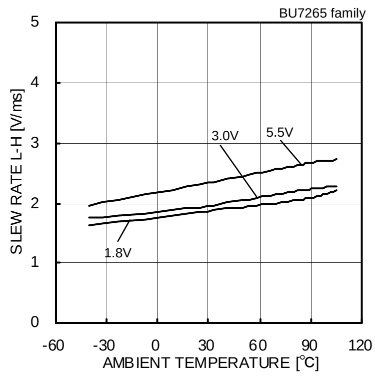


Fig.21
Slew Rate L-H
– Ambient Temperature

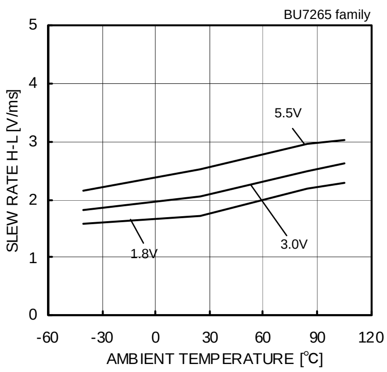


Fig.22
Slew Rate H-L – Ambient Temperature

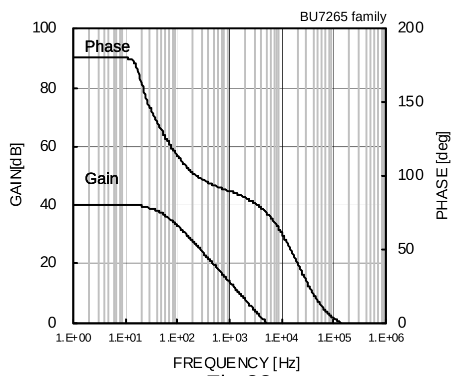


Fig.23
Voltage Gain－frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7265G: -40[℃] ~ +85[℃]　BU7265SG: -40[℃] ~ +105[℃]

○BU7271 family

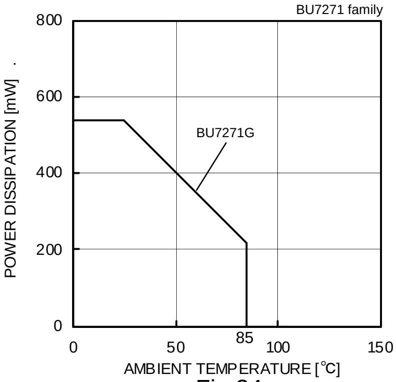


Fig.24
Derating curve

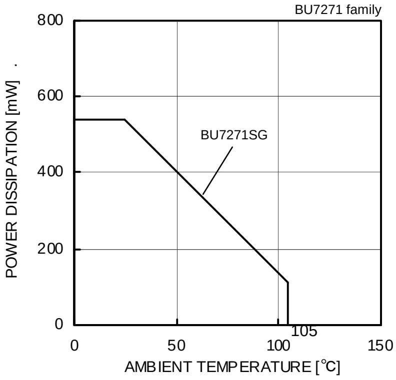


Fig.25
Derating curve

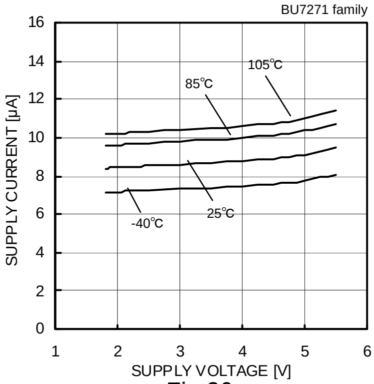


Fig.26
Supply Current – Supply Voltage

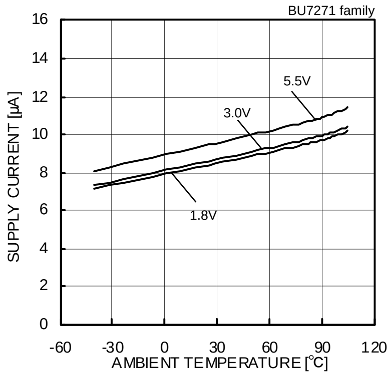


Fig.27
Supply Current – Ambient Temperature

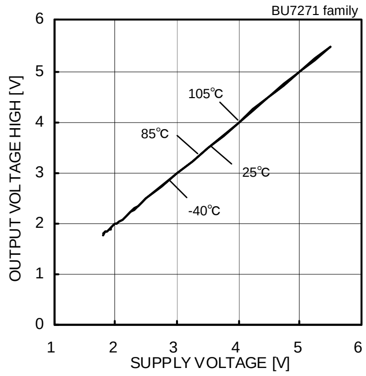


Fig.28
Output Voltage High – Supply Voltage
(RL=10[kΩ])

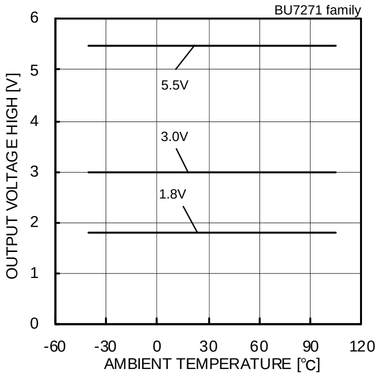


Fig.29
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

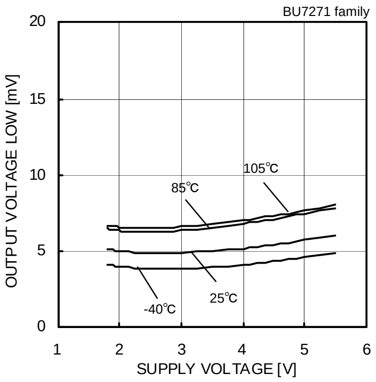


Fig.30
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

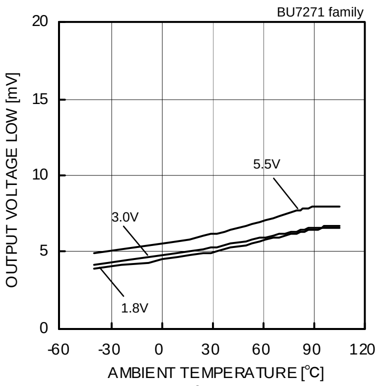


Fig.31
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

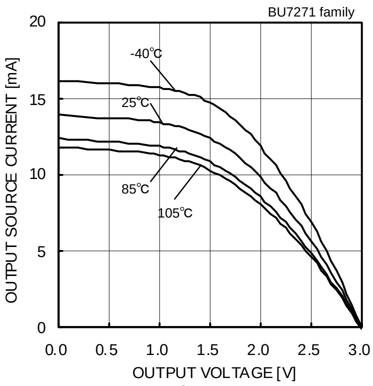


Fig.32
Output Source Current – Output Voltage
(VDD=3[V])

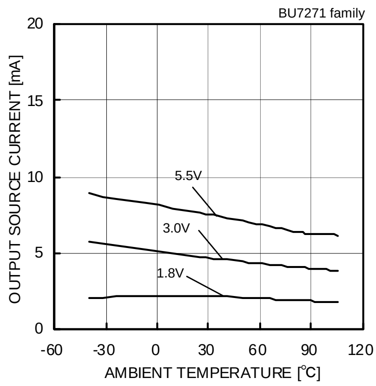


Fig.33
Output Source Current –Ambient Temperature
(VOUT=VDD-0.4[V])

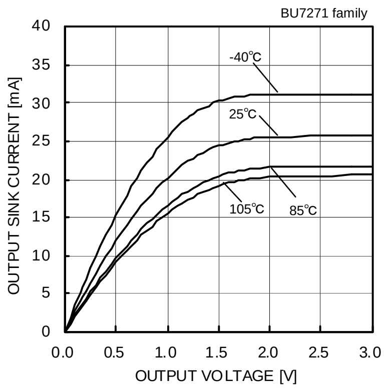


Fig.34
Output Sink Current – Output Voltage
(VDD=3[V])

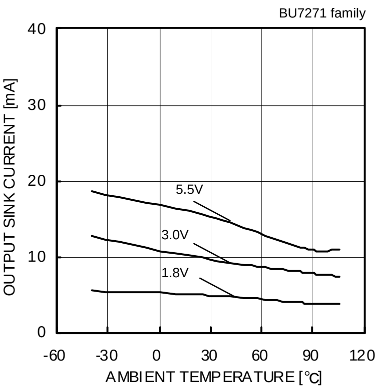


Fig.35
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7271G: -40[℃] ~ +85[℃] BU7271SG: -40[℃] ~ +105[℃]

○BU7271 family

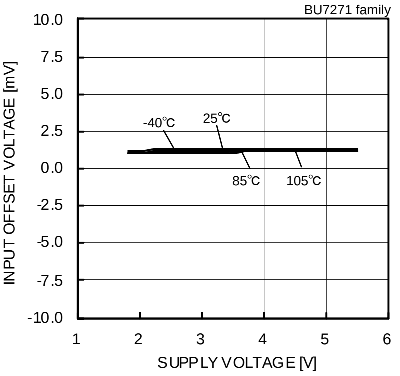


Fig.36

Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=0.1[V])

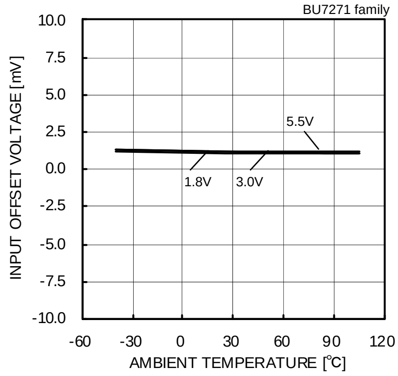


Fig.37

Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

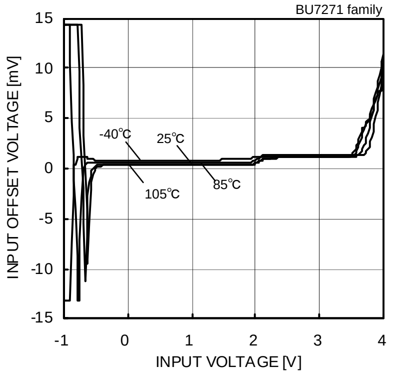


Fig.38

Input Offset Voltage – Input Voltage
(VDD=3[V])

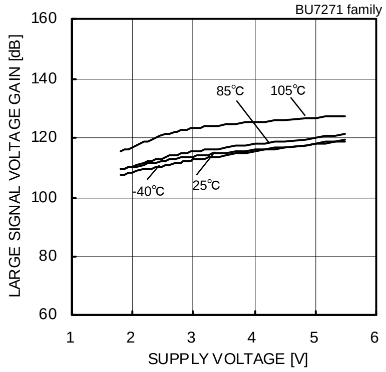


Fig.39

Large Signal Voltage Gain
– Supply Voltage

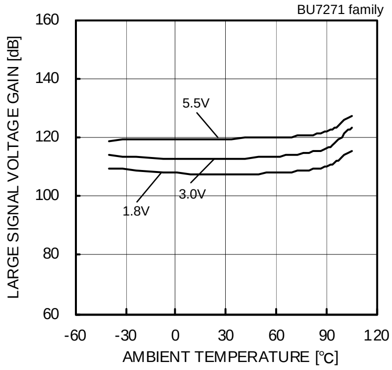


Fig.40

Large Signal Voltage Gain
– Ambient Temperature

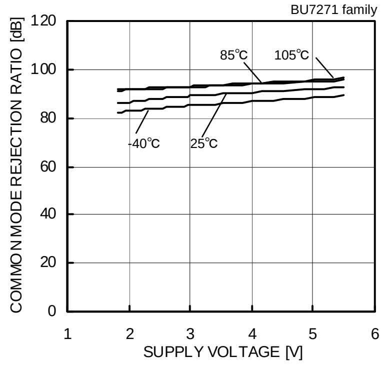


Fig.41

Common Mode Rejection Ratio
– Supply Voltage
(VDD=3[V])

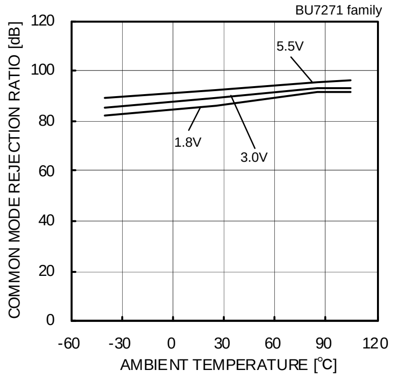


Fig.42

Common Mode Rejection Ratio
– Ambient Temperature

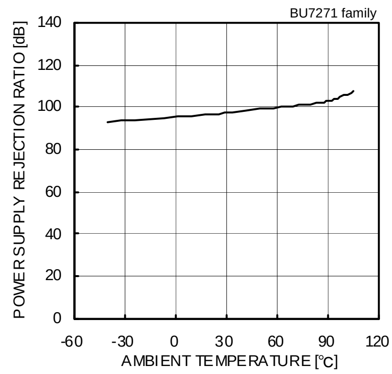


Fig.43

Power Supply Rejection Ratio
– Ambient Temperature

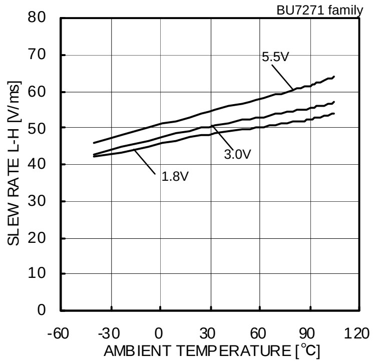


Fig.44

Slew Rate L-H – Ambient Temperature

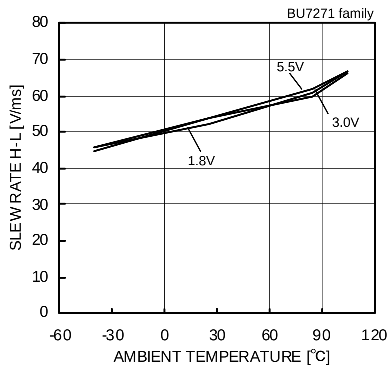


Fig.45

Slew Rate H-L – Ambient Temperature

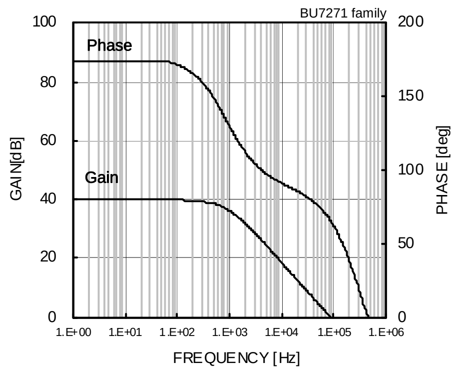


Fig.46

Voltage Gain－Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7271G: -40[℃] ~ +85[℃] BU7271SG: -40[℃] ~ +105[℃]

○BU7205 family

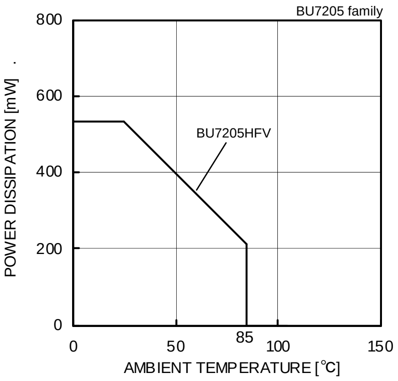


Fig.47
Derating curve

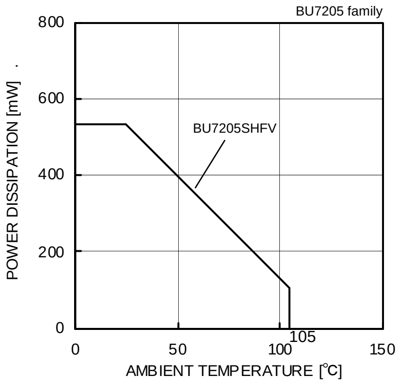


Fig.48
Derating curve

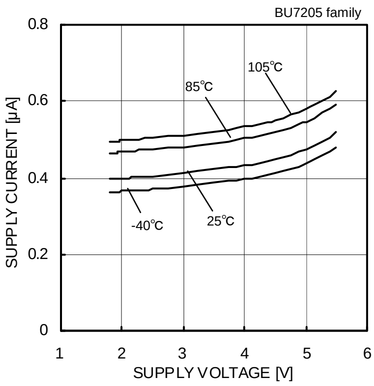


Fig.49
Supply Current – Supply Voltage

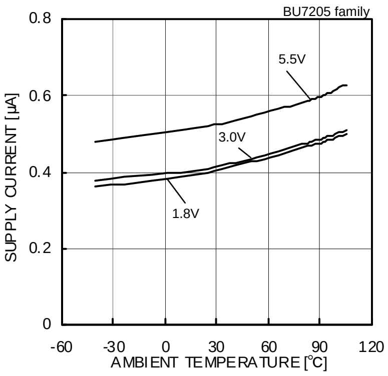


Fig.50
Supply Current – Ambient Temperature

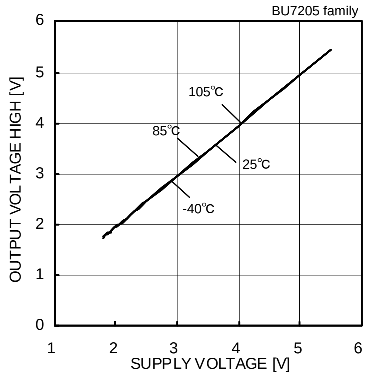


Fig.51
Output Voltage High – Supply Voltage
(RL=10[kΩ])

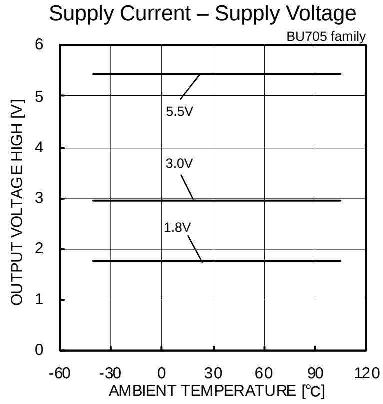


Fig.52
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

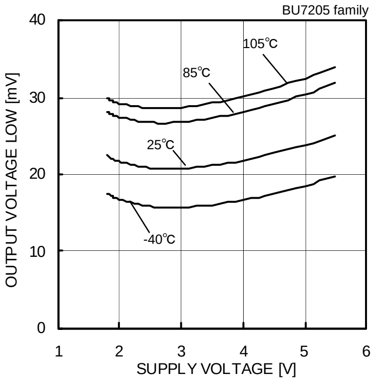


Fig.53
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

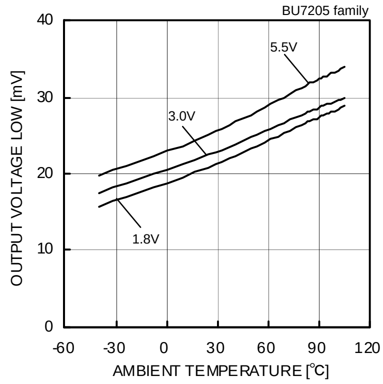


Fig.54
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

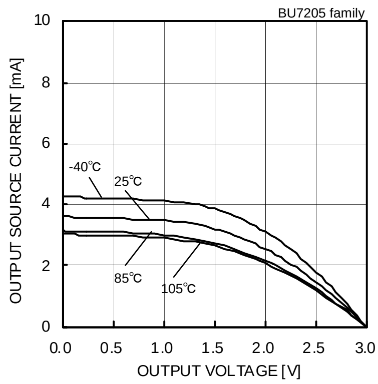


Fig.55
Output Source Current – Output Voltage
(VDD=3[V])

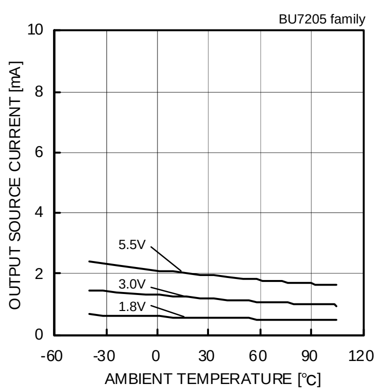


Fig.56
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

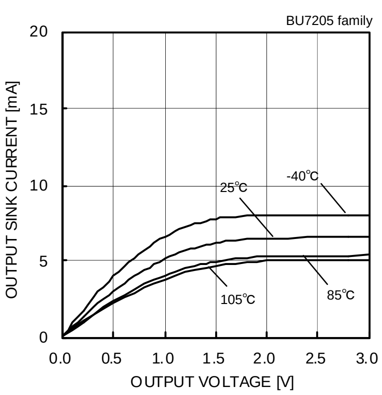


Fig.57
Output Sink Current – Output Voltage
(VDD=3[V])

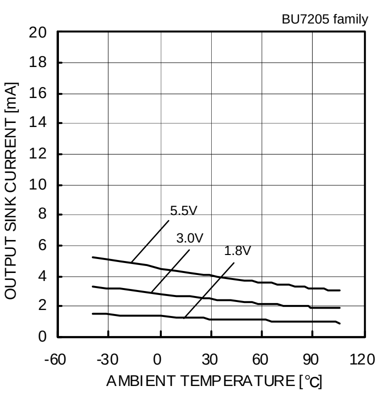


Fig.58
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7205HFV: -40[℃] ~ +85[℃] BU7205SHFV: -40[℃] ~ +105[℃]

○BU7205 family

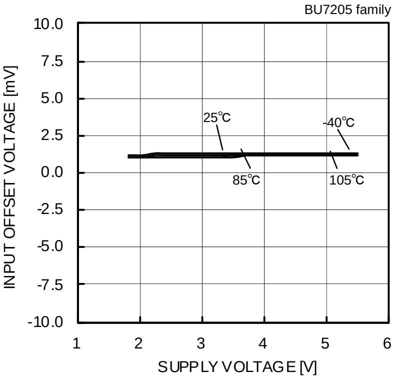


Fig.59
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=1.5[V])

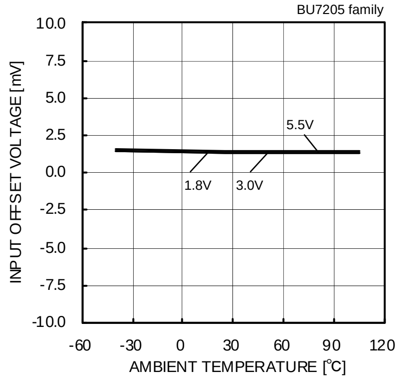


Fig.60
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

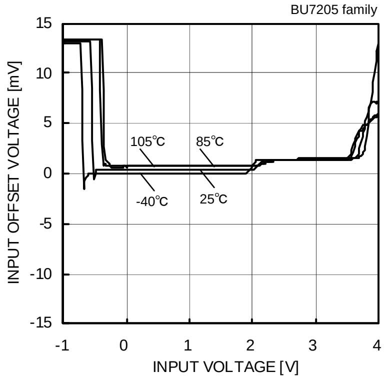


Fig.61
Input Offset Voltage – Input Voltage
(VDD=3[V])

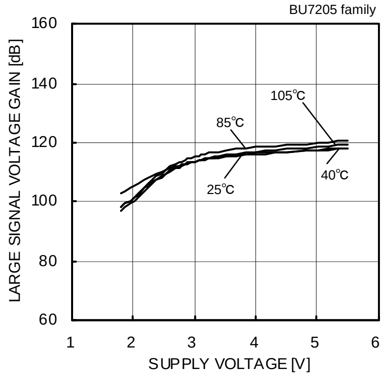


Fig.62
Large Signal Voltage Gain
– Supply Voltage

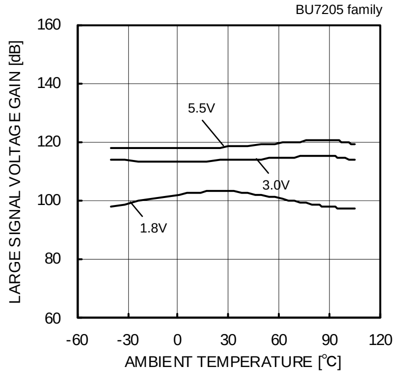


Fig.63
Large Signal Voltage Gain
– Ambient Temperature

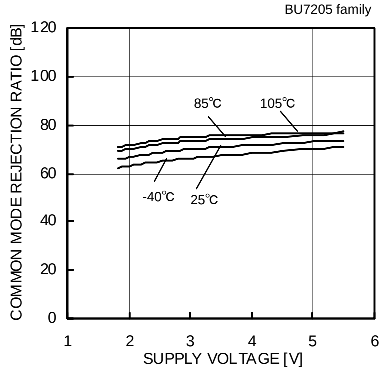


Fig.64
Common Mode Rejection Ratio
– Supply Voltage

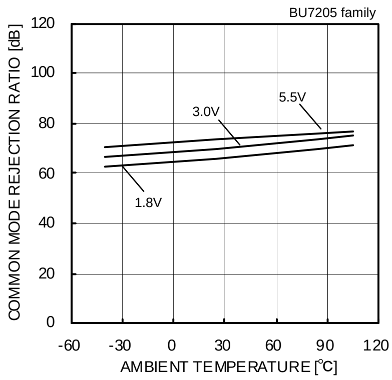


Fig.65
Common Mode Rejection Ratio
– Ambient Temperature

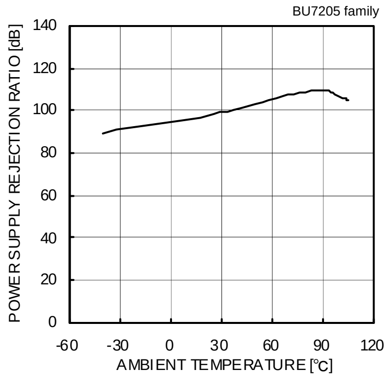


Fig.66
Power Supply Rejection Ratio
– Ambient Temperature

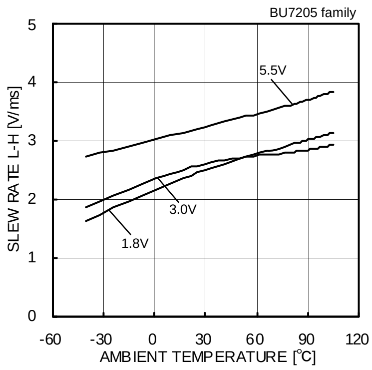


Fig.67
Slew Rate L-H – Ambient Temperature

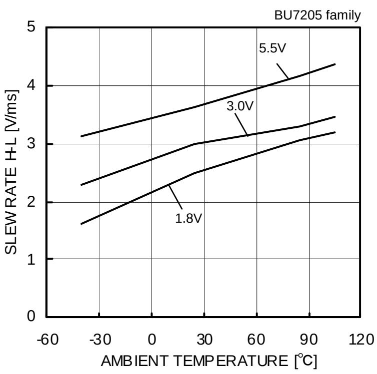


Fig.68
Slew Rate H-L – Ambient Temperature

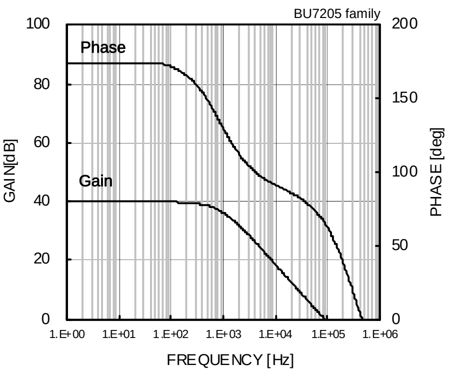


Fig.69
Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7205HFV: -40[℃] ~ +85[℃] BU7205SHFV: -40[℃] ~ +105[℃]

○BU7245 family

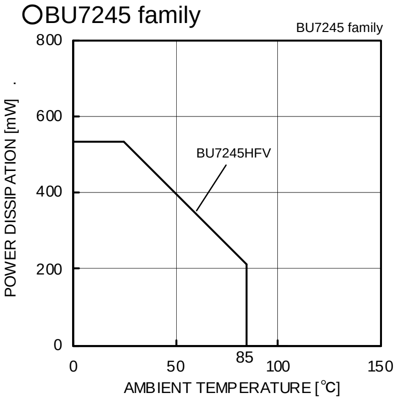


Fig.70
Derating curve

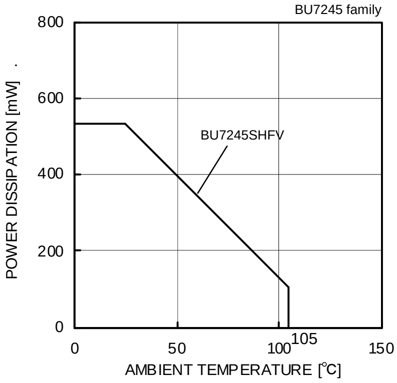


Fig.71
Derating curve

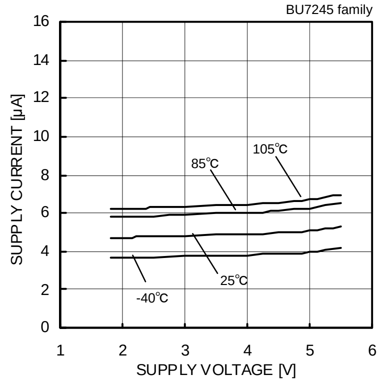


Fig.72
Supply Current – Supply Voltage

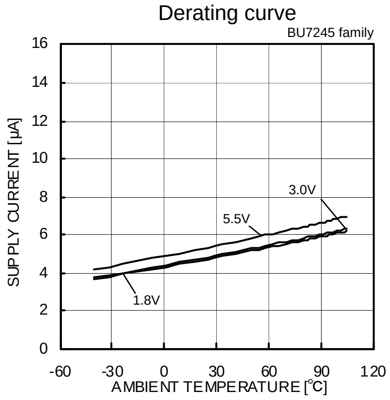


Fig.73
Supply Current – Ambient Temperature

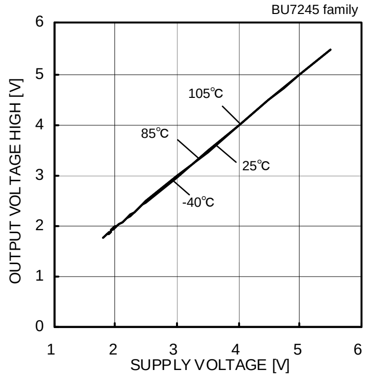


Fig.74
Output Voltage High – Supply Voltage
(RL=10[kΩ])

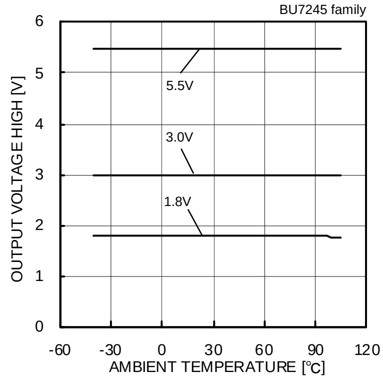


Fig.75
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

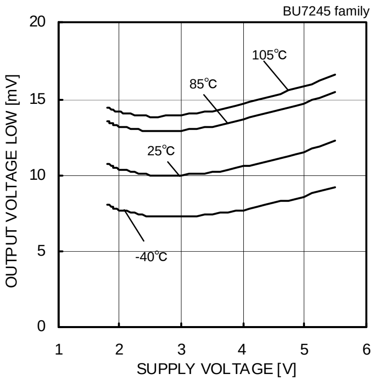


Fig.76
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

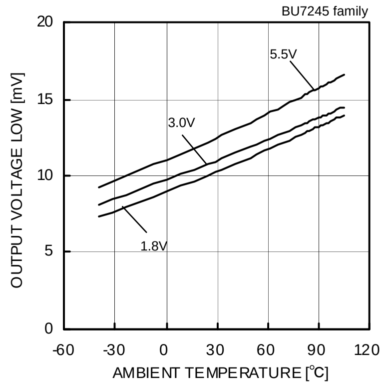


Fig.77
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

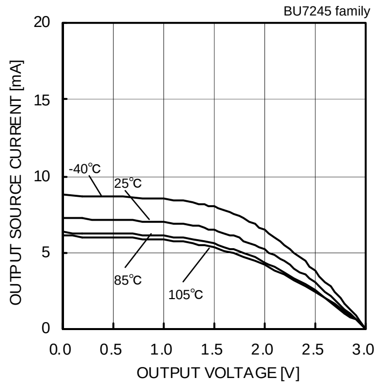


Fig.78
Output Source Current – Output Voltage
(VDD=3[V])

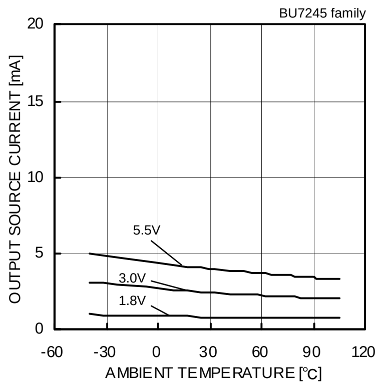


Fig.79
Output Source Current –Ambient Temperature
(VOUT=VDD-0.4[V])

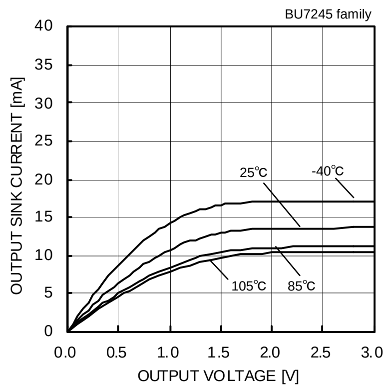


Fig.80
Output Sink Current – Output Voltage
(VDD=3[V])

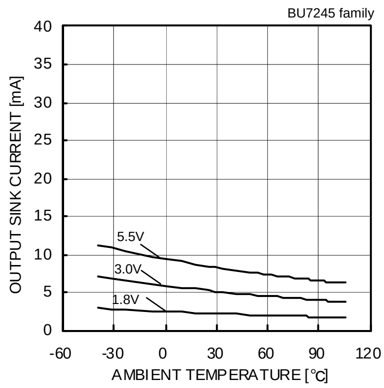


Fig.81
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7245HFV: -40[℃] ~ +85[℃] BU7245SHFV: -40[℃] ~ +105[℃]

○BU7245 family

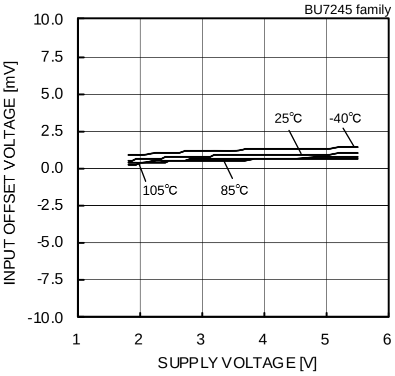


Fig.82
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=1.5[V])

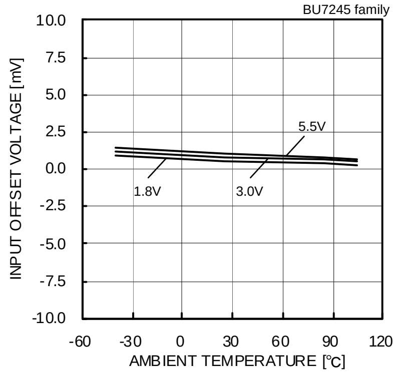


Fig.83
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

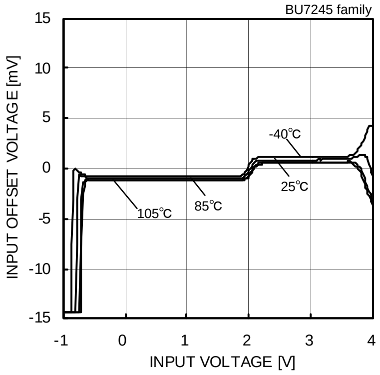


Fig.84
Input Offset Voltage – Input Voltage
(VDD=3[V])

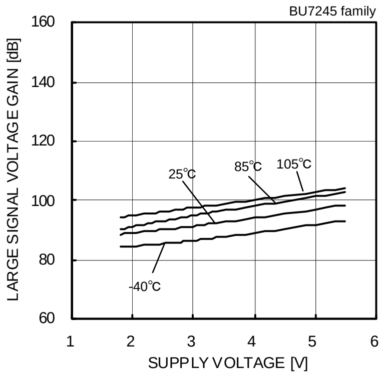


Fig.85
Large Signal Voltage Gain
– Supply Voltage

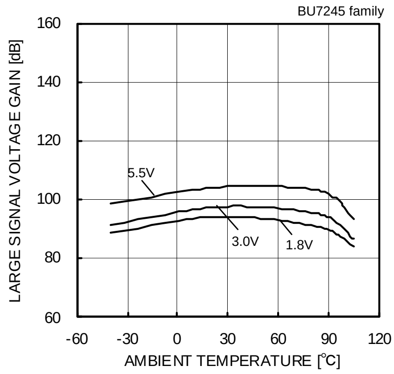


Fig.86
Large Signal Voltage Gain
– Ambient Temperature

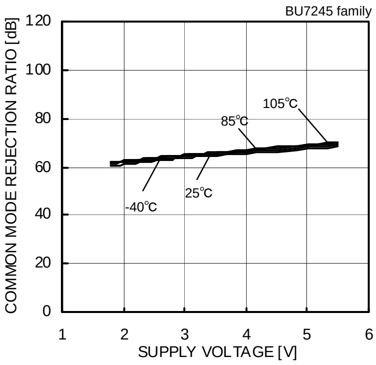


Fig.87
Common Mode Rejection Ratio
– Supply Voltage

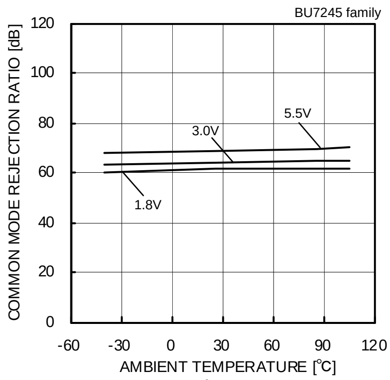


Fig.88
Common Mode Rejection Ratio
– Ambient Temperature

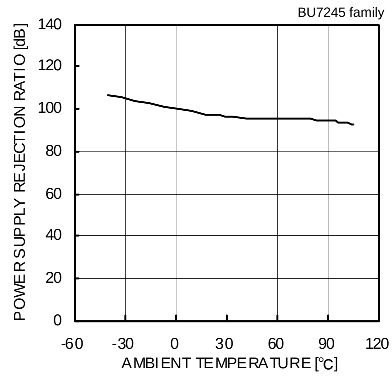


Fig.89
Power Supply Rejection Ratio
– Ambient Temperature

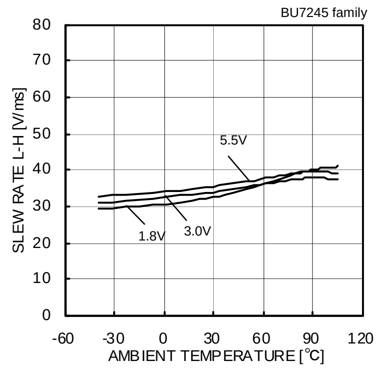


Fig.90
Slew Rate L-H – Ambient Temperature

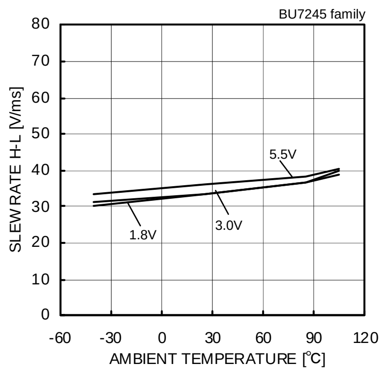


Fig.91
Slew Rate H-L – Ambient Temperature

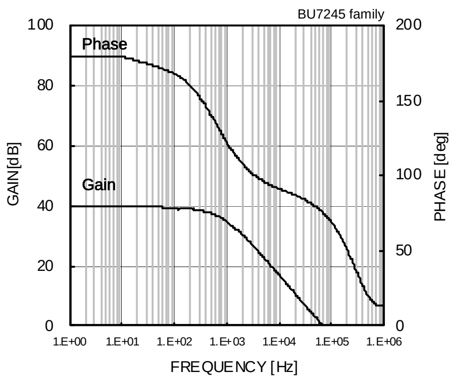


Fig.92
Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7245HFV: -40[℃] ~ +85[℃] BU7245SHFV: -40[℃] ~ +105[℃]

○BU7411 family

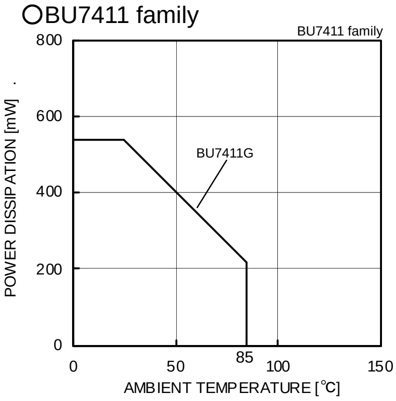


Fig.93
Derating curve

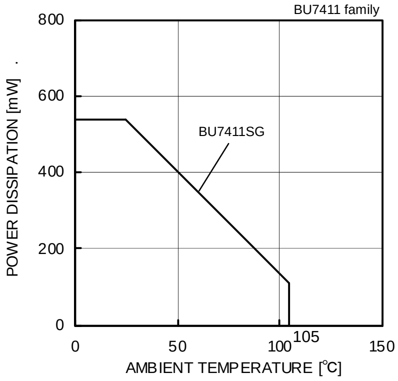


Fig.94
Derating curve

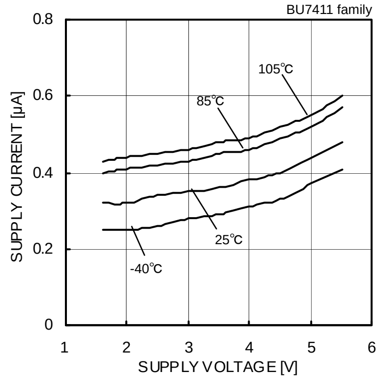


Fig.95
Supply Current – Supply Voltage

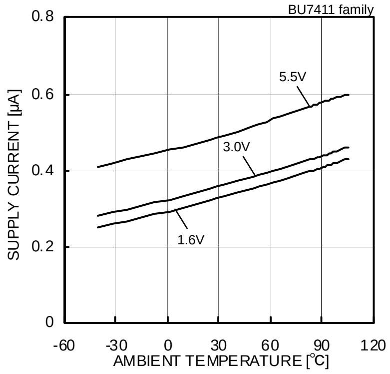


Fig.96
Supply Current – Ambient Temperature

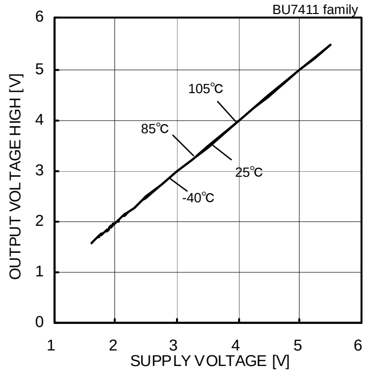


Fig.97
Output Voltage High – Supply Voltage
(RL=10[kΩ])

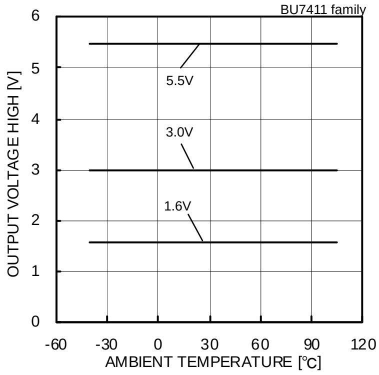


Fig.98
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

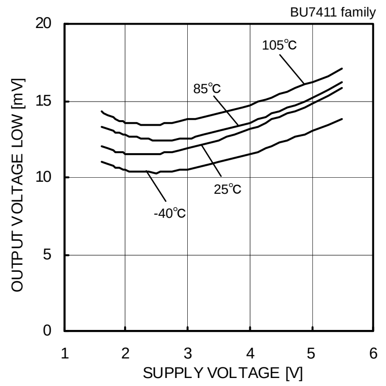


Fig.99
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

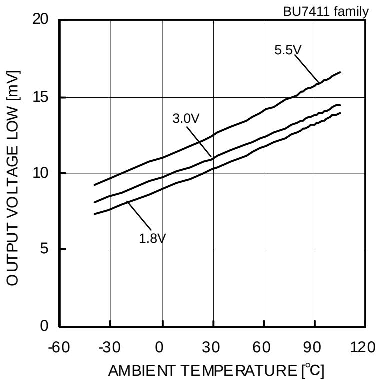


Fig.100
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

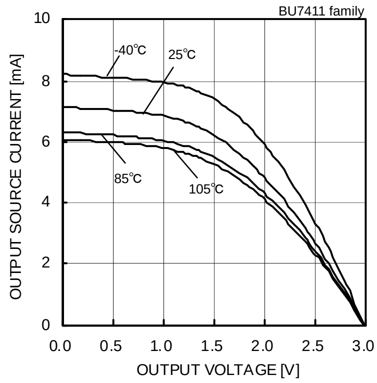


Fig.101
Output Source Current – Output Voltage
(VDD=3[V])

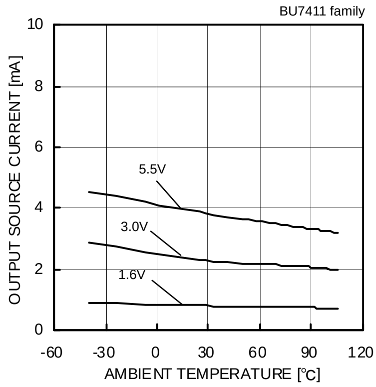


Fig.102
Output Source Current –Ambient Temperature
(VOUT=VDD-0.4[V])

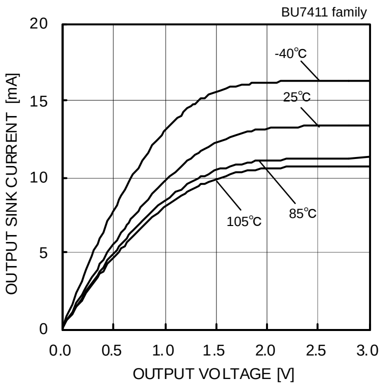


Fig.103
Output Sink Current – Output Voltage
(VDD=3[V])

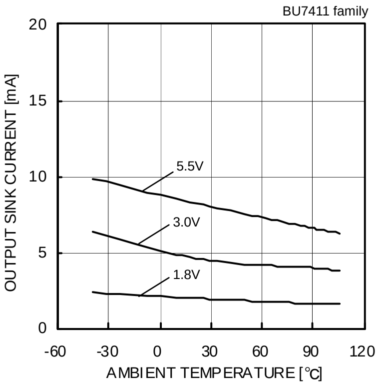


Fig.104
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7411G: -40[℃] ~ +85[℃] BU7411SG: -40[℃] ~ +105[℃]

○BU7411 family

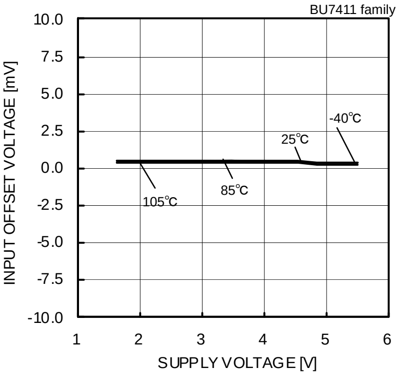


Fig.105
Input Offset Voltage – Supply Voltage
(Vicm=VDD-1.2[V], VOUT=1.5[V])

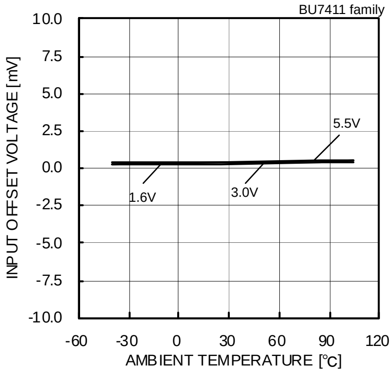


Fig.106
Input Offset Voltage – Ambient Temperature
(Vicm=VDD-1.2[V], VOUT=1.5[V])

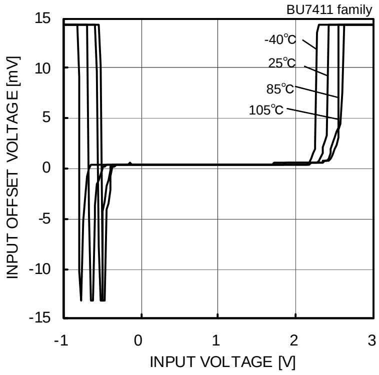


Fig.107
Input Offset Voltage – Input Voltage
(VDD=3[V])

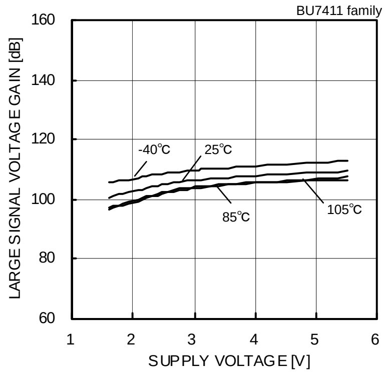


Fig.108
Large Signal Voltage Gain
– Supply Voltage

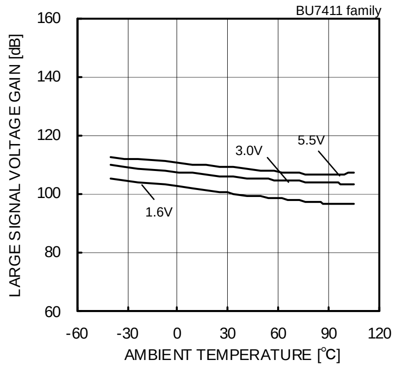


Fig.109
Large Signal Voltage Gain
– Ambient Temperature

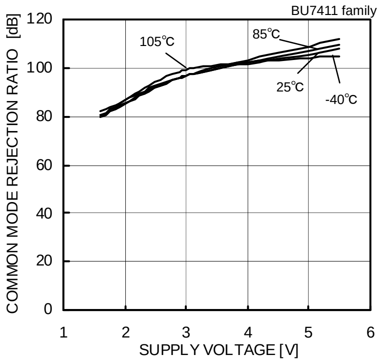


Fig.110
Common Mode Rejection Ratio
– Supply Voltage

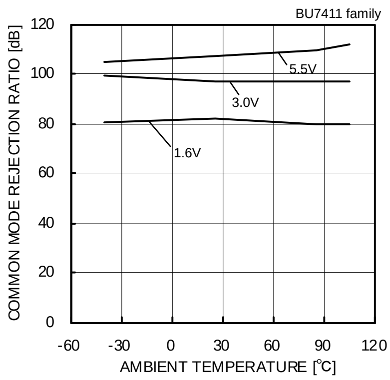


Fig.111
Common Mode Rejection Ratio
– Ambient Temperature

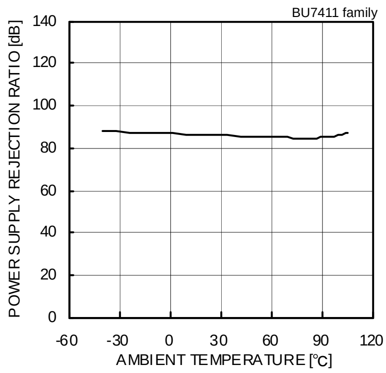


Fig.112
Power Supply Rejection Ratio
– Ambient Temperature

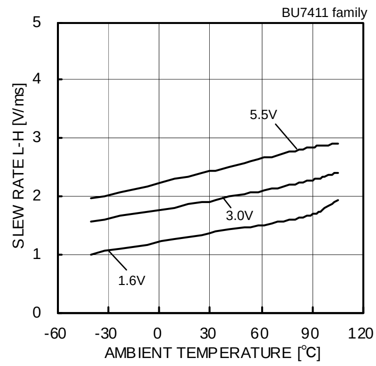


Fig.113
Slew Rate L-H – Ambient Temperature

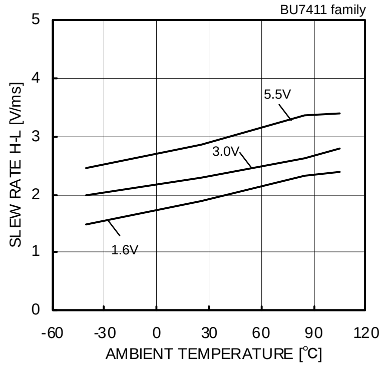


Fig.114
Slew Rate H-L – Ambient Temperature

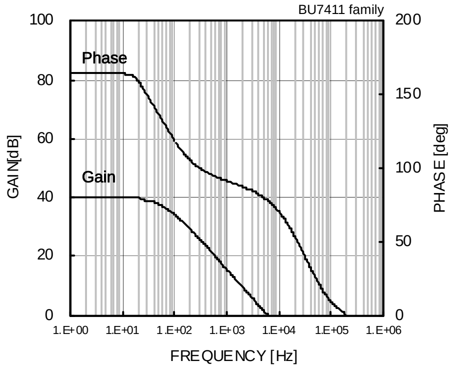


Fig.115
Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7411G: -40[℃] ~ +85[℃] BU7411SG: -40[℃] ~ +105[℃]

○BU7421 family

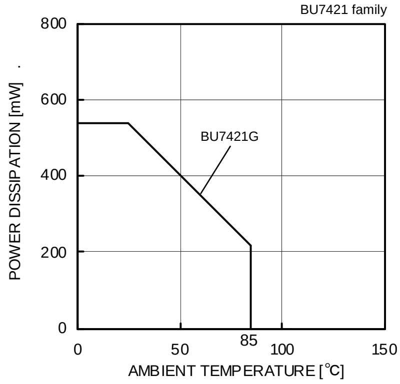


Fig.116
Derating curve

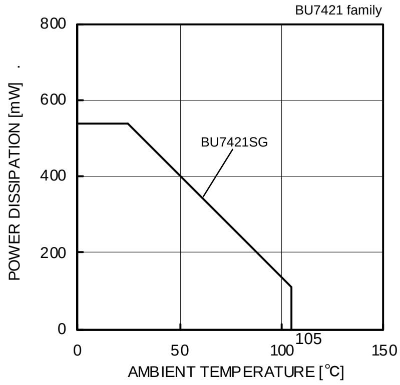


Fig.117
Derating curve

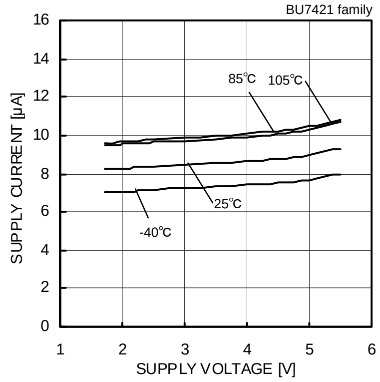


Fig.118
Supply Current – Supply Voltage

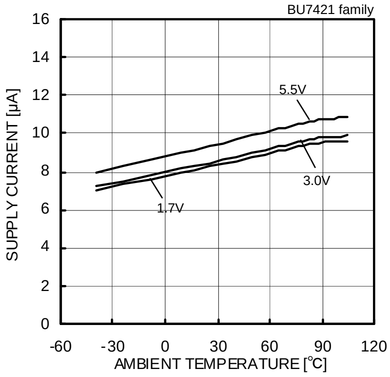


Fig.119
Supply Current – Ambient Temperature

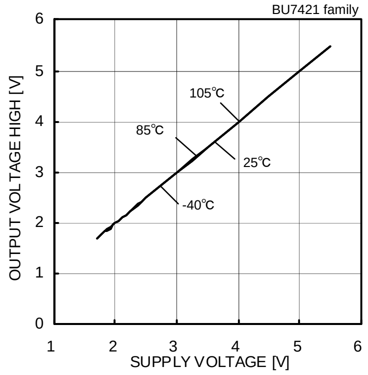


Fig.120
Output Voltage High – Supply Voltage
(RL=10[kΩ])

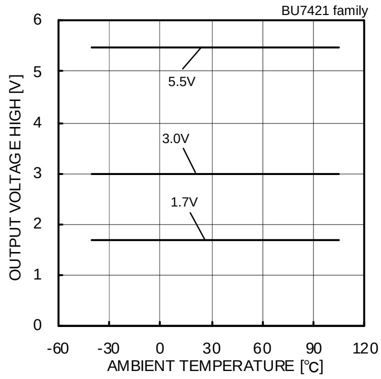


Fig.121
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

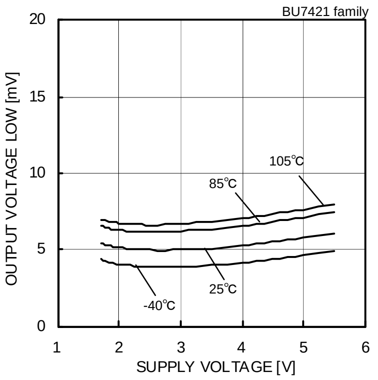


Fig.122
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

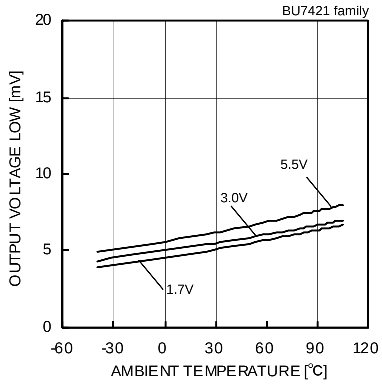


Fig.123
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

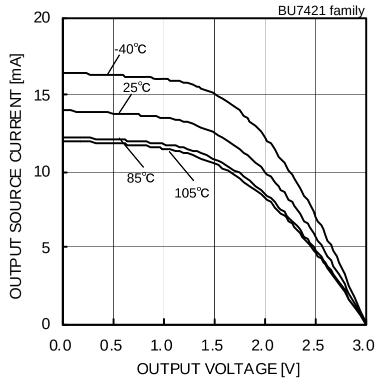


Fig.124
Output Source Current – Output Voltage
(VDD=3[V])

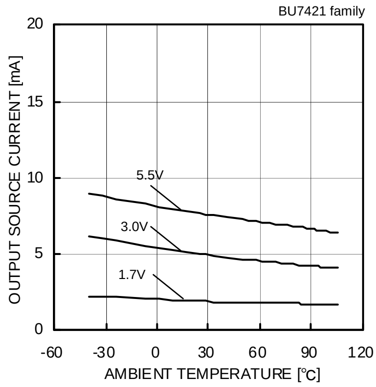


Fig.125
Output Source Current –Ambient Temperature
(VOUT=VDD-0.4[V])

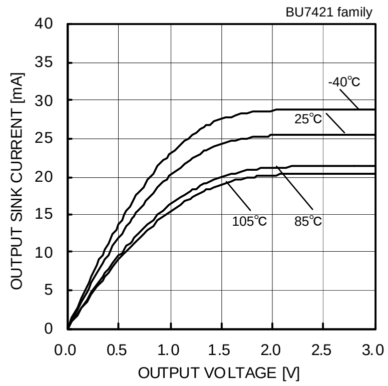


Fig.126
Output Sink Current – Output Voltage
(VDD=3[V])

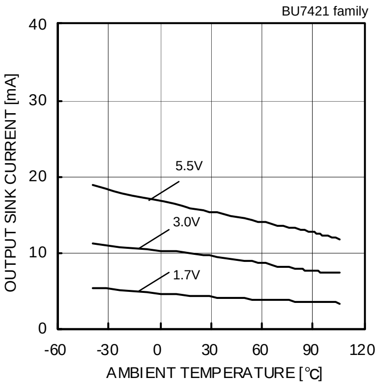


Fig.127
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7421G: -40[℃] ~ +85[℃] BU7421SG: -40[℃] ~ +105[℃]]

○BU7421 family

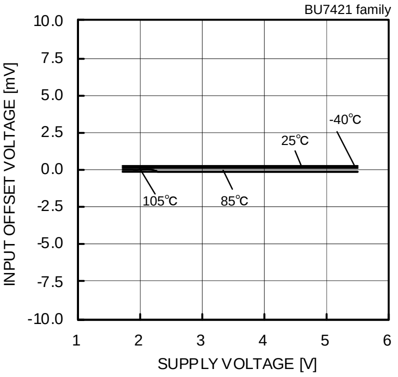


Fig.128
Input Offset Voltage – Supply Voltage
(Vicm=VDD-1.2[V], VOUT=1.5[V])

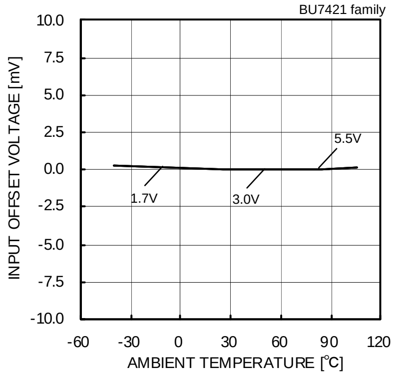


Fig.129
Input Offset Voltage – Ambient Temperature
(Vicm=VDD-1.2[V], VOUT=1.5[V])

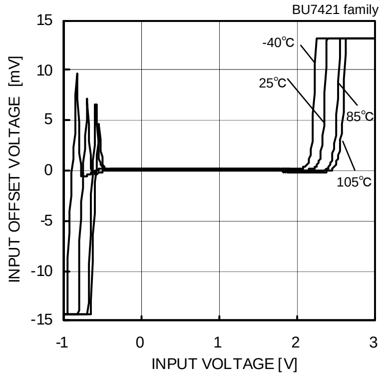


Fig.130
Input Offset Voltage – Input Voltage
(VDD=3[V])

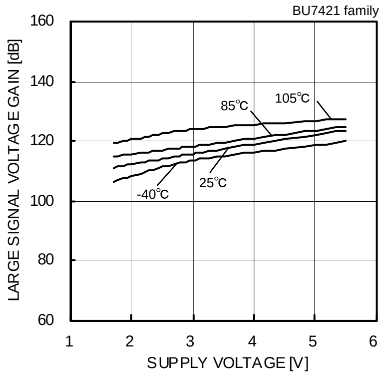


Fig.131
Large Signal Voltage Gain
– Supply Voltage

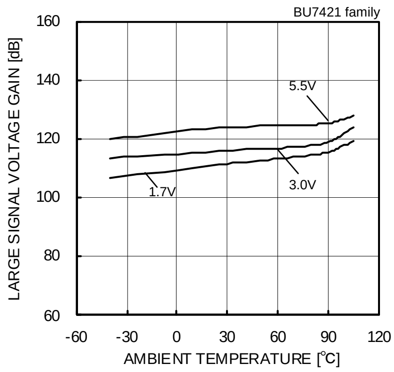


Fig.132
Large Signal Voltage Gain
– Ambient Temperature

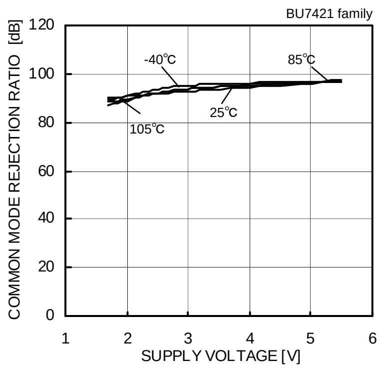


Fig.133
Common Mode Rejection Ratio
– Supply Voltage

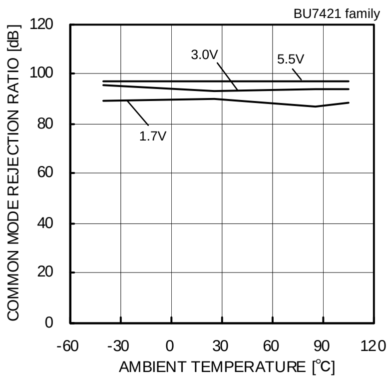


Fig.134
Common Mode Rejection Ratio
– Ambient Temperature

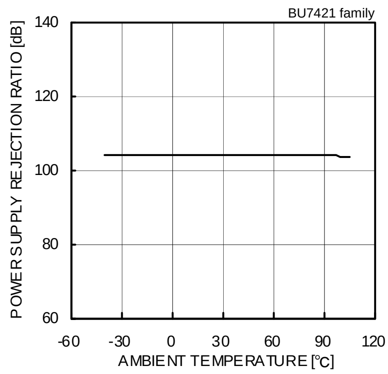


Fig.135
Power Supply Rejection Ratio
– Ambient Temperature

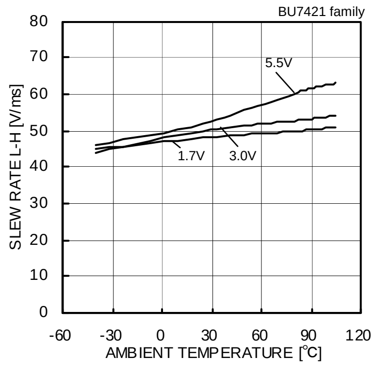


Fig.136
Slew Rate L-H – Ambient Temperature

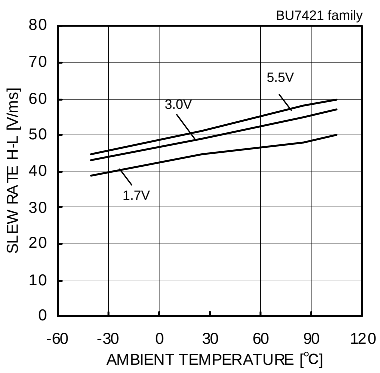


Fig.137
Slew Rate H-L – Ambient Temperature

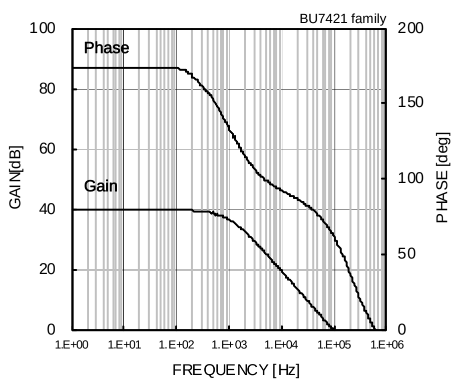


Fig.138
Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7421G: -40[℃] ~ +85[℃] BU7421SG: -40[℃] ~ +105[℃]

○BU7475 family

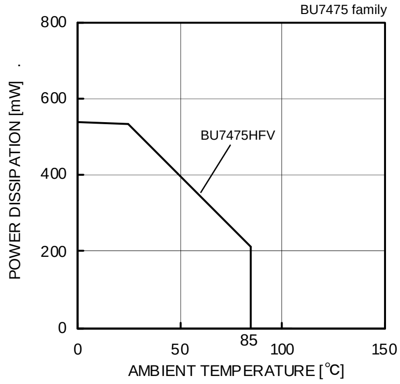


Fig.139
Derating curve

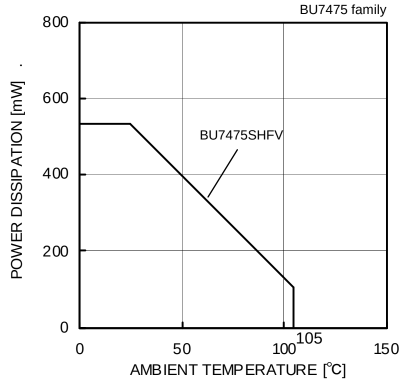


Fig.140
Derating curve

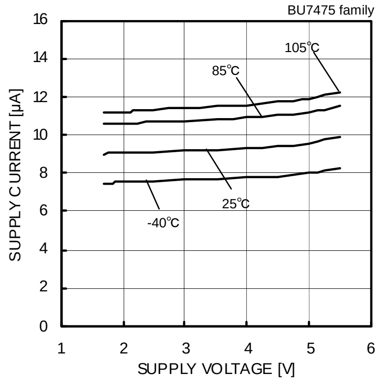


Fig.141
Supply Current – Supply Voltage

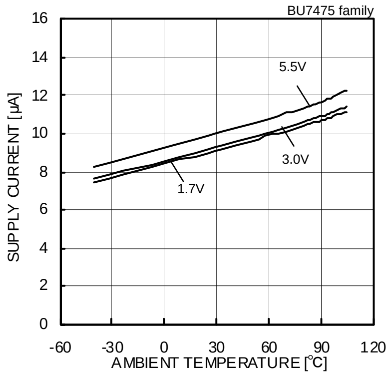


Fig.142
Supply Current – Ambient Temperature

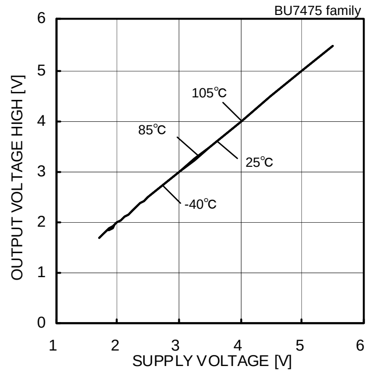


Fig.143
Output Voltage High – Supply Voltage
(RL=10[kΩ])

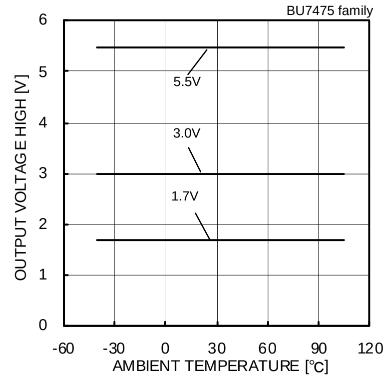


Fig.144
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

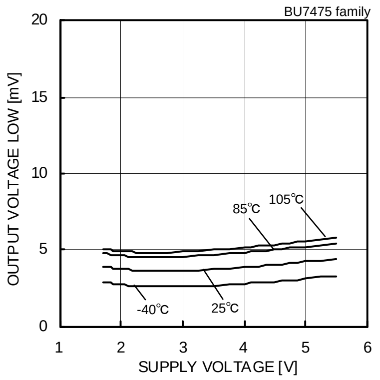


Fig.145
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

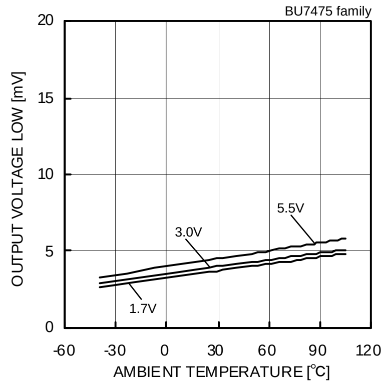


Fig.146
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

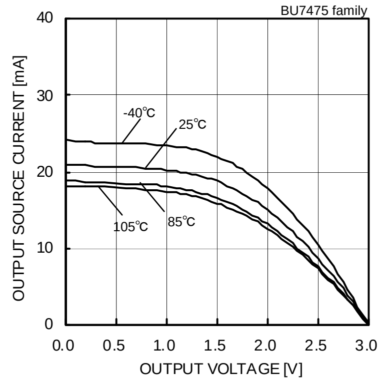


Fig.147
Output Source Current – Output Voltage
(VDD=3[V])

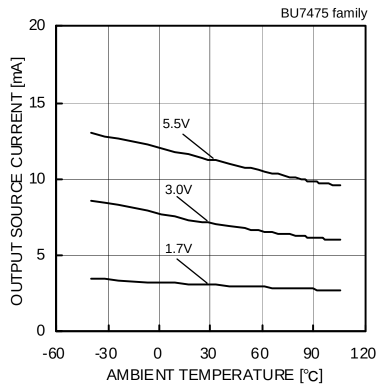


Fig.148
Output Source Current –Ambient Temperature
(VOUT=VDD-0.4[V])

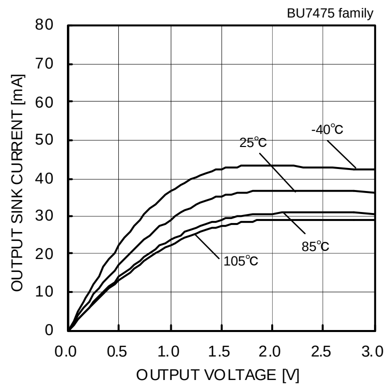


Fig.149
Output Sink Current – Output Voltage
(VDD=3[V])

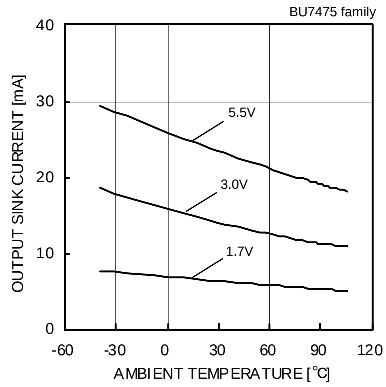


Fig.150
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7475HFV: -40[℃] ~ +85[℃] BU7475SHFV: -40[℃] ~ +105[℃]

○BU7475 family

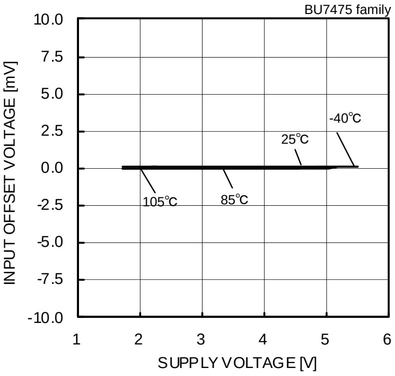


Fig.151
Input Offset Voltage – Supply Voltage
(Vicm=VDD-1.2[V], VOUT=1.5[V])

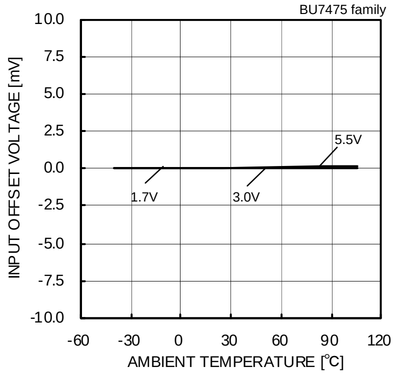


Fig.152
Input Offset Voltage – Ambient Temperature
(Vicm=VDD-1.2[V], VOUT=1.5[V])

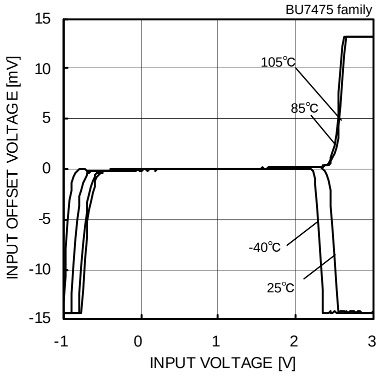


Fig.153
Input Offset Voltage – Input Voltage
(VDD=3[V])

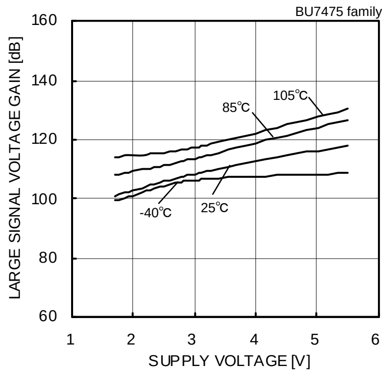


Fig.154
Large Signal Voltage Gain
– Supply Voltage

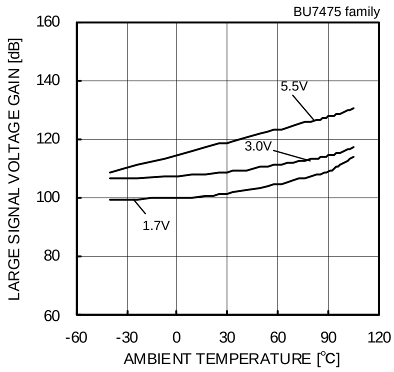


Fig.155
Large Signal Voltage Gain
– Ambient Temperature

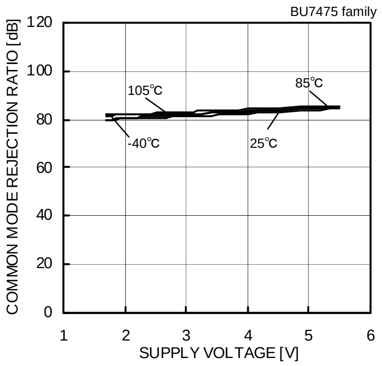


Fig.156
Common Mode Rejection Ratio
– Supply Voltage

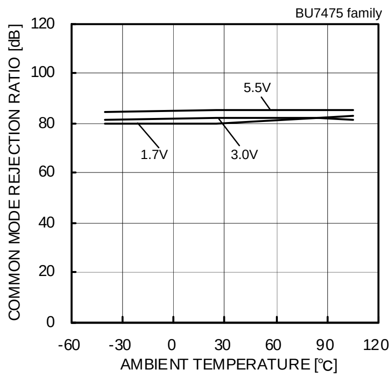


Fig.157
Common Mode Rejection Ratio
– Ambient Temperature

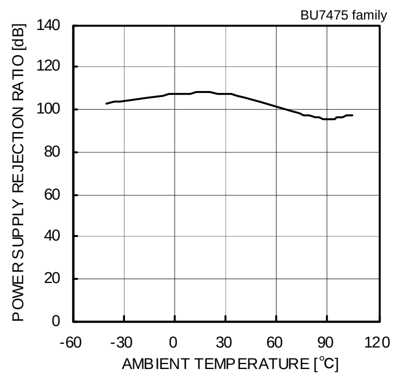


Fig.158
Power Supply Rejection Ratio
– Ambient Temperature

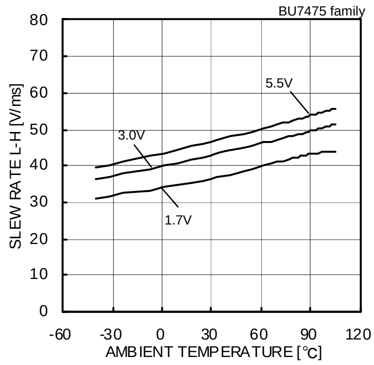


Fig.159
Slew Rate L-H – Ambient Temperature

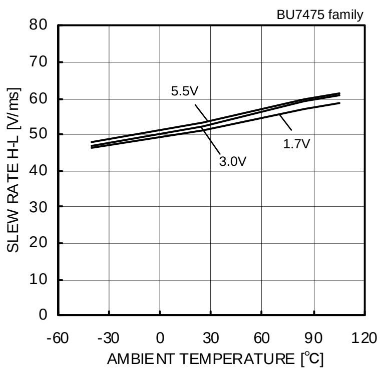


Fig.160
Slew Rate H-L – Ambient Temperature

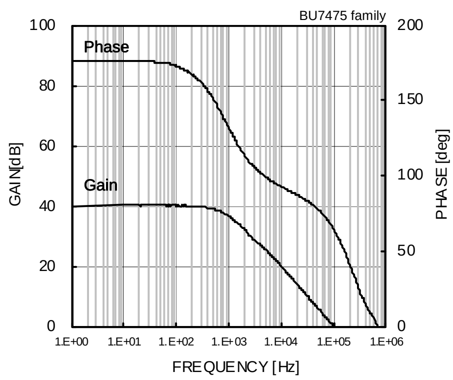
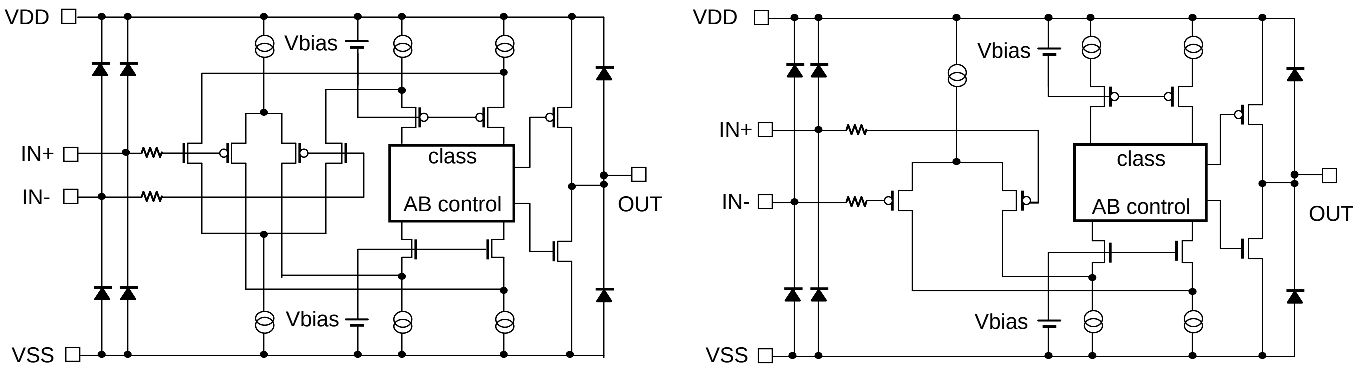


Fig.161
Voltage Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7475HFV: -40[℃] ~ +85[℃] BU7475SHFV: -40[℃] ~ +105[℃]

●Schematic Diagram



○Input-Output Full Swing
BU7265/BU7271/BU7205/BU7245 family

○Ground Sense
BU7411/BU7421/BU7475family

Fig.162 Schematic Diagram

●Test circuit 1 NULL method

VDD, VSS, EK, Vicm Unit:[V]

Parameter	VF		S1	S2	S3	VDD	VSS	EK	Vicm BU7265 /BU7271	Vicm BU7205 /BU7245	Vicm BU7411	Vicm BU7421 /BU7475	Calculation
Input Offset Voltage	VF1		ON	ON	OFF	3	0	-1.5	3	3	2	1.8	1
Large Signal Voltage Gain	VF2		ON	ON	ON	3	0	-0.5	1.5	1.5	1	0.9	2
	VF3							-2.5					
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	VF4		ON	ON	OFF	3	0	-1.5	0	0	0	0	3
	VF5								3	3	2	1.8	
Power Supply Rejection Ratio	VF6	BU7265/BU7271	ON	ON	OFF	1.8	0	-0.9	0	0	0	0	4
		BU7205/BU7245	ON	ON	OFF	1.8							
		BU7421/BU7475	ON	ON	OFF	1.7							
		BU7411	ON	ON	OFF	1.6							
	VF7		ON	ON	OFF	5.5							

－ Calculation－

1. Input Offset Voltage (Vio) $Vio = \frac{|VF1|}{1+Rf/Rs}$ [V]

2. Large Signal Voltage Gain (Av) $Av = 20Log \frac{2 \times (1+Rf/Rs)}{|VF2-VF3|}$ [dB]

3 Common-mode Rejection Ratio (CMRR) $CMRR = 20Log \frac{\Delta Vicm \times (1+Rf/Rs)}{|VF4-VF5|}$ [dB]

4. Power Supply Rejection Ratio (PSRR) $PSRR = 20Log \frac{\Delta VDD \times (1+Rf/Rs)}{|VF6-VF7|}$ [dB]

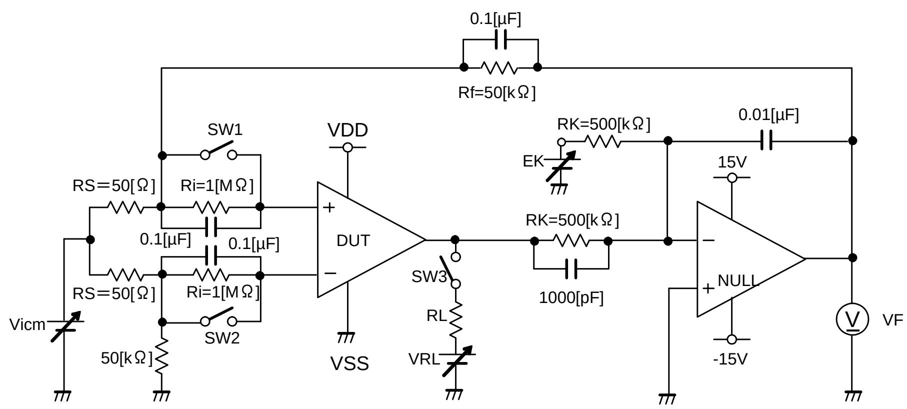


Fig.163 Test circuit 1

●Test circuit 2 switch condition

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage (RL=10[kΩ])	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Maximum Frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

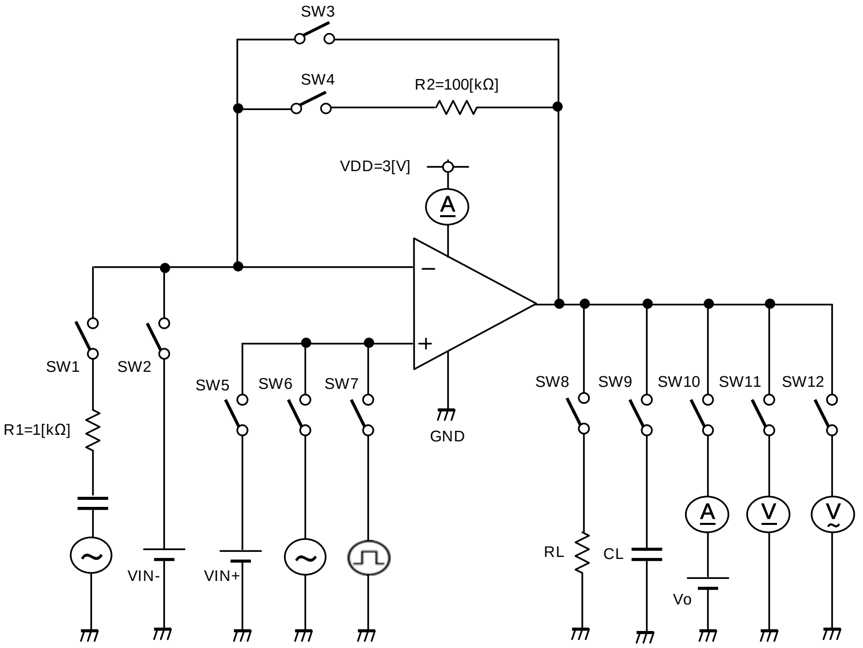


Fig.164 Test circuit 2

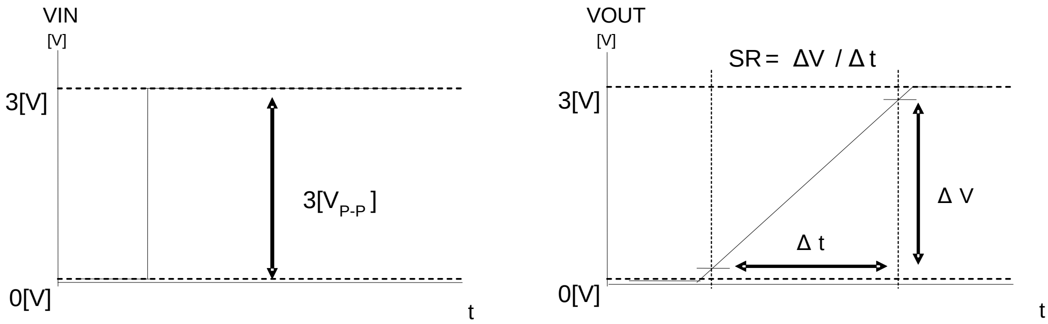


Fig.165 Slew rate input output wave
(Input-Output Full Swing BU7261/BU7271/BU7205/BU7245 family)

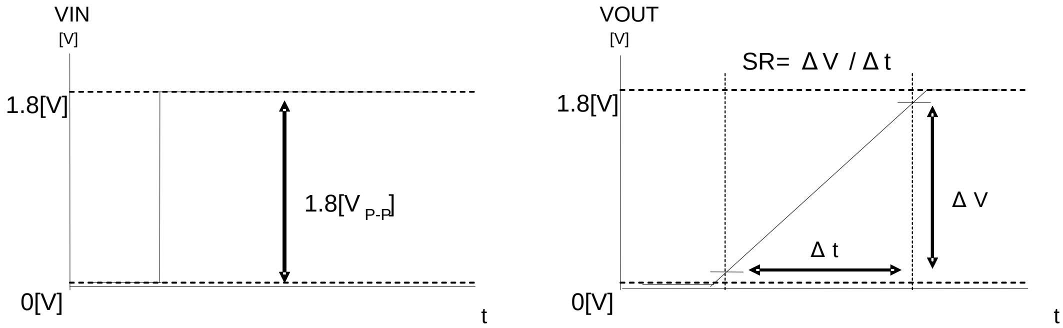


Fig.166 Slew rate input output wave
(Ground Sense BU7411/BU7421/BU7475 family)

●Examples of circuit

○Voltage follower

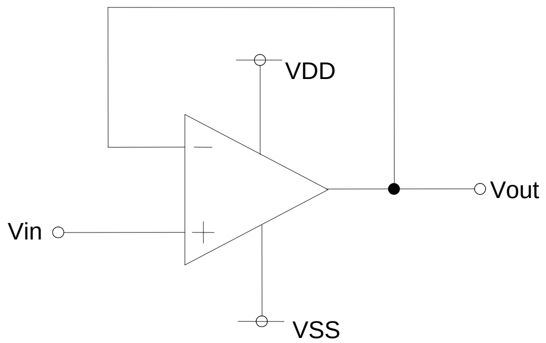


Fig.167 voltage follower circuit

Voltage gain is 0 [dB].
This circuit controls output voltage (Vout) equal input voltage (Vin), and keeps Vout with stable because of high input impedance and low output impedance.
Vout is shown next formula.

Vout=Vin

○Inverting amplifier

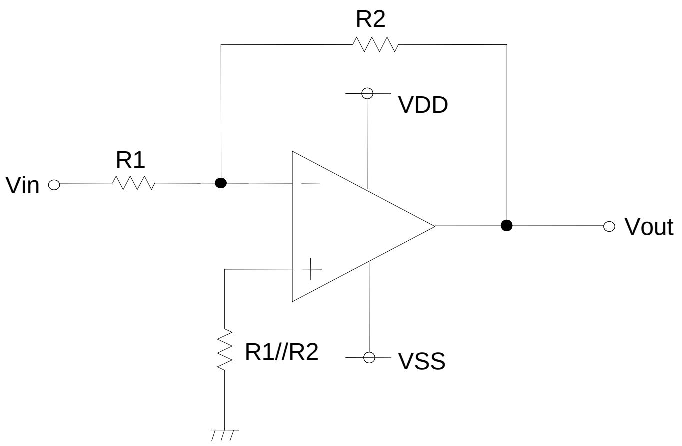


Fig.168 Inverting amplifier circuit

For inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase reversed voltage is outputed. Vout is shown next formula.

Vout=-(R2/R1)・Vin

Input impedance is R1.

○Non-inverting amplifier

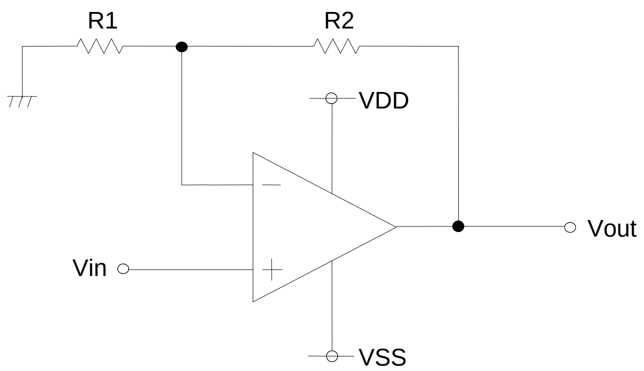


Fig.169 Non-inverting amplifier circuit

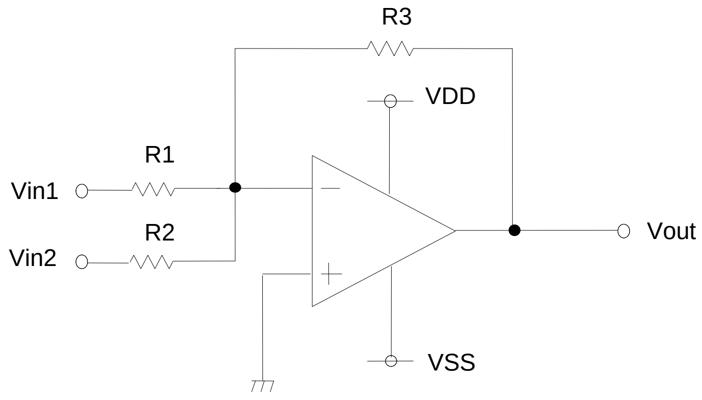
For non-inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase is same with Vin. Vout is shown next formula.

Vout=(1+R2/R1)・Vin

This circuit realizes high input impedance because Input impedance is operational amplifier’s input Impedance.

●Examples of circuit

○Adder circuit



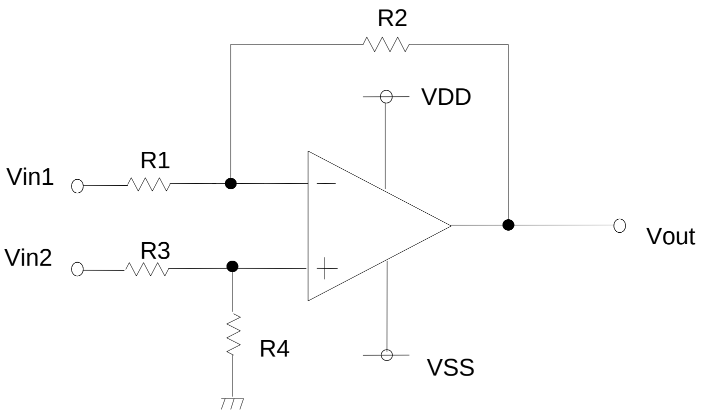
Adder circuit output the voltage that added up Input voltage. A phase of the output voltage turns orver, because non-inverting circuit is used.
Vout is shown next formula.

Vout = -R3(Vin1/R1+Vin2/R2)

When three input voltage is as above, it connects with input through resistance like R1 and R2.

Fig.170 Adder circuit

○Differential amplifier



Differential amplifier output the voltage that amplified a difference of input voltage.
In the case of R1=R3=Ra、R2=R4=Rb
Vout is shown next formula.

Vout = -Rb/Ra(Vin1-Vin2)

Fig.171 Differential amplifier

●Description of electrical characteristics

Described here are the terms of electric characteristics used in this technical note. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings
   Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics

   1.1 Power supply voltage (VDD/VSS)
   Without deterioration or destruction of characteristics of internal circuit.

   1.2 Differential input voltage (Vid)
   Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

   1.3 Input common-mode voltage range (Vicm)
   Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assure normal operation of IC. When normal operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

   1.4 Power dissipation (Pd)
   Indicates the power that can be consumed by specified mounted board at the ambient temperature 25℃(normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package.

2. Electrical characteristics item

   2.1 Input offset voltage (Vio)
   Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 [V].

   2.2 Input offset current (Iio)
   Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

   2.3 Input bias current (Ib)
   Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

   2.4 Circuit current (IDD)
   Indicates the IC current that flows under specified conditions and no-load steady status.

   2.5 High level output voltage / Low level output voltage (VOM)
   Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into high-level output voltage and low-level output voltage. High-level output voltage indicates the upper limit of output voltage. Low-level output voltage indicates the lower limit.

   2.6 Large signal voltage gain (Av)
   Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
   Av = (Output voltage fluctuation) / (Input offset fluctuation)

   2.7 Input common-mode voltage range (Vicm)
   Indicates the input voltage range where IC operates normally.

   2.8 Common-mode rejection ratio (CMRR)
   Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.
   CMRR = (Change of Input common-mode voltage)/(Input offset fluctuation)

   2.9 Power supply rejection ratio (PSRR)
   Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.
   PSRR = (Change of power supply voltage)/(Input offset fluctuation)

   2.10 Channel separation (CS)
   Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

   2.11 Slew rate (SR)
   Indicates the time fluctuation ratio of voltage output when step input signal is applied.

   2.12 Unity gain frequency (ft)
   Indicates a frequency where the voltage gain of Op-Amp is 1.

   2.13 Total harmonic distortion + Noise (THD+N)
   Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

   2.14 Input referred noise voltage (Vn)
   Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

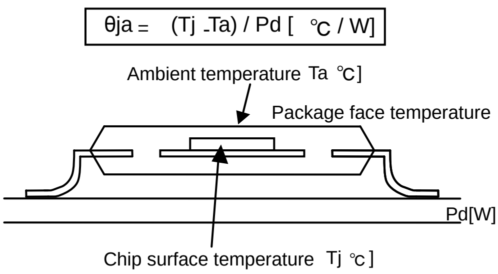
●Derating Curve

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25℃(normal temperature).IC is heated when it consumed power, and the temperature of IC ship becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θj-a[℃/W]. The temperature of IC inside the package can be estimated by this thermal resistance.

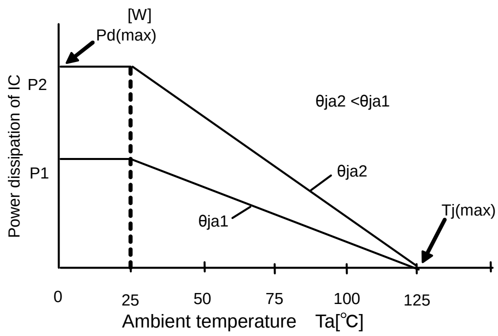
Fig.172 (a) shows the model of thermal resistance of the package. Thermal resistance θja, ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below:

θja = (Tj－Ta) / Pd [℃/W] ・・・・・ (Ⅰ)

Derating curve in Fig.172 (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θja. Thermal resistance θja depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig.173(c)-(d) show a derating curve for an example of BU7265 / BU7205 / BU7271 / BU7245 / BU7411 / BU7421 / BU7475 family.

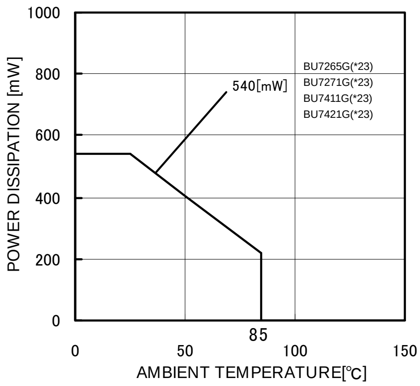


(a) Thermal resistance

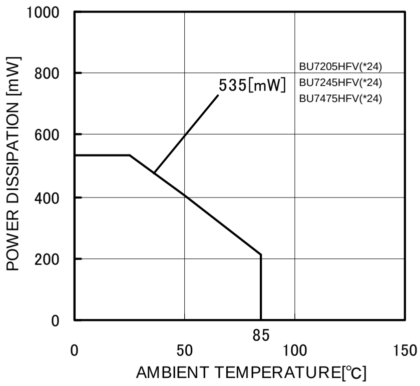


(b) Derating curve

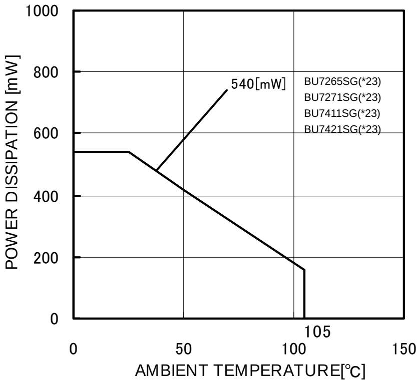
Fig.172 Thermal resistance and derating



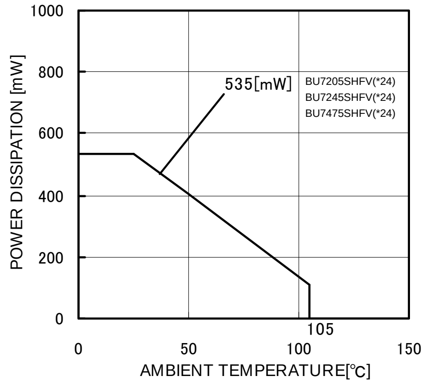
(c) BU7265G BU7271G BU7411G BU7421G



(d) BU7205HFV BU7245HFV BU7475HFV



(e) BU7265SG BU7271SG BU7411SG BU7421SG



(f) BU7205SHFV BU7245SHFV BU7475SHFV

(*23)	(*24)	Unit
5.4	5.35	[mW/℃]

When using the unit above Ta=25[℃], subtract the value above per degree[℃]. Permissible dissipation is the value when FR4 glass epoxy board 70[mm]×70[mm]×1.6[mm] (cooper foil area below 3[%]) is mounted

Fig.173 Derating Curve

●Notes for Use

1) Absolute maximum ratings
Absolute maximum ratings are the values which indicate the limits,within which the given voltage range can be safely charged to the terminal.However, it does not guarantee the circuit operation.

2) Applied voltage to the input terminal
For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage VDD+0.3[V]. Then, regardless of power supply voltage,VSS-0.3[V] can be applied to input terminals without deterioration or destruction of its characteristics.

3) Operating power supply (split power supply/single power supply)
The operational amplifier operates if a given level of voltage is applied between VDD and VSS. Therefore, the operational amplifier can be operated under single power supply or split power supply.

4) Power dissipation (Pd)
If the IC is used under excessive power dissipation. An increase in the chip temperature will cause deterioration of the radical characteristics of IC. For example, reduction of current capability.Take consideration of the effective power dissipation and thermal design with a sufficient margin. Pd is reference to the provided power dissipation curve.

5) Short circuits between pins and incorrect mounting
Short circuits between pins and incorrect mounting when mounting the IC on a printed circuits board, take notice of the direction and positioning of the IC.If IC is mounted erroneously, It may be damaged. Also, when a foreign object is inserted between output, between output and VDD terminal or VSS terminal which causes short circuit, the IC may be damaged.

6) Output short circuit
If short circuit occurs between the output terminal and VDD terminal , excessive in output current may flow and generate heat , causing destruction of the IC.Take due care.

7) Using under strong electromagnetic field
Be careful when using the IC under strong electromagnetic field because it may malfunction.

8) Usage of IC
When stress is applied to the IC through warp of the printed circuit board, The characteristics may fluctuate due to the piezo effect. Be careful of the warp of the printed circuit board.

9) Testing IC on the set board
When testing IC on the set board, in cases where the capacitor is connected to the low impedance, make sure to discharge per fabrication because there is a possibility that IC may be damaged by stress.When removing IC from the set board, it is essential to cut supply voltage. As a countermeasure against the static electricity, observe proper grounding during fabrication process and take due care when carrying and storage it.

10) The IC destruction caused by capacitive load
The transistors in circuits may be damaged when VDD terminal and VSS terminal is shorted with the charged output terminal capacitor.When IC is used as a operational amplifier or as an application circuit, where oscillation is not activated by an output capacitor,the output capacitor must be kept below 0.1[μF] in order to prevent the damage mentioned above.

11) Decupling capacitor
Insert the decupling capacitance between VDD and VSS, for stable operation of operational amplifier.

12) Latch up
Be careful of input voltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up operation. And protect the IC from abnormaly noise.

13) Crossover distortion
Inverting amplifier generates crossover distortion when feed back resistance value is small. To suppress the crossover distortion, connect a resistor between the output terminal and VSS Then increse the bias current to enable class A output stage operation.

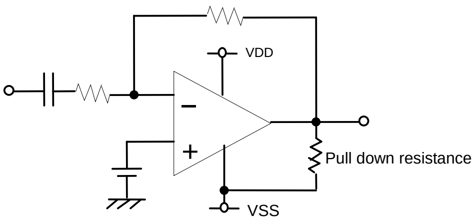


Fig.174 Pull down resistance

●Ordering Part Number

B	U		7	2	6	5	S		H	F	V	-	T	R

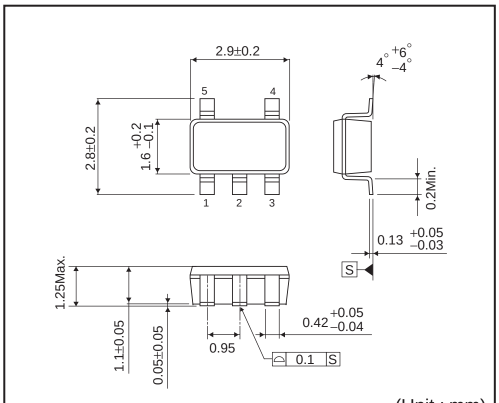
Part No.
BU

Part No.
・7265 7265S ・7411 7411S
・7271 7271S ・7421 7421S
・7205 7205S ・7475 7475S
・7245 7245S

Package
G :SSOP5
HFV :HVSOF5

Packaging and forming specification
TR: Embossed tape and reel

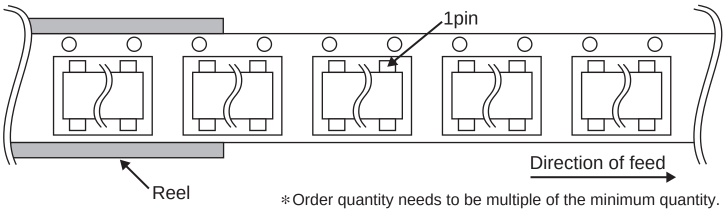
SSOP5



(Unit : mm)

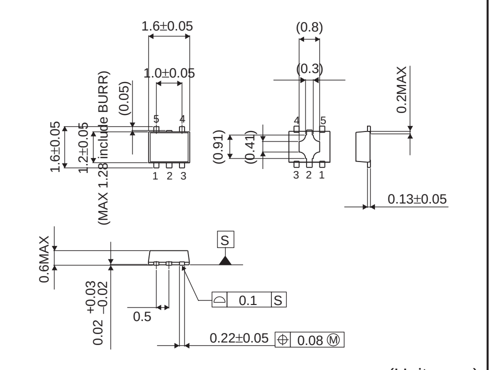
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

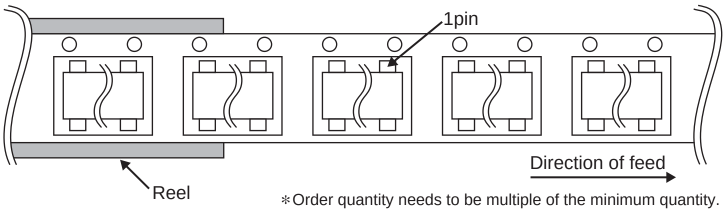
HVSOF5



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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