

*VMTA*

## TABLE OF CONTENTS

### GENERAL INFORMATION/CROSS REFERENCES

A

DISCRETES	1
DIGITAL	2
ANALOG SWITCHES AND MULTIPLEXERS	3
DATA ACQUISITION	4
LINEAR	5
TIMERS, COUNTERS, AND DISPLAY DRIVERS	6
CONSUMER CIRCUITS	7

### APPENDICES/PHYSICAL DIMENSIONS

B

## ENGINEERING SOLUTIONS ON A CHIP FROM INTERSIL

*Product offerings described in this data book reflect Intersil's commitment to industry leadership as a producer of advanced low-power analog and digital semiconductor components and data acquisition systems.*

*These components are fabricated using a wide variety of process technologies and are intended to provide state-of-the-art performance and maximum cost effectiveness.*

*Product areas in which Intersil demonstrates its innovative approach to providing engineering solutions on a chip include:*

- **FIELD EFFECT AND DUAL MATCHED BIPOLAR TRANSISTORS**

A complete line of high-performance junction FETs, dual JFETs, MOSFETs and matched dual bipolar devices.

- **DIGITAL**

Very low-power CMOS ROMs and EPROMs, as well as high-speed HMOS ROMs; CMOS microprocessors, peripherals and UARTs.

- **ANALOG SWITCHES AND MULTIPLEXERS**

The industry's broadest offering of highest-performance switches, including a video-RF switch with excellent isolation at 100 MHz, and multiplexers featuring the least error as well as unprecedented input overload protection.

- **ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS**

3½- and 4½-digit display output (DVM) analog-to-digital converters; 12-, 14- and 16-bit microprocessor-compatible analog-to-digital converters; and high-speed precision digital-to-analog converters up to 14 bits.

- **LINEAR**

A new set of low-power devices with unequalled performance—1- $\mu$ V offset voltage op amps, 4- $\mu$ A quiescent current regulators and supply monitors, 95-per-cent-efficient voltage converters and 1ppm/ $^{\circ}$ C voltage references; a complete family of CMOS op amps; and a wide variety of special analog function circuits.

- **TIMERS, COUNTERS AND DISPLAY DRIVERS**

A wide range of low-power counters, timers and multidigit LED, LCD and vacuum fluorescent display decoder/drivers, including those with full alphanumeric capability.

# General Information

	Page
<b>Explanation of Terms, Indices, and Special Subsections</b>	A-2
<b>Alphanumeric Index</b>	A-3
<b>Base Number Index</b>	A-5
<b>Functional Index</b>	A-7
<b>Obsolete Products List</b>	A-9
<b>IC Alternate Source Index</b>	A-10
<b>Discrete Cross Reference</b>	A-13
<b>Analog Switch Cross Reference</b>	A-21
<b>Data Acquisition Cross Reference</b>	A-23
<b>Watch &amp; Clock Cross Reference</b>	A-24
<b>Linear Cross Reference</b>	A-25

# **EXPLANATION OF TERMS, INDICES AND SPECIAL SUBSECTIONS**

## **A**

### **PRODUCTION DATA SHEET**

This is a full, final data sheet, and describes a mature product in full production. Although Intersil reserves the right to make changes in specifications contained in these data sheets at any time without notice, such changes are not common and are usually minor, generally relating to yield and processing improvements. These data sheets are not marked; others are marked preliminary.

### **PRELIMINARY DATA SHEET**

A preliminary data sheet is issued in advance of the availability of production samples and generally indicates that at the time of printing, the device had not been fully characterized. In the case of a second-source part, the specifications are already determined, and a "preliminary" designation indicates the anticipated availability of the device.

### **ALPHANUMERIC INDEX**

This part number index is arranged first by alpha sequence, (ie: ADCxxxx, DGxxx, Gxxx, ICLxxxx, ICMxxxx, etc.) then by numeric sequence (ie: LM100, LM101A, LM102, LM105, etc.) and ignoring package/temperature/pin number suffixes. The basic numbering sequence, is sorted by reading the part number characters from left to right. Reading the left character first (which is usually an alpha character), then the next character to the right and so forth.

### **BASE NUMBER INDEX**

If only the basic part number is known, use the Base Number Index as a locator aid. The Base Number Index is organized in numeric sequence (with alpha prefixes appearing in bold type and numeric characters set in medium type). Devices are arranged in this index according to the numeric value of the first digit on the left, then the value of the second digit, then the third, and so on. For example, device number ICM7218 precedes ICL741, no package/temperature/pin number suffixes are included, but these may be obtained from the specific product data sheet.

### **FUNCTION INDEX**

This is an index of Intersil device types categorized by product grouping and function. The first major subsection, DISCRETES, is further subdivided into categories for JFETs and Special Function devices.

All remaining major subsections (ANALOG SWITCHES/MULTIPLEXERS, DATA ACQUISITION, LINEAR, TIMERS/COUNTERS, TIMEKEEPING/DTMF, MEMORIES and MICROPROCESSORS/PERIPHERALS)

are organized alphabetically by function. The Functional Index appears in its entirety in section A, and an appropriate subindex appears at the beginning of each major product section.

### **CROSS-REFERENCE GUIDES**

Two cross-reference guides are provided: one for Discrete Devices and one for Integrated Circuits.

The Discrete Cross-Reference Guide indicates whether Intersil can provide the industry-standard type, or an Intersil preferred part instead.

The IC Alternate Source Cross-Reference Guide lists competitive manufacturer device types for which Intersil makes pin-for-pin replacements. In the left-hand column, the competitive device part number is organized alphabetically by manufacturer. The Intersil pin-for-pin replacement appears in the right hand column.

### **SELECTOR GUIDES**

Selector guide tables appear at the front of each major product category subsection and provides a quick reference of key parameters for devices contained in that section.

### **DEVICE FUNCTION/PACKAGE CODES**

Package dimensions and diagrams explaining device prefix and suffix codes appear in Appendix B.

### **DIE SELECTION CRITERIA**

Many of Intersil's semiconductor products are available in die form. This subsection of Appendix B contains general information on criteria for transistor and integrated circuit die selection, including physical parameters, packaging for shipment, assembly, testing and purchase options.

### **HIGH-RELIABILITY PROCESSING**

This subsection of Appendix B defines Intersil's commitment to 100 percent compliance with MIL-STD-883, MIL-STD-750, MIL-M-38510 and MIL-S-19500 specifications. It also outlines Intersil's programs for quality conformance, quality testing and limited use qualification and includes a glossary of military/aerospace Hi-Rel terms.

Intersil reserves the right to make changes in circuitry or specifications contained herein at any time without notice.

Intersil assumes no responsibility for the use of any circuits described herein and makes no representations that they are free patent infringement.

**LIFE SUPPORT POLICY. INTERSIL'S PRODUCTS ARE NOT AUTHORIZED, NOR WARRANTED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES AND/OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF INTERSIL, INC.**

For the purposes of this policy, critical components in life support systems and/or devices are defined as:

1. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
2. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

Intersil cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in an Intersil product. No circuit patent licenses are implied. Intersil reserves the right to change the circuitry and specifications without notice at any time.

# ALPHANUMERIC INDEX

TYPE #	PAGE	TYPE #	PAGE	TYPE #	PAGE	TYPE #	PAGE
2N2607	1-9	2N5115	1-37	3N173	1-60	ICH8500	5-208
2N2608	1-9	2N5116	1-37	3N188	1-61	ICH8510	5-214
2N2609	1-9	2N5117	1-39	3N189	1-61	ICH8515	5-222
2N3684	1-10	2N5118	1-39	3N190	1-61	ICH8520	5-214
2N3685	1-10	2N5119	1-39	3N191	1-61	ICH8530	5-214
2N3686	1-10	2N5196	1-40	$\mu$ A723	**	ICL101ALN	5-46
2N3687	1-10	2N5197	1-40	$\mu$ A733	**	ICL108ALN	5-46
2N3810	1-11	2N5198	1-40	$\mu$ A740	**	ICL301ALN	5-46
2N3811	1-11	2N5199	1-40	$\mu$ A741	**	ICL308LN	5-46
2N3821	1-13	2N5397	1-41	$\mu$ A748	**	ICL7104	4-166
2N3822	1-13	2N5398	1-41	$\mu$ A777	5-49	ICL7106	4-20
2N3823	1-14	2N5432	1-42	AD503	**	ICL7107	4-20
2N3824	1-15	2N5433	1-42	AD590	5-28	ICL7109	4-30
2N3921	1-16	2N5434	1-42	AD741K	**	ICL7115	4-46
2N3922	1-16	2N5452	1-43	AD7520	4-138	ICL7116	4-59
2N3964	1-17	2N5453	1-43	AD7521	4-138	ICL7117	4-59
2N3955	1-17	2N5454	1-43	AD7523	4-144	ICL7126	4-67
2N3956	1-17	2N5457	1-44	AD7530	4-138	ICL7129	4-75
2N3957	1-17	2N5458A	1-44	AD7531	4-138	ICL7134	4-86
2N3958	1-17	2N5459	1-44	AD7533	4-148	ICL7135	4-98
2N3970	1-18	2N5460	1-45	AD7541	4-152	ICL7136	4-108
2N3971	1-18	2N5461	1-45	ADC0801	4-4	ICL7137	4-116
2N3972	1-18	2N5462	1-45	ADC0802	4-4	ICL7145	4-124
2N3993	1-19	2N5463	1-45	ADC0803	4-4	ICL7146	4-132
2N3994	1-19	2N5464	1-45	ADC0804	4-4	ICL741HS	5-44
2N4044	1-20	2N5465	1-45	D123	3-9	ICL741LN	5-46
2N4045	1-20	2N5484	1-46	D125	3-9	ICL7605	5-63
2N4091	1-22	2N5485	1-46	D129	3-13	ICL7606	5-63
2N4092	1-22	2N5486	1-46	DG118	3-6	ICL7611	5-73
2N4093	1-22	2N5515	1-47	DG123	3-6	ICL7612	5-73
2N4100	1-23	2N5516	1-47	DG125	3-6	ICL7613	5-73
2N4117	1-25	2N5517	1-47	DG139	3-15	ICL7614	5-73
2N4118	1-25	2N5518	1-47	DG142	3-15	ICL7615	5-73
2N4119	1-25	2N5519	1-47	DG143	3-15	ICL7621	5-73
2N4220	1-26	2N5520	1-47	DG144	3-15	ICL7622	5-73
2N4221	1-26	2N5521	1-47	DG145	3-15	ICL7631	5-73
2N4222	1-26	2N5522	1-47	DG146	3-15	ICL7632	5-73
2N4223	1-27	2N5523	1-47	DG161	3-15	ICL7641	5-73
2N4224	1-27	2N5524	1-47	DG162	3-15	ICL7642	5-73
2N4338	1-28	2N5638	1-49	DG163	3-15	ICL7650	5-88
2N4339	1-28	2N5639	1-49	DG164	3-15	ICL7652	5-96
2N4340	1-28	2N5640	1-49	DG180	3-19	ICL7660	5-104
2N4341	1-28	2N5902	1-50	DG181	3-19	ICL7663	5-111
2N4351	1-29	2N5903	1-50	DG182	3-19	ICL7664	5-111
2N4391	1-30	2N5904	1-50	DG183	3-19	ICL7665	5-121
2N4392	1-30	2N5905	1-50	DG184	3-19	ICL7667	5-128
2N4393	1-30	2N5906	1-50	DG185	3-19	ICL8001	5-135
2N4416	1-31	2N5907	1-50	DG186	3-19	ICL8007	5-139
2N4856	1-32	2N5908	1-50	DG187	3-19	ICL8008	5-142
2N4857	1-32	2N5909	1-50	DG188	3-19	ICL8013	5-144
2N4858	1-32	2N5911	1-51	DG189	3-19	ICL8017	5-151
2N4859	1-32	2N5912	1-51	DG190	3-19	ICL8018A	4-158
2N4860	1-32	2N6483	1-52	DG191	3-19	ICL8019A	4-158
2N4861	1-32	2N6484	1-52	DG200	3-28	ICL8020A	4-158
2N4867	1-33	2N6485	1-52	DG201	3-32	ICL8021	4-155
2N4868	1-33	3N161	1-56	DGM181	3-23	ICL8022	5-155
2N4869	1-33	3N163	1-57	DGM182	3-23	ICL8023	5-155
2N4878	1-34	3N164	1-57	DGM184	3-23	ICL8038	5-158
2N4879	1-34	3N165	1-58	DGM185	3-23	ICL8043	5-167
2N4880	1-34	3N166	1-58	DGM187	3-23	ICL8048	5-174
2N5018	1-36	3N170	1-59	DGM188	3-23	ICL8049	5-174
2N5019	1-36	3N171	1-59	DGM190	3-23	ICL8052A	4-166
2N5114	1-37	3N172	1-60	DGM191	3-23	ICL8063	5-182

\*\* Obsolete product, refer to page A-9.

# A

## ALPHANUMERIC INDEX

TYPE #	PAGE	TYPE #	PAGE	TYPE #	PAGE	TYPE #	PAGE
ICL8068	4-166	IH5017	3-36	IM6654	2-11	LH2308	5-55
ICL8069	5-190	IH5018	3-36	IM7332	2-18	LH2310	**
ICL8075	5-192	IH5019	3-36	IM7364	2-21	LH2311	**
ICL8076	5-192	IH5020	3-36	IM82C43	2-24	LM100	**
ICL8077	5-192	IH5021	3-36	IMF6485	1-54	LM101A	**
ICL8078	5-192	IH5022	3-36	IT100	1-64	LM102	**
ICL8079	5-192	IH5023	3-36	IT101	1-64	LM105	**
ICL8211	5-198	IH5024	3-36	IT120	1-65	LM107	**
ICL8212	5-198	IH5025	3-41	IT121	1-65	LM108	5-24
ICM1115	7-19	IH5026	3-41	IT122	1-65	LM110	**
ICM7038	7-5	IH5027	3-41	IT124	1-66	LM111	**
ICM7045	7-10	IH5028	3-41	IT126	1-67	LM114	1-83
ICM7050	7-19	IH5029	3-41	IT127	1-67	LM300	**
ICM7051	7-23	IH5030	3-41	IT128	1-67	LM301A	**
ICM7070	7-27	IH5031	3-41	IT129	1-67	LM302	**
ICM7201	**	IH5032	3-41	IT130	1-68	LM305	**
ICM7206	7-31	IH5034	3-41	IT131	1-68	LM307	**
ICM7207	6-3	IH5035	3-41	IT132	1-68	LM308	5-24
ICM7207A	6-3	IH5036	3-41	IT136	1-69	LM310	**
ICM7208	6-7	IH5037	3-41	IT137	1-69	LM311	**
ICM7209	7-39	IH5038	3-41	IT138	1-69	LM4250	**
ICM7211	6-14	IH5040	3-48	IT139	1-69	M116	1-84
ICM7212	6-14	IH5041	3-48	IT1700	1-75	NE536	**
ICM7213	7-42	IH5042	3-48	IT1750	1-76	NE/SE592	5-38
ICM7215	7-47	IH5043	3-48	IT500	1-71	NE592-8	5-41
ICM7216	6-24	IH5044	3-48	IT501	1-71	OP05	5-8
ICM7217	6-39	IH5045	3-48	IT502	1-71	OP07	5-16
ICM7218	6-55	IH5046	3-48	IT503	1-71	SU536	**
ICM7223	7-53	IH5047	3-48	IT504	1-71	U1897	1-92
ICM7223A	7-59	IH5048	3-48	IT505	1-71	U1898	1-92
ICM7223VF	7-67	IH5049	3-48	IT550	1-74	U1899	1-92
ICM7224	6-64	IH5050	3-48	IT5911	1-51	U200	1-85
ICM7225	6-64	IH5051	3-48	IT5912	1-51	U201	1-85
ICM7226	6-72	IH5052	3-56	ITE4091	1-22	U202	1-85
ICM7227	6-39	IH5053	3-56	ITE4092	1-22	U231	1-86
ICM7231	6-84	IH5101	**	ITE4093	1-22	U232	1-86
ICM7232	6-84	IH5108	3-63	ITE4391	1-30	U233	1-86
ICM7233	6-84	IH5110	5-57	ITE4392	1-30	U234	1-86
ICM7234	6-84	IH5111	5-57	ITE4393	1-30	U235	1-86
ICM7235	6-104	IH5112	5-57	ITE4416	1-31	U257	1-87
ICM7236	6-110	IH5113	5-57	J105	1-77	U304	1-88
ICM7240	6-116	IH5114	5-57	J106	1-77	U305	1-88
ICM7241	7-75	IH5115	5-57	J107	1-77	U306	1-88
ICM7242	6-127	IH5140	3-71	J111	1-78	U308	1-89
ICM7243	6-133	IH5141	3-71	J112	1-78	U309	1-89
ICM7245	7-77	IH5142	3-71	J113	1-78	U310	1-89
ICM7250	6-116	IH5143	3-71	J174	1-79	U401	1-90
ICM7260	6-116	IH5144	3-71	J175	1-79	U402	1-90
ICM7281	6-143	IH5145	3-71	J176	1-79	U403	1-90
ICM7555	6-155	IH5200	3-28	J177	1-79	U404	1-90
ICM7556	6-155	IH5201	3-32	J201	1-80	U405	1-90
ID100	1-62	IH5208	3-79	J202	1-80	U406	1-90
ID101	1-62	IH5341	3-87	J203	1-80	VCR2N	1-92
IGC10000	2-34	IH6108	3-93	J204	1-80	VCR3P	1-92
IH5009	3-36	IH6116	3-99	J308	1-82	VCR4N	1-92
IH5010	3-36	IH6201	3-105	J309	1-82	VCR7N	1-92
IH5011	3-36	IH6208	3-109	J310	1-82		
IH5012	3-36	IH6216	3-115	LH0042	**		
IH5013	3-36	IM6402	23	LH2101A	**		
IH5014	3-36	IM6403	23	LH2108	5-55		
IH5015	3-36	IM6653	2-11	LH2110	**		
IH5016	3-36			LH2111	**		
				LH2301A	**		

\*\*Obsolete product, refer to page A-9.

# BASE NUMBER INDEX

TYPE #	PAGE	TYPE #	PAGE	TYPE #	PAGE	TYPE #	PAGE
LH 0042	**	DG 164	3-15	U 257	1-87	2N 4118	1-25
OP 05	5-8	3N 165	1-58	2N 2607	1-9	2N 4119	1-25
OP 07	5-16	3N 166	1-58	2N 2608	1-9	2N 4220	1-26
ADC 0801	4-4	3N 170	1-59	2N 2609	1-9	2N 4221	1-26
ADC 0802	4-4	IT 1700	1-75	VCR 3P	1-92	2N 4222	1-26
ADC 0803	4-4	3N 171	1-59	LM 300	**	2N 4223	1-27
ADC 0804	4-4	3N 172	1-60	LM 301A	**	2N 4224	1-27
ID 100	1-62	3N 173	1-60	ICL 301ALN	5-46	LM 4250	**
IT 100	1-64	J 174	1-79	LM 302	**	2N 4338	1-28
LM 100	**	J 175	1-79	U 304	1-88	2N 4339	1-28
ICL 101ALN	5-46	IT 1750	1-76	LM 305	**	2N 4340	1-28
ID 101	1-62	J 176	1-79	U 305	1-88	2N 4341	1-28
IT 101	1-64	J 177	1-79	U 306	1-88	2N 4351	1-29
LM 101A	**	DG 180	3-19	LM 307	**	2N 4391	1-30
LM 102	**	DG 181	3-19	ICL 308LN	5-46	ITE 4391	1-30
J 105	1-77	DGM 181	3-23	J 308	1-82	2N 4392	1-30
LM 105	**	DG 182	3-19	LM 308	5-24	ITE 4392	1-30
J 106	1-77	DGM 182	3-23	U 308	1-89	2N 4393	1-30
J 107	1-77	DG 183	3-19	J 309	1-82	ITE 4393	1-30
LM 107	**	DG 184	3-19	U 309	1-89	2N 4416	1-31
ICL 108ALN	5-46	DGM 184	3-23	J 310	1-82	ITE 4416	1-31
LM 108	5-24	DG 185	3-19	LM 310	**	2N 4856	1-32
LM 110	**	DGM 185	3-23	U 310	1-89	2N 4857	1-32
J 111	1-78	DG 186	3-19	LM 311	**	2N 4858	1-32
LM 111	**	DG 187	3-19	2N 3684	1-10	2N 4859	1-32
ICM 1115	7-19	DGM 187	3-23	2N 3685	1-10	2N 4860	1-32
J 112	1-78	3N 188	1-61	2N 3686	1-10	2N 4861	1-32
J 113	1-78	DG 188	3-19	2N 3687	1-10	2N 4867	1-33
LM 114	1-83	DGM 188	3-23	2N 3810	1-11	2N 4868	1-33
M 116	1-84	3N 189	1-61	2N 3811	1-11	2N 4869	1-33
DG 118	3-6	DG 189	3-19	2N 3821	1-13	2N 4878	1-34
IT 120	1-65	U 1897	1-92	2N 3822	1-13	2N 4879	1-34
IT 121	1-65	U 1898	1-92	2N 3823	1-14	2N 4880	1-34
IT 122	1-65	U 1899	1-92	2N 3824	1-15		
D 123	3-9	3N 190	1-61	2N 3921	1-16	IT 500	1-71
DG 123	3-6	DG 190	3-19	2N 3922	1-16	IH 5009	3-36
IT 124	1-66	DGM 190	3-23	2N 3954	1-17	IT 501	1-71
D 125	3-9	3N 191	1-61	2N 3955	1-17	IH 5010	3-36
DG 125	3-6	DG 191	3-19	2N 3956	1-17	IH 5011	3-36
IT 126	1-67	DGM 191	3-23	2N 3957	1-17	IH 5012	3-36
IT 127	1-67	VCR 2N	1-92	2N 3958	1-17	IH 5014	3-36
IT 128	1-67	DG 200	3-28	2N 3970	1-18	IH 5015	3-36
D 129	3-13	U 200	1-85	2N 3971	1-18	IH 5016	3-36
IT 129	1-67	DG 201	3-32	2N 3972	1-18	IH 5017	3-36
IT 130	1-68	J 201	1-80	2N 3993	1-19	2N 5018	1-36
IT 131	1-68	U 201	1-85	2N 3994	1-19	IH 5018	3-36
IT 132	1-68	J 202	1-80	VCR 4N	1-92	2N 5019	1-36
IT 136	1-69	U 202	1-85	U 401	1-90	IH 5019	3-36
IT 137	1-69	J 203	1-80	U 402	1-90	IT 502	1-71
IT 138	1-69	J 204	1-80	U 403	1-90	IH 5020	3-36
IT 139	1-69	LH 2101A	**	U 404	1-90	IH 5021	3-36
DG 139	3-15	LH 2108	5-55	2N 4044	1-20	IH 5022	3-36
DG 142	3-15	LH 2110	**	2N 4045	1-20	IH 5023	3-36
DG 143	3-15	LH 2111	**	U 405	1-90	IH 5024	3-36
DG 144	3-15	LH 2301A	**	U 406	1-90	IH 5025	3-41
DG 145	3-15	LH 2308	5-55	2N 4091	1-22	IH 5026	3-41
DG 146	3-15	U 231	1-86	ITE 4091	1-22	IH 5027	3-41
3N 161	1-56	LH 2310	**	2N 4092	1-22	IH 5028	3-41
DG 161	3-15	LH 2311	**	ITE 4092	1-22	IH 5029	3-41
DG 162	3-15	U 232	1-86	2N 4093	1-22	AD 503	**
3N 163	1-57	U 233	1-86	ITE 4093	1-22	IT 503	1-71
DG 163	3-15	U 234	1-86	2N 4100	1-23		
3N 164	1-57	U 235	1-86	2N 4117	1-25		

\*\* Obsolete product, refer to page A-9.

# A

## BASE NUMBER INDEX

TYPE #	PAGE	TYPE #	PAGE	TYPE #	PAGE	TYPE #	PAGE
IH 5030	3-41	2N 5458	1-44	ICL 7109	4-30	ICM 7555	6-143
IH 5031	3-41	2N 5459	1-44	ICL 7115	4-46	ICM 7556	6-143
IH 5032	3-41	2N 5460	1-45	ICL 7116	4-59	ICL 7605	5-63
IH 5034	3-41	2N 5461	1-45	ICL 7117	4-59	ICL 7606	5-63
IH 5035	3-41	2N 5462	1-45	ICL 7126	4-67	ICL 7611	5-73
IH 5036	3-41	2N 5463	1-45	ICL 7129	4-75	ICL 7612	5-73
IH 5037	3-41	2N 5464	1-45	ICL 7134	4-86	ICL 7613	5-73
IH 5038	3-41	2N 5465	1-45	ICL 7135	4-98	ICL 7614	5-73
IT 504	1-71	2N 5484	1-46	ICL 7136	4-108	ICL 7615	5-73
IH 5040	3-48	2N 5485	1-46	ICL 7137	4-116	ICL 7621	5-73
IH 5041	3-48	2N 5486	1-46	ICL 7145	4-124	ICL 7622	5-73
IH 5042	3-48	IT 550	1-74	ICL 7146	4-132	ICL 7631	5-73
IH 5043	3-48	2N 5515	1-47	ICM 7201	**	ICL 7632	5-73
IH 5044	3-48	2N 5516	1-47	ICM 7206	7-31	ICL 7641	5-73
IH 5045	3-48	2N 5517	1-47	ICM 7207	6-3	ICL 7642	5-73
IH 5046	3-48	2N 5518	1-47	ICM 7207A	6-3	ICL 7650	5-88
IH 5047	3-48	2N 5519	1-47	ICM 7208	6-7	ICL 7652	5-96
IH 5048	3-48	2N 5520	1-47	ICM 7209	7-39	ICL 7660	5-104
IH 5049	3-48	2N 5521	1-47	ICM 7211	6-14	ICL 7663	5-111
IT 505	1-71	2N 5522	1-47	ICM 7212	6-14	ICL 7664	5-111
IH 5050	3-48	2N 5523	1-47	ICM 7213	7-42	ICL 7665	5-121
IH 5051	3-48	2N 5524	1-47	ICM 7215	7-47	ICL 7667	5-128
IH 5052	3-56	2N 5638	1-49	ICM 7216	6-24	$\mu A$ 777	5-49
IH 5053	3-56	2N 5639	1-49	ICM 7217	6-39	ICL 8001	5-135
IH 5101	**	2N 5640	1-49	ICM 7218	6-55	ICL 8007	5-139
IH 5108	3-63	AD 590	5-28	ICM 7223	7-53	ICL 8008	5-142
IH 5110	5-57	2N 5902	1-50	ICM 7223A	7-59	ICL 8013	5-144
IH 5111	5-57	2N 5903	1-50	ICM 7223VF	7-67	ICL 8017	5-151
IH 5112	5-57	2N 5904	1-50	ICM 7224	6-64	ICL 8018A	5-158
IH 5113	5-57	2N 5905	1-50	ICM 7225	6-64	ICL 8019A	5-158
2N 5114	1-37	2N 5906	1-50	ICM 7226	6-72	ICL 8020A	5-158
IH 5114	5-57	2N 5907	1-50	ICM 7227	6-39	ICL 8021	5-155
2N 5115	1-37	2N 5908	1-50	$\mu A$ 723	**	ICL 8022	5-155
IH 5115	5-57	2N 5909	1-50	ICM 7231	6-84	ICL 8023	5-155
2N 5116	1-37	2N 5911	1-51	ICM 7232	6-84	ICL 8038	5-158
2N 5117	1-39	IT 5911	1-51	ICM 7233	6-84	ICL 8043	5-167
2N 5118	1-39	2N 5912	1-51	ICM 7234	6-84	ICL 8048	5-174
2N 5119	1-39	IT 5912	1-51	ICM 7235	6-104	ICL 8049	5-174
IH 5140	3-71	NE/SE 592	5-38	ICM 7236	6-110	ICL 8052A	4-166
IH 5141	3-71	NE 592-8	5-41	ICM 7240	6-116	ICL 8063	5-182
IH 5142	3-71	IH 6108	3-93	ICM 7241	7-75	ICL 8068	4-166
IH 5143	3-71	IH 6116	3-99	ICM 7242	6-127	ICL 8069	5-190
IH 5144	3-71	IH 6201	3-105	ICM 7243	6-133	ICL 8075	5-192
IH 5145	3-71	IH 6208	3-109	ICM 7245	7-77	ICL 8076	5-192
2N 5196	1-40	IH 6216	3-115	ICM 7250	6-116	ICL 8077	5-192
2N 5197	1-40	IM 6402	2-3	ICM 7260	6-116	ICL 8078	5-192
2N 5198	1-40	IM 6403	2-3	ICM 7281	6-143	ICL 8079	5-192
2N 5199	1-40	2N 6483	1-52	$\mu A$ 733	**	IM 82C43	2-24
IH 5200	3-28	2N 6484	1-52	IM 7332	2-18	ICL 8211	5-198
IH 5201	3-32	2N 6485	1-52	IM 7364	2-21	ICL 8212	5-198
IH 5208	3-79	IMF 6485	1-54	$\mu A$ 740	**	ICH 8500	5-208
IH 5341	3-87	IM 6653	2-17	$\mu A$ 741	**	ICH 8510	5-214
NE 536	**	IM 6654	2-17	ICL 741HS	5-44	ICH 8615	5-222
SU 536	**	VCR 7N	1-92	AD 741K	**	ICH 8620	5-214
2N 5397	1-41	ICM 7038	7-5	ICL 741LN	5-46	ICH 8530	5-214
2N 5398	1-41	ICM 7045	7-10	$\mu A$ 748	**	IGC 10000	2-28
2N 5432	1-42	ICM 7050	7-19	AD 7520	4-138		
2N 5433	1-42	ICM 7051	7-23	AD 7521	4-138		
2N 5434	1-42	ICM 7070	7-27	AD 7523	1-144		
2N 5452	1-43	ICL 7104	4-166	AD 7530	4-138		
2N 5453	1-43	ICL 7106	4-20	AD 7531	4-138		
2N 5454	1-43	ICL 7107	4-20	AD 7533	4-148		
2N 5457	1-44			AD 7541	4-152		

\*\*Obsolete product, refer to page A-9.

# FUNCTIONAL INDEX

A

<b>DISCRETES</b>	2N5452-54 2N5515-24 2N5902-9 2N5911/12 2N6483-85 IMF6485 IT500-5 IT550 IT5911/12 U231-35 U257 U401-6	1-43 1-47 1-50 1-51 1-52 1-54 1-71 1-74 1-51 1-86 1-87 1-90	<b>DIGITAL</b>	<b>Video/RF Switch</b>
<b>JFET Single Switches</b>			<b>Memory</b>	IH5341 3-87
N-Channel	Page		NMOS ROMs	
2N3970-72	1-18		IM7332 2-18	
2N4091-93	1-22		IM7364 2-21	
2N4391-93	1-30		<b>CMOS EPROMs</b>	
2N4856-61	1-32		IM6653/4 2-11	
2N5432-34	1-42		<b>Gate Arrays</b>	
2N5638-40	1-49		IGC10000 2-28	
ITE4091-3	1-22		<b>Peripherals</b>	
ITE4391-3	1-30		IM6402/3 2-3	
J105-7	1-77		IM82C43 2-24	
J111-13	1-78		<b>ANALOG SWITCHES AND MULTIPLEXERS</b>	
U200-2	1-85		<b>Multiplexers</b>	
U1897-99	1-92		IH5108 3-63	
P-Channel			IH5208 3-79	
2N3993/4	1-19		IH6108 3-93	
2N5018/19	1-36		IH6116 3-99	
2N5114-16	1-37		IH6208 3-109	
IT100/1	1-64		IH6216 3-115	
J174-77	1-79		<b>Analog Switch Drivers/ Level Translators</b>	
<b>JFET Single Amplifiers</b>			D123/125 3-9	
N-Channel			D129 3-13	
2N3684-87	1-10		IH6201 3-105	
2N3821/22	1-13		<b>Analog Switches with Drivers</b>	
2N3823	1-14		DG118/123/125 3-6	
2N3824	1-15		DG139A Family 3-15	
2N4117-19	1-25		DG180 Family 3-19	
2N4220-22	1-26		DGM181 Family 3-23	
2N4223/24	1-27		DG200 3-28	
2N4338-41	1-28		DG201 3-32	
2N4416	1-31		IH5009-24 3-36	
2N4867-69	1-33		IH5025-38 3-41	
2N5397/98	1-41		IH5040-51 3-48	
2N5457-59	1-44		IH5052/3 3-56	
2N5484-86	1-46		IH5140-45 3-71	
ITE4416	1-31		IH5200 3-28	
J201-4	1-80		IH5201 3-32	
J308-10	1-82			
U308-10	1-89			
P-Channel				
2N2607-9	1-9			
2N5460-65	1-45			
U304-6	1-88			
<b>JFET Dual Amplifiers</b>				
N-Channel				
2N3921/22	1-16			
2N3954-58	1-17			
2N5196-99	1-40			

**A****FUNCTIONAL INDEX****Operational, FET Input**

LH0042	**
AD503	**
SU/NE536	**
$\mu$ A740	**
ICL8007	5-139
ICL8043	5-167
ICH8500	5-208

**Operational, General Purpose**

OP-05	5-8
OP-07	5-16
LM101/301	**
LM107/307	**
LM108/308	5-24
$\mu$ A741	**
ICL741HS	5-44
AD741K	**
ICL741LN	5-46
$\mu$ A748	**
$\mu$ A777	5-49
LH2101/2301	**
LH2108/2308	5-55
IH5101	**
ICL8008	5-142

**Operational, High Speed**

ICL8017	5-151
---------	-------

**Operational, Low Power**

LM4250	**
ICL76XX Series	5-73
ICL8021-23	5-155

**Video**

$\mu$ A733	**
NE/SE592	5-38
NE592-8	5-41

**Voltage Followers**

LM102/302	**
LM110/310	**
LH2110/2310	**

**Comparators**

Dual	
LH2111/2311	**

**Low Power**

ICL8001	5-135
Precision	

**Sample and Hold**

IH5110-15	5-57
-----------	------

**Temperature Sensor**

AD590	5-28
-------	------

**Voltage Reference**

ICL8069	5-190
ICL8075-9	5-192
ICL8211/12	5-198

**Voltage Regulators**

LM100/300	**
LM105/305	**
$\mu$ A723	**
ICL7663/64	5-111

**Special Function**

Multiplier	
ICL8013	5-144

**Voltage Converter**

ICL7660	5-104
---------	-------

**Waveform Generator**

ICL8038	5-158
---------	-------

**Low Battery Detectors**

*ICM7201	**
ICL7665	5-121
ICL8211/12	5-200

**Dual Power MOS Driver**

ICL7667	5-128
---------	-------

**TIMERS, COUNTERS, AND DISPLAY DRIVERS****Timers**

ICM7240/50/60	6-116
ICM7242	6-127
ICM7555	6-155
ICM7556	6-155

**Counters**

ICM7208	6-7
ICM7216	6-24
ICM7217/27	6-39
ICM7224/25	6-64
ICM7226	6-72
ICM7236	6-110

**Counter Timebase**

ICM7207/A	6-3
-----------	-----

**Display Drivers**

ICM7211/12	6-14
ICM7218	6-55
ICM7231-34	6-84
ICM7235	6-104
ICM7243	6-133
ICM7281	6-143

**TIMEKEEPING, DTMF CIRCUITS****Stopwatches**

ICM7045	7-10
ICM7215	7-47

**Display Watches/Clocks**

ICM7223	7-53
ICM7223A	7-59
ICM7223VF	7-67

**Analog Watches/Clocks**

ICM1115	7-19
ICM7038	7-5
ICM7050	7-19
ICM7051	7-23
ICM7070	7-27
ICM7245	7-77

**Clock Generators**

ICM7209	7-39
ICM7213	7-42

**Frequency Divider**

ICM7241	7-75
---------	------

**Touch Tone Encoder**

ICM7206	7-31
---------	------

\*\* Obsolete product, refer to page A-9.

## OBSOLETE PRODUCTS

The products listed below have been designed into circuits in the past, but are no longer likely to be the most economic choice for new designs.

These products are still available for use in existing designs. Data sheets for these products are available upon request.

AM2502/3/4	AD503
AM25L02/3/4	SU/NE536
DG126A Family	$\mu$ A740
G115/123	LM101/301
G116-19	LM107/307
G125-32	$\mu$ A741
ICL7600/01	AD741K
ICL8052/7101	$\mu$ A748
ICL8052/71C03	LH2101/2301
ICL8068/71C03	IH5101
ICL8052/53	LM4250
IH401	$\mu$ A733
IMF5911/12	LM102/302
LD110/111	LM110/310
LD114	LH2110/2310
MM450/550	LH2111/2311
MM451/551	LM111/311
MM452/552	LM100/300
MM455/555	LM105/305
VCR5P	$\mu$ A723
LH0042	ICM7201

## **IC ALTERNATIVE SOURCE INDEX**

A

# IC Alternate Source Index (continued)

A

continued

MP7520UD	AD7520UD	AD7531LN (DAC1220LCN)	AD7531LN	<b>NEC</b>	Intersil
MP7521JD	AD7521JD	AD7533AD (DAC1022LCD)	AD7533AD	PD816C	ICM7038
MP7521JN	AD7521JN	AD7533BD (DAC1021LCD)	AD7533BD	PD820C	ICM1115B
MP7521KD	AD7521KD	AD7533CD (DAC1020LCD)	AD7533CD	PD833G	ICM7223
MP7521KN	AD7521KN	AD7533IN (DAC1022LCN)	AD7533IN	PD1963C	ICM7050
MP7521LD	AD7521LD	AD7533KN (DAC1021LCN)	AD7533KN	PD2332	IM7332
MP7521LN	AD7521LN	AD7533LN (DAC1020LCN)	AD7533LN	PD2364	IM7364
MP7521SD	AD7521SD	AD7533SD (DAC1022LD)	AD7533SD		
MP7521TD	AD7521TD	AD7533UD (DAC1020LD)	AD7533UD		
MP7521UD	AD7521UD	AH0139CD	DG139BK		
MP7523JN	AD7523JN	AH0139D	DG139AK		
MP7523KN	AD7523KN	AH0139D/883	DG139AK/883B		
MP7523LN	AD7523LN	AH0142CD	DG142BK		
MP7530JD	AD7530JD	AH0142D/883	DG142AK/883B		
MP7530JN	AD7530JN	AH0143CD	DG143BK		
MP7530KD	AD7530KD	AH0143D	DG143AK		
MP7530KN	AD7530KN	AH0143D/883	DG143AK/883B		
MP7530LD	AD7530LD	AH0144CD	DG144BK		
MP7530LN	AD7530LN	AH0144D	DG144AK		
MP7531JD	AD7531JD	AH0144D/883	DG144AK/883B		
MP7531JN	AD7531JN	AH0145CD	DG145BK		
MP7531KD	AD7531KD	AH0145D	DG145AK		
MP7531KN	AD7531KN	AH0145D/883	DG145AK/883B		
MP7531LD	AD7531LD	AH0146CD	DG146BK		
MP7531LN	AD7531LN	AH0146D	DG146AK		
MP7533AD	AD7533AD	AH0146D/883	DG146AK/883B		
MP7533BD	AD7533BD	AH0161CD	DG161BK		
MP7533CD	AD7533CD	AH0161D	DG161AK		
MP7533JN	AD7533JN	AH0161D/883	DG161AK/883B		
MP7533KN	AD7533KN	AH0162CD	DG162BK		
MP7533LN	AD7533LN	AH0162D	DG162AK		
MP7533SD	AD7533SD	AH0162D/883B	DG162AK/883B		
MP7533TD	AD7533TD	AH0163CD	DG163BK		
MP7533UD	AD7533UD	AH0163	DG163AK		
MP7621AD	AD7541AD	AH0163D/883	DG163AK/883B		
MP7621BD	AD7541BD	AH0164CD	DG164BK		
MP7621JN	AD7541JN	AH0164D	DG164AK		
MP7621KN	AD7541LN	AH0164D/883	DG164AK/883B		
MP7621SD	AD7541SD	AH5009CN	IH5009CPD		
MP7621TD	AD7541TD	AH5010CN	IH5010CPD		
Mitsubishi	Intersil	AH5011CN	IH5011CPD		
M58435P	ICM1115B	AH5012CN	IH5012CPD		
Motorola	Intersil	AH5013CN	IH5013CPD		
LM101	LM101	AH5014CN	IH5014CPD		
LM105	LM105	AH5015CN	IH5015CPD		
LM107	LM107	AM9709CN	IH5009CPD		
LM110	LM110	AM9710CN	IH5009CPD		
LM111	LM111	AM9710CN	IH5010CPD		
LM301	LM301	AM9711CN	IH5011CPD		
LM305	LM305	AM9712CN	IH5012CPD		
LM307	LM307	AM9712CN	IH5012CPD		
LM308	LM308	DM7555	ICM7555		
LM310	LM310	DM7556	ICM7556		
LM311	LM311	LF11201D/883	DG201AK		
MCM68332	IM7332	LF11508D	IH6108MJE		
MCM68364	IM7364	LF11508D/883	IH6108MJE/883B		
MC1723	A723	LF11509D	IH6208MJE		
MC1741	A741	LF11509D/883	IH6208MJE/883B		
MC1748	A748	LF12201	DG201		
MHW590	AD590	LM0042	LH0042		
National Semiconductor	Intersil	LM2108	LH2108		
AD7520JD (DAC1022LCD)	AD7520JD	LM2110	LH2111		
AD7520JN (DAC1022LCN)	AD7520KD	LM2301	LH2301		
AD7520KN (DAC1021LCD)	AD7520KD	LM2308	LH2308		
AD7520KJN (DAC1021LCN)	AD7520KN	LM2310	LH2310		
AD7520LD (DAC1020LCD)	AD7520LD	LM2311	LH2311		
AD7520LN (DAC1020LCN)	AD7520LN	LM100	LM100		
AD7520LN (DAC1020LCN)	AD7520LN	LM101	LM101		
AD7520SK (DAC1022LD)	AD7520SD	LM102	LM102		
AD7520TD (DAC1021LD)	AD7520TD	LM107	LM107		
AD7520UD (DAC1020LD)	AD7520UD	LM108	LM108		
AD7521JD (DAC1222LCD)	AD7521JD	LM110	LM110		
AD7521JN (DAC1222LCN)	AD7521JN	LM111	LM111		
AD7521KD (DAC1221LCD)	AD7521KD	LM300	LM300		
AD7521KN (DAC1221LCN)	AD7521KN	LM301	LM301		
AD7521LD (DAC1220LCD)	AD7521LD	LM302	LM302		
AD7521LN (DAC1220LCN)	AD7521LN	LM305	LM305		
AD7521SD (DAC1222LD)	AD7521SD	LM307	LM307		
AD7521TD (DAC1221LD)	AD7521TD	LM308	LM308		
AD7521UD (DAC1220LD)	AD7521UD	LM310	LM310		
AD7530JD (DAC1022LCD)	AD7530JD	LM311	LM311		
AD7530JN (DAC1022LCN)	AD7530JN	LM4250	LH4250		
AD7530KD (DAC1021LCD)	AD7530KD	LM723	A723		
AD7530KN (DAC1021LCN)	AD7530KN	LM733	A733		
AD7530LD (DAC1020LCD)	AD7530LD	LM740	A740		
AD7530LN (DAC1020LCN)	AD7530LN	LM741	A741		
AD7531JD (DAC1222LCD)	AD7531JD	LM742	A748		
AD7531JN (DAC1222LCN)	AD7531JN	MM52132	IM7332		
AD7531KD (DAC1221LCD)	AD7531KD	MM52164	IM7364		
AD7531KN (DAC1221LCN)	AD7531KN	MM74C946	ICM7224		

# IC Alternate Source Index (continued)

A

continued

Silicon General	Intersil	DG186AP	DG186AK	TI	Intersil
#A777	μA777	DG186BP	DG186BK	μA723	μA723
SG101	LM101	DG187AA	DG187AA	μA733	μA733
SG105	LM105	DG187AL	DG187AL	μA741	μA741
SG107	LM107	DG187AP	DG187AK	μA746	μA748
SG108	LM108	DG187BA	DG187BA	μA777	μA777
SG110	LM110	DG187BP	DG187BK	LM101	LM101
SG111	LM111	DG188AA	DG188AA	LM105	LM105
SG301	LM301	DG188AL	DGM188AA	LM107	LM107
SG305	LM305	DG188AP	DG188AK	LM111	LM111
SG307	LM307	DG188BA	DG188BA	LM301	LM301
SG308	LM308	DGM188BA	DGM188BA	LM305	LM305
SG311	LM311	DG188BP	DG188BK	LM307	LM307
SG4250	LM4250	DG189AL	DG189AL	LM311	LM311
SG723	μA723	DG189AP	DG189AK	SN74S188	DGM182BA
SG733	μA733	DG189BP	DG189BK	TL182CL	DGM182BA
SG741	μA741	DG190AL	DG190AL	TL182CN	DGM182CJ
SG748	μA748	DG190AP	DG190AK	TL182L	DGM182BA
SG7520	AD7520	DG190BP	DG190BK	TL182ML	DGM182CJ
SG7521	AD7521	DG191AL	DGM191AL	TL185CJ	DGM182AA
SG7523	AD7523	DG191AP	DG191AK	TL185J	IH5045CJE
Siliconix	Intersil	DG191BP	DGM191AK	TL185N	IH5045CPE
DF412	ICM7211	DG192AA	DG191BK	TL185M	IH5045MJE
DG123AL	DG123AL	DG200AA	DGM191BK	TL188CL	IH5042CTW
DG123AP	DG123AK	DG200AL	DG200AA	TL188CN	IH5042CPE
DG123BP	DG123BK	DG200AP	DG200AK	TL188L	IH5042CTW
DG125AL	DG125AK	DG200B	DG200BA	TL188IN	IH5042CPE
DG125BP	DG125BK	DG200P	DG200BK	TL188ML	IH5042MTW
DG139AL	DG139AL	DG200CJ	DG200CJ	TL191CJ	IH5043CJE
DG139AP	DG139AK	DG201AP	DG201AK	TL191CN	IH5043CPE
DG139BP	DG139BK	DG201BP	DG201BK	TL191IJ	IH5043CJE
DG142AL	DG142AL	DG201CJ	DG201CJ	TL191IN	IH5043CPE
DG142AP	DG142AK	DG381AA	DGM182AA	TL191MJ	IH5043MJE
DG142BP	DG142BK	DG381AK	DGM182AK	TL503	AD503
DG143AL	DG143AL	DG381AP	DGM182AK	Toshiba	Intersil
DG143AP	DG143AK	DG381BP	DGM182AK	TC8031P	ICM7038A
DG143BP	DG143BK	DG381BA	DGM181BA	TC8051P	ICM7038B
DG144AL	DG144AL	DG381BK	DGM181BK	TC8056PA	ICM1115B
DG144AS	DG144AK	DG381BP	DGM181BK	TC8057P	ICM7038D
DG144AP	DG144BK	DG381CJ	DGM181CJ	TMM2114	IM7332
DG145AL	DG145AL	DG384AK	DGM185AK	TMM2332	IM7364
DG145AE	DG145AK	DG384AP	DGM185AK		
DG145BP	DG145BK	DG384BK	DGM184BK		
DG146AL	DG146AL	DG384BP	DGM184BK		
DG146AP	DG146AK	DG384CJ	DGM184CJ		
DG146BP	DG146BK	DG387AA	DGM188AA		
DG161AL	DG161AL	DG387AK	DGM188AK		
DG161AP	DG161AK	DG387AP	DGM188AK		
DG161BP	DG161BK	DG387BA	DGM187BA		
DG162AL	DG162AL	DG387BK	DGM187BK		
DG162AP	DG162AK	DG387BP	DGM187BK		
DG162BP	DG162BK	DG390AK	DGM191AK		
DG163AL	DG163AL	DG390AK	DGM191AK		
DG163AP	DG163AK	DG390BK	DGM190BK		
DG163BP	DG163BK	DG390BP	DGM190BK		
DG164AL	DG164AL	DG390CJ	DGM190CJ		
DG164AF	DG164AK	DG503	AD503		
DG164BP	DG164BK	DG506AR	IH6116MJ		
DG180AA	DG180AA	DG506BR	IH6116CJI		
DG180AL	DG180AL	DG506CJ	IH6116CPI		
DG180AP	DG180AK	DG507AR	IH6216MJI		
DG180BA	DG180BA	DG507BR	IH6216CII		
DG180BP	DG180BK	DG507CJ	IH6216CPI		
DG181AA	DG181AA	DG508AP	IH6108MJE		
DG181AL	DG181AL	DG508BP	IH6108CJE		
DG181AP	DG181AK	DG508CJ	IH6108CPE		
DG181BA	DG181BA	DG509AP	IH6208MJE		
DG181BP	DG181BK	DG509BP	IH6208CJE		
DG182AA	DG182AA	DG509CJ	IH6208CPE		
DG182AL	DGM182AA	D123AL	D123AL		
DG182AP	DGM182AL	D123AP	D123AK		
DG182BP	DGM182AK	D123BP	D123BK		
DG182BA	DGM182AK	D125AL	D125BJ		
DG182BP	DGM182BA	D125AP	D125AL		
DG183AL	DGM182BK	D125BP	D125AK		
DG183AP	DGM182BK	D125AL	D125BK		
DG183BP	DGM182BK	D125AP	D125BJ		
DG184AL	DGM182BK	D125BP	D125AK		
DG184AP	DGM182BK	D125AL	D125BK		
DG184BP	DGM182BK	D125AP	D125BJ		
DG185AL	DGM185AK	D125BP	D125AK		
DG185BP	DGM185AK	D125AL	D125BK		
DG186AA	DG186AK	UCN4112M	ICM7051A		
DG186AL	DG186AK	UCN4113M	ICM7038B		
DG186AP	DGM185AK	UHP-503	AD503		
DG186BP	DGM185AK	Synertek	Intersil		
DG186BP	DGM185BK	SY2332	Intersil		
DG186BP	DGM185BK	SY2364	Intersil		
DG186AA	DG186AA				
DG186AL	DG186AL				

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
100S 100U 102M 102S 103M	2N5458 2N5684 2N5886 2N5887 2N5889	2N2608 2N2607 2N2608 2N2609 2N2609JAN	2N2607 2N2607 2N2608 2N2609 2N2609JAN	2N3321 2N3322 2N3323 2N3324 2N3325	2N5270 2N5268 IT132 IT132 IT132	2N3914 2N3915 2N3916 2N3917A 2N3917A	IT132 IT132 IT130 IT130 IT130
103S 103M 105M 105U 106M	2N5459 2N5459 2N5886 2N5887 2N5888	2N2609 2N2640 2N2641 2N2642 2N2643	IT120 IT122 IT120 IT120 IT122	2N3326 2N3327 2N3328 2N3329 2N3350	IT132 IT137 IT138 IT139 IT137	2N3917A 2N3919 2N3920 2N3921 2N3922	IT130A 2N5454 2N2609 2N3821 2N3822
107M 110U 120U 125U 1277A	2N5458 2N3685 2N5886 2N4339 2N3922	2N2644 2N2652 2N2652A 2N2720 2N2721	IT120 IT120 IT120 IT120 IT120	2N3351 2N3352 2N3365 2N3366 2N3367	IT138 IT139 2N4340 2N4343 2N4348	2N3923 2N3924 2N3907 2N3908 2N3909	2N3823 2N3824 IT120 IT120 2N2609
1278A *1278A 1280A 1281A 1282A	2N3821 2N3821 2N3824 2N3824 2N4341	2N2622 2N2622 2N2803 2N2804 2N2805	IT120 IT122 IT139 IT139 IT139	2N3368 2N3369 2N3370 2N3375 2N3379	2N4341 2N4348 2N4348 2N2608 2N3409	2N3909A 2N3921 2N3922 2N3922 2N3949 2N3950	2N2609 2N3921 2N3922 2N3922 IT132 IT132
1283A 1284A 1285A 1286A 130U	2N4340 2N4222 2N5821 2N4220 2N3687	2N2606 2N2607 2N2607 2N2607 2N2607	IT139 IT139 IT139 IT139 IT139	2N3380 2N3382 2N3384 2N3386 2N3409	2N2608 2N3994 2N3995 2N3995A IT122	2N3954 2N3954A 2N3955 2N3955A 2N3955	2N3954 2N3954A 2N3955 2N3955A 2N3955
1325A 135U 147 155U 1714A	2N4222 2N4222 2N4224 2N4116 2N4340	2N2644 2N2650 2N2650A 2N2610 2N2913	2N2607 IT120 IT120 IT120 IT122	2N3410 2N3411 2N3423 2N3424 2N3425	IT122 IT122 IT122 IT122 IT122	2N3957 2N3966 2N3957 2N3957A 2N3958	2N3957 2N4416 2N4221 2N4221 2N3685
182S 183S 187S 188S 199S	2N4391 2N3923 2N4338 2N4340 2N4341	2N2914 2N2915 2N2915A 2N2916 2N2916A	IT120 IT120 IT120 IT120 IT120	2N3435 2N3437 2N3438 2N3452 2N3453	2N4341 2N4340 2N4348 2N4220 2N4368	2N3968A 2N3969 2N3969A 2N3970 2N3971	2N3685 2N3685 2N3685 2N3970 2N3971
2000M 2001M 2002 200U 2015	2N3823 2N3823 2N3823 2N3824 2N3911	2N2917 2N2918 2N2919 2N2919A 2N2920	IT120 IT120 IT120 IT120 2N2920	2N3454 2N3455 2N3455 2N3457 2N3458	2N4368 2N4370 2N4370 2N4370 2N4341	2N3972 2N3953 2N3953A 2N3954 2N3954A	2N3972 2N3953 2N3953A 2N3954 2N3954A
202S 203S 204S 2078A 2079A	2N4392 2N3921 2N3921 2N3955 2N3955	2N2920A 2N2935 2N2937 2N2972 2N2973	2N2920 IT120 IT120 IT122 IT122	2N3459 2N3460 2N3513 2N3514 2N3515	2N4339 2N4338 2N4338 2N4220 2N4368	2N4009 2N4010 2N4011 2N4015 2N4016	IT132 IT132 IT132 IT139 IT137
2080A 2081A 2093M 2094M 2095M	2N3955A 2N3955A 2N3687 2N3686 2N3686	2N2974 2N2975 2N2976 2N2977 2N2978	IT120 IT120 IT120 IT120 IT120	2N3516 2N3517 2N3521 2N3522 2N3574	IT122 IT122 IT122 IT122 2N2607	2N4017 2N4018 2N4018 2N4020 2N4021	IT139 IT139 IT139 IT139 IT139
2098A 2099A 210U 2130U 2132U	2N3954 2N3955A 2N4415 2N5452 2N3955	2N2979 2N2980 2N2981 2N2982 2N3043	IT120 IT121 IT122 IT122 IT121	2N3575 2N3578 2N3587 2N3608 2N3680	2N2607 2N2608 IT122 3N172 IT120	2N4022 2N4023 2N4024 2N4025 3N163	IT139 IT137 IT137 IT137 3N163
2134U 2135U 2139U 2139U 2147U	2N3955 2N3957 2N3958 2N3958 2N3958	2N3044 2N3045 2N3050 2N3050 2N3048	IT120 IT120 IT121 IT121 IT120	2N3684 2N3684A 2N3685 2N3685A 2N3688	2N3684 2N3684A 2N3685 2N3685A 2N3688	2N4038 2N4039 2N4039 2N4086 2N4087	2N4351 2N4351 3N163 3N163 3N166
2148U 2149U 2151S 2152S 2153S	2N3958 2N3958 2N3954 2N3955 2N3956	2N3049 2N3050 2N3051 2N3052 2N3059	IT139 IT139 IT139 IT129 IT139	2N3685A 2N3687 2N3687A 2N3726 2N3727	2N3685 2N3687 2N3687 T131 T13D	2N4092 2N4083 2N4084 2N4085 2N4091	2N3954 2N3955 2N3954 2N3955 2N4091
234S 235S 241U 260U 261U	2N3957 2N3958 2N4359 2N4359 2N4359	2N3066 2N3067 2N3068 2N3069 2N3070	2N4340 2N4340 2N4348 2N4348 2N4349	2N3728 2N3728 2N3800 2N3800 2N3801	IT122 IT121 IT132 IT132 IT132	2N4091A 2N4091JAN 2N4091JANTX 2N4091JANTXV 2N4092	2N4091 2N4091JAN 2N4091JANTX 2N4091JANTXV 2N4092
2N2606 2N2606A 2N2606B 2N2223 2N2223A	IT120 IT121 IT121 IT122 IT121	2N3071 2N3084 2N3085 2N3085 2N3087	2N4338 2N4339 2N4339 2N4339 2N4339	2N3803 2N3804 2N3804A 2N3805 2N3805A	IT132 IT130 IT130A IT130 IT130	2N4092A 2N4092JAN 2N4092JANTX 2N4092JANTXV 2N4093	2N4092 2N4092JAN 2N4092JANTX 2N4092JANTXV 2N4093
2N2386 2N2386A 2N2423 2N2423A 2N2480	2N2808 2N2808 IT122 IT121 IT122	2N3058 2N3058A 2N3059 2N3059A 2N3113	2N4339 2N4339 2N4339 2N4339 2N4339	2N3806 2N3807 2N3808 2N3808 2N3807	IT122 IT122 IT122 IT122 2N3810	2N4093A 2N4093JAN 2N4093JANTX 2N4093JANTXV 2N4100	2N4093 2N4093JAN 2N4093JANTX 2N4093JANTXV 2N4100
2N2490A 2N2497 2N2498 2N2500	IT121 2N2608 2N2608 2N2608	2N3277 2N3278 2N3282 2N3303	2N2608 2N2607 2N2607 2N2609	2N3810A 2N3811 2N3811A 2N3812 2N3813	2N3810A 2N3811 2N3811A IT132 IT132	2N4117 2N4117A 2N4118 2N4118A 2N4119	2N4117 2N4117A 2N4118 2N4118A 2N4119

CONSULT FACTORY

# DISCRETE CROSS REFERENCE (cont.)

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
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2N4221 2N4221A 2N4222 2N4222A 2N4223	2N4221 2N4222 2N4222 2N4223	2N5103 2N5104 2N5105 2N5114 2N5114JAN	2N4416 2N4416 2N4416 2N5114 2N5114JAN	2N5517 2N5518 2N5519 2N5520 2N5521	2N5517 2N5518 2N5519 2N5520 2N5521	2N5658 2SC294 2SJ11 2SJ12 2SJ13	2N5432 IT122 2N2607 2N2607 2N2607
2N4224 2N4257 2N4258 2N4302 2N4303	2N4224 3N163 3N161 2N4302 2N5459	2N5114JANTX 2N5114JANTXV 2N5115 2N5115JAN	2N5114JANTX 2N5114JANTXV 2N5115 2N5115JAN	2N5522 2N5523 2N5524 2N5545 2N5546	2N5522 2N5523 2N5524 2N5545 2N555A	2SJ15 2SJ16 2SJ17 2SJ18 2SJ49	2N2607 2N2607 2N2607 2N2607 2N2607
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2N4889A 2N4879 2N4879 2N4879 2N4880 2N4880 2N4887	2N4859A 2N4859 2N4859 2N4859 2N4859 2N4859 IT131	2N5433 2N5434 2N5434 2N5435 2N5435 2N5434	2N5433 2N5434 2N5434 2N5435 2N5435 2N5434	2N5088 2N5089 2N5090 2N5091 2N5092	IT122 IT121 IT121 IT121 IT121 IT121	3N158A 3N160 3N161 3N163 3N164	3N163 3N163 3N163 3N163 3N163
2N4898 2N4899 2N4899 2N4899 2N4899 2N4899 IT132	2N4857 2N4857 2N4857 2N4857 2N4857 2N4857 IT132	2N5457 2N5458 2N5458 2N5459 2N5459 2N5459 IT132	2N5457 2N5458 2N5458 2N5459 2N5459 2N5459 IT132	2N6081 2N6082 2N6083 2N6084 2N6085	IT121 IT121 IT121 IT121 IT122	3N165 3N166 3N167 3N168 3N169	3N165 3N165 3N165 3N165 3N165
2N4938 2N4939 2N4940 2N4941 2N4942	IT132 IT132 IT132 IT131 IT132	2N5457 2N5458 2N5458 2N5460 2N5461	2N5457 2N5458 2N5458 2N5460 2N5461	2N6081 2N6082 2N6083 2N6084 2N6085	IT121 IT121 IT121 IT122 IT122	3N165 3N166 3N167 3N168 3N169	3N165 3N165 3N165 3N165 3N165
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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
SN180 SN181 SN182 SN183 SN188	3N172 3N181 3N181 3N181 3N188	6CY89 BF244 BF244A BF244B BF244C	T122 2N5486 2N5484 2N5485 2N5486	BFX78 BFX82 BFX83 BFX89 BFY20	2N5397 2N5019 2N5019 T120A T122	CML552 CML653 CML657 CML800 CML856	2N5432 2N5433 2N5433 2N5433 2N5433
SN189 SN190 SN191 SN207 SN208	3N189 3N180 3N191 3N190 3N188	BF245 BF245A BF245B BF245C BF246	2N5486 2N4416 2N4415 2N4416 2N5485	BFY81 BFY82 BFY83 BFY84 BFY85	T122 T122 T122 T122 T122	CML820 CMX740 CP540 CP543 CP550	2N4858A 2N4858 2N4853 2N5434 2N5432
SSK22 SSK23 SSK28 2ET 4360TP	2N5486 2N5397 2N5397 2N5482 2N5482	BF246A BF246B BF246C BF247 BF247A	2N5539 2N5538 2N5538 2N4091 2N4091	BFY86 BFY91 BFY92 BN208 BSV22	T122 T122 T122 T122 T122	CP651 CP652 CP653 D1101 D1102	2N5433 2N5433 2N5433 2N3821 2N3821
5033TP 558U 55T 55T 703U	2N5460 2N4416 2N5457 2N4415 2N4220	BF247B BF247C BF255 BF255A BF255B	2N4091 2N4091 2N5484 2N5484 2N4416	BSV78 BSV78 BSV80 BSV80 C21	2N4056A 2N4057A 2N5484 2N5484 C21	D1103 D117 D1178 D1178 D1180	2N4338 2N4321 2N4321 2N4321 2N4322
704U 705U 707U 714U 734EU	2N4220 2N4224 2N4224 2N5822 2N4416	BF256C BF320 BF320A BF320B BF320C	2N4416 2N5451 2N5451 2N5461 2N5462	C2308 C38 C413N C510 C511	2N5196 2N4338 2N4338 2N4343 2N4343	D1181 D1182 D1183 D1184 D1185	2N4338 2N4338 2N4341 2N4340 2N4339
734U 751U 752U 753U 754U	2N5516 2N4340 2N4340 2N4341 2N4340	BF345 BF347 BF348 BF349 BF349	T1E4392 J201 J310 J310 BF301	C612 C613 C614 C615 C620	2N4221 2N4221 2N4220 2N4221 2N4220	D1201 D1202 D1203 D1201 D1392	2N4224 2N4221 2N4220 2N4222 2N4220
755U 756U A180 A181 A182	2N4341 2N4340 2N4340 2N4341 2N4341	BF302 BF304 BF305 BF305 BF308	2N4338 2N4338 2N4859 2N4859 2N4857	C621 C622 C623 C624 C625	2N4220 2N4220 2N4220 2N4220 2N4220	D1303 D1420 D1421 D1422 D272218	2N4220 2N4858 2N3822 2N4859 T129
A183 A194 A195 A196 A197	2N5484 2N5484 2N5484 2N5484 2N4391	BF610 BF611 BF615 BF616 BF617	2N4958 2N4959 2N4959 2N4959 2N4959	C650 C651 C652 C653 C680	2N4220 2N4220 2N4220 2N4220 2N4341	D272218A D272219 D272219A D272204 D27204A	T129 T129 T129 T129 T139
A198 A199 A513821 A513822 A513823	IT4E392 IT4E393 2N5484 2N5484 2N4416	BF618 BF610 BF611 BF612 BF613	2N4958 U401 U401 U402 U403	C6651 C6652 C573 C574 C580	2N4341 2N4339 2N4341 2N4341 2N4338	D27205 D27205A D27318 D102 DA402	T139 T139 T129 T129 2N5196
A5T3824 A5T5480 A5T5481 A5T5482 AD3954	2N4341 2N5480 2N5451 2N5482 2N3954	BF614 BF615 BF616 BF623 BF626	U404 U405 U406 T5912 U403	C680A C681 C681A C682 C682A	2N4338 2N4338 2N4338 2N4338 2N4338	DN3066A DN3067A DN3068A DN3069A DN3070A	2N3821 2N4338 2N4338 2N3822 DN3621
AD3954A AD3955 AD3955 AD3955 AD3955	2N3954A 2N3955 2N3955 2N3955 2N3955	BF6044 BF6045 BFQ49A BFQ49B BFQ49C	T15912 T15912 2N3055 2N3958 2N3958	C683 C683A C684 C684A C685	2N4339 2N4339 2N4220 2N4220 2N4220	DN3071A DN3654A DN3655A DN3656A DN3668A	2N4238 DN4220 DN4220 DN4220 DN4231
AD5506 AD5507 AD5508 AD5509 AD810	2N5906 2N5907 2N5908 2N5909 2N4978	BF521 BF521A BF567 BF567P BF568	2N5193 2N5180 2N5221 C01 2N3823	C685A C690 C691 C692 C695	2N4220 2N4338 2N4338 2N4338 2N4338	DN3367A DN3367B DN3368A DN3369A DN3369A	2N3587 2N4051 2N4341 2N4221 2N4338
AD811 AD812 AD813 AD814 AD815	2N4879 2N4878 2N4879 IT124 IT124	BF568P BF570 BF571 BF572 BF573	2N4416 2N3821 2N3822 2N3923 2N3821	C91 C92 C93 C94 C94E	2N4859 2N4051 2N4383 2N5457 2N5457	DN3359B DN3270A DN3270B DN3435A DN3436B	2N4220 DN4233 DN4233 DN4221 DN4222
AD816 AD818 AD820 AD821 AD822	IT120A T140 T122 T130A T130A	BF574 BF575 BF575 BF577 BF578	2N4225 2N4227 2N4228 2N4229 2N4220	C95 C95E C95E C97E C97E	2N4547 2N4549 2N4549 2N3822 2N3822	DN3437A DN3437B DN3439A DN3439B DN3458A	2N4240 DN4220 DN4220 DN4233 DN4241
AD830 AD831 AD832 AD833 AD833A	2N5520 2N5521 2N5522 2N5523 2N5524	BF579 BF580 BF5710 BF711 BFW10	2N4851 2N4416A 2N5397 2N5019 2N3823	CC4445 CC4446 CB897 CF2386 CF24	2N5432 2N5434 2N4656 2N5458 2N3824	DN3458B DN3459A DN3459B DN3459A DN3460B	2N4222 DN4338 DN4338 DN4220 DN4338
AD835 AD836 AD837 AD838 AD839	2N3954 2N3955 2N3955 2N3955 2N3957	BFW11 BFW12 BFW13 BFW39 BFW39A	2N3822 2N4416B 2N4867 T128 T120	CRM13026 CMB600 CMB601 CMB602 CMB603	2N4858 2N4092 2N4091 2N4091 2N4081	DNX1 DNX2 DNX3 DNX4 DNX5	2N4338 2N4338 2N4338 2N4869 2N4868
AD840 AD841 AD842 BC264 BC264A	2N5520 2N5521 2N5523 2N5456 2N5457	BFW54 BFW55 BFW55 BFW56 BFX11	2N3822 2N3822 2N4860 2N4224 IT132	CMB640 CMB641 CMB642 CMB643 CMB644	2N4083 2N4083 2N4083 2N4082 2N4082	DNX6 DNX7 DNX8 DNX9 DL4339	2N4338 DN4418 2N4418 2N4339 DN5387
BC264B BC264C BC264D BCY87 BCY88	2N5458 2N5458 2N4416 IT121 IT122	BFX15 BFX16 BFX20 BFX71 BFX72	IT122 IT131 IT134 IT120 IT120	CM645 CM645 CM647 CM650 CM651	2N4082 2N4082 2N4081 2N5432 2N5433	DU4340 E100 E101 E102 E103	2N5385 2N5458 2024 2N5457 2N5459

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
E105 E106 E107 E108 E109	J105 J106 J107 J105 J106	FF400 FM1100 FM1100A FM1101A FM1102	2N5457 2N5354A 2N5306 2N5306 2N3554	IT127 IT128 IT129 IT130 IT130A	IT127 IT128 IT129 IT130 IT130A	ITE2977 ITE2978 ITE2979 ITE2965 ITE3057	IT120 IT120 IT120 2N3685 2N3686
E110 E111 E111A E112 E112A	J107 J111 J111 J112 J112	FM1102A FM1103 FM1103A FM1104 FM1104A	2N5906 2N3955 2N5808 2N3957 2N5909	IT131 IT132 IT135 IT137 IT138	IT131 IT132 IT136 IT137 IT138	ITE3068 ITE3347 ITE3348 ITE3349 ITE3350	2N3687 IT137 IT138 IT139 IT137
E113 E113A E114 E117 E174 E175	J113 J113 J204 J174 J175	FM1105 FM1105A FM1106 FM1106A FM1107	2N3564A IT500 2N3564A IT500 2N3564	IT139 IT140 IT1700 IT1701 IT1702	IT139 IT140 IT1700 3N172 3N163	ITE3351 ITE3680 ITE3690 ITE3692 ITE3694	IT138 IT120 IT132 IT132 IT130
E176 E177 E201 E202 E203	J176 J177 J201 J202 J203	FM1107A FM1108 FM1108A FM1109 FM1109A	IT500 IT500 IT502 IT400 IT500	IT1750 IT2700 IT2701 IT400 IT500	IT1750 3N165 3N165 2N4332 IT500	ITE3306 ITE3807 ITE3808 ITE3809 ITE3810	IT132 IT132 IT132 IT132 IT130
E204 E210 E211 E212 E230	J204 2N5397 2N5397 2N5397 2N4867	FM1110 FM1110A FM1111 FM1111A FM1112	2N3955 2N5908 2N3957 2N5909 2N5196	IT500P IT501 IT501P IT502 IT502P	IT500 IT501 IT501P IT502 IT502P	ITE3811 ITE3807 ITE3808 ITE4317 ITE4018	IT130 IT120 IT120 IT120 IT139
E231 E232 E270 E271 E300	2N4868 2N4659 J270 J271 2N5397	FM1200 FM1201 FM1202 FM1203 FM1204	2N3954 2N3954 2N3954 2N3955 2N3955	IT503 IT503P IT504 IT505 IT550	IT503 IT503P IT504 IT505 IT550	ITE4019 ITE4020 ITE4221 ITE4022 ITE4023	IT139 IT139 IT139 IT139 IT137
E304 E305 E308 E309 E310	2N5486 2N5484 J308 J309 J310	FM1205 FM1206 FM1207 FM1208 FM1209	2N3954 2N3954 2N3954 2N3955A 2N3955	IT5911 IT5912 IT2572 IT2573 IT2574	IT5911 IT5912 IT122 IT123 IT120	ITE4024 ITE4025 ITE4091 ITE4092 ITE4093	IT137 IT137 IT132 IT132 IT137
E311 E312 E400 E401 E402	J310 2N5397 2N3955 2N3955 2N3957	FM1210 FM1211 FM3554 FM3554A FM3555	2N3955A IT5911 2N3954 2N3954A 2N3955	IT2975 IT2976 IT2977 IT2978 IT2979	IT120 IT120 T120 IT120 IT120	ITE4117 ITE4118 2N4119 2N4119 2N4339	2N4117 2N4118 2N4119 2N4338 2N4339
E410 E411 E412 E413 E414	2N3955 IT5911 IT5911 2N5454 2N3556	FM3955A FM3956 FM3957 FM3958 FM4339	2N3955A 2N3956 2N3957 2N3958 2N4339	ITC3347 ITC3348 ITC3348 ITC3350 ITC3351	IT137 IT138 IT139 IT137 IT138	ITE4340 ITE4341 ITE4391 ITE4392 ITE4393	2N4340 2N4341 ITE4391 ITE4392 ITE4393
E415 E420 E421 E420 E431	2N3957 IT5911 IT5912 J309(X2) J310(X2)	FP4340 FT0854A FT0854B FT0654C FT0654D	2N4340 2N5486 2N5486 2N4221 2N4221	ITC3652 ITC3600 ITC3602 ITC3604 ITC3606	IT139 IT132 IT132 IT130 IT132	ITE4416 ITE4857 ITE4858 ITE4859 J100	ITE4416 2N4857 2N4858 2N4859 2N5458
ESM25 ESM25A ESM4091 ESM4092 ESM4093	U401 U401 2N4091 2N4092 2N4093	FT3820 FT3820 FT3909 FT703 FT704	2N5019 2N5450 2N5019 3N151 3N163	ITC3807 ITC3808 ITC3608 ITC3610 ITC3611	IT132 IT132 IT132 IT130 IT130	J101 J102 J103 J105 J105-1B	2N4339 2N5457 2N5459 2N5459
ESM4302 ESM4303 ESM4304 ESM4445 ESM4446	2N5457 2N5458 2N5458 2N5432 2N5434	G75457 G75458 G75458 HA7807 HA7809	2N5457 2N5458 2N5458 IT132 IT132	ITC4017 ITC4018 ITC4019 ITC4020 ITC4021	IT139 IT139 IT139 IT139 IT139	J106 J106-1B J107 J107-1B J105	J106 J106 J107 J107 J105
ESM4447 ESM4448 FE0554A FE0554B FE100	2N5432 2N5434 2N4368 2N5485 2N3221	HDI1030 HEPBD1 HEPBD2 HEPBD3 HEPFO021	3N153 2N3822 2N3824 2N3825 2N5484	ITC4022 ITC4023 ITC4024 ITC4025 ITC2453	IT139 IT137 IT137 IT137 IT120	J106-1B J106 J106 J106 J10-1B	J106 J106 J106 J106 J107
FE100A FE102 FE102A FE104 FE104A	2N3821 2N4119 2N4119 2N4118 2N4118	HFP1035 HFP2004 HFP2005 ID100 ID101	J176 2N5484 2N5485 ID100 ID101	IT28289 IT28240 IT26451 IT26452 IT26503	IT120 IT122 IT122 IT120 IT122	J111 J111-1B J111A J111A-1B J112	J111 J111 J111 J111 J112
FE1800 FE200 FE202 FE204 FE300	2N4092 2N3921 2N3921 2N3921 2N3922	IMF3954 IMF3954A IMF3955 IMF3955A IMF3956	2N3954 2N3954A 2N3955 2N3955A 2N3955	IT2644 IT2720 IT2721 IT2722 IT26503	IT122 IT120 IT122 IT120 IT122	J112-1B J112A J112A-1B J113 J113-1B	J112 J112 J112 J113 J113
FE202 FE304 FE3819 FE4302 FE4303	2N3921 2N3821 2N5454 2N5457 2N5458	IMF3957 IMF3958 IMF5911 IMF5912 IMF6485	2N3957 2N3958 IMF5911 IMF5912 IMF6485	IT22913 IT22914 IT22915 IT22916 IT22917	IT122 IT122 IT120 IT120 IT122	J113A J113A-1B J114 J1401 J1402	J113 J113 2N5555 IT807 IT502
FE4304 FE5245 FE5246 FE5247 FE5457	2N5458 2N5459 2N5459 2N5458 2N5457	IT100 IT101 IT108 IT109 IT120	IT100 IT101 IT24416 IT24418 IT120	IT2919 IT2920 IT2920 IT2936 IT2937	IT122 IT122 IT120 IT120 IT120	J1403 IT503 IT504 J1405 J1406 J174	IT503 IT503 IT504 IT505 J174
FE5458 FE5459 FE5464 FE5465 FE5466	2N5458 2N5459 2N5484 2N5485 2N5486	IT120A IT121 IT122 IT124 IT126	IT120A IT121 IT122 IT124 IT126	IT2972 IT2973 IT2974 IT2975 IT2976	IT122 IT122 IT120 IT120 IT120	J174-1B J175 J175-1B J176 J176-1B	J174 J175 J175 J176 J176

\*\*CONSULT FACTORY

# DISCRETE CROSS REFERENCE (cont.)

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
J177 J177-18	J177 J177	K309-18 K310-18 KE3684 KE3685 KE3686	J309 J310 2N3684 2N3685 2N3686	LS5105 LS5245 LS5246 LS5247 LS5248	2N5485 2N5484 2N5485 2N5485	MD7026B MD7033 MD7033A MD7033B MD7034	IT122 IT122 IT122 IT122 IT122
J202-18	J202	KE3687	2N3687	LS5358	J204	MD7007	IT129
J203	J203	KE3693	2N3693	LS5359	J204	MD7007A	IT129
J203-18	J203	KE3690	2N3690	LS5360	J202	MD7007B	IT129
J204	J204	KE3691	2N3691	LS5361	J202	MD7008	IT129
J204-18	J204	KE3693	2N3693	LS5362	J203	MD7008A	IT129
J210	2N5367	KE4091	ITE4091	LS5363	J203	MD7008B	IT128
J211	2N5367	KE4092	ITE4092	LS5364	J203	MD8001	IT120
J212	2N5367	KE4093	ITE4093	LS5361	2N4967A	MD8002	IT120
J230	2N4667	KE4220	2N5457	LS5392	2N4956A	MD8003	IT122
J231	2N4669	KE4221	2N5455	LS5393	2N4955A	MD918	IT122
J232	2N4689	KE4222	2N5459	LS5394	2N4959A	MD918A	IT122
J235	J230	KE4223	J204	LS5395	2N4959A	MD918B	IT122
J270-18	J270	KE4321	ITE4321	LS5391	2N4959A	MD982	IT123
J271	J271	KE4322	ITE4322	LS5397	2N5457	MD984	IT123
J271-18	J271	KE4333	ITE4333	LS5458	2N5458	MEP103	2N5457
J300	2N5397	KE4416	ITE4416	LS5459	2N5459	MEP104	2N5459
J304	2N5485	KE4856	ITE4391	LS5484	2N5484	MEP3069	2N4341
J305	2N5484	KE4857	ITE4392	LS5485	2N5485	MEP3070	2N4339
J308	J308	KE4858	ITE4393	LS5486	2N5486	MEP3458	2N4341
J309	J309	KE4859	ITE4391	LS5556	2N5685	MEP3459	2N4339
J310	J310	KE4860	ITE4392	LS5557	2N5684	MEP3460	2N4338
J315	2N5397	KE4861	ITE4393	LS5558	2N5684	MEP3684	2N3684
J316	U308	KE5101	ITE4393	LS5559	2N5685	MEP3685	2N3685
J317	U310	KE5103	J204	LS5559	2N5685	MEP3686	2N3686
J3970	ITE4391	KE5104	ITE4416	LS5640	2N5640	MEP3687	2N3687
J3971	ITE4392	KE5105	ITE4416	M103	3N161	MEP3821	2N3821
J3972	ITE4393	KE5111	ITE4392	M104	3N161	MEP3822	2N3822
J401	T501	KH5195	2N5195	M105	3N166	MEP3823	2N3823
J402	T502	KH5197	2N5197	M107	3N169	MEP3554	2N3554
J403	T503	KH5199	2N5199	M108	3N191	MEP3555	2N3555
J404	IT503	KH5199	2N5199	M113	3N161	MEF3556	2N3556
J405	IT504	LDF603	2N4221	M114	3N161	MEF3857	2N3857
J406	IT505	LDF604	2N4221	M115	3N161	MEF4358	2N4358
J4091	ITE4091	LDF605	2N4221	M117	3N251	MEF4359	2N4323
J4092	ITE4092	LM114	IT120	M119	3N161	MEF4224	2N4224
J4093	ITE4093	LM114A	IT120A	M153	3N163	MEF4391	IT4391
J410	T502	LM114AH	IT120A	M154	3N154	MEF4392	IT4392
J411	T503	LM114H	IT120	M511	3N172	MEF4393	IT4393
J412	T503	LM115	IT120	M511A	3N172	MEF4416	IT4416
J420	IT5811	LM115A	IT120A	M517	3N163	MEF4356	2N4356
J421	IT5812	LM115AH	IT120A	MA7807	IT122	MEF4857	2N4857
J4220	J204	LM115H	IT120	MA7809	IT122	MEF4858	2N4858
J4221	J202	LM1194	IT120A	MA701AH	IT140	MEF4859	2N4859
J4222	J203	LM394	IT120A	MA701RH	IT140	MEF4860	2N4860
J4223	J202	LS3069	2N5458	MA701DH	IT140	MEF4861	2N4861
J4224	J202	LS3070	2N5458	MA701H	IT140	MEF5103	IT4416
J430	J309(X2)	LS3071	2N5458	MD1120	IT122	MEF5104	IT4415
J4302	2N4302	LS3456	J204	MD1121	IT122	MEF5105	IT4416
J4303	2N5459	LS3459	J204	MD1122	IT122	MEF5245	IT4416
J4304	2N5458	LS3460	J204	MD1123	IT139	MEF5246	2N5484
J431	J310(X2)	LS3684	2N5684	MD1123	IT129	MEF5247	2N5486
J433	2N5457	LS3685	2N5685	MD1120	IT129	MEF5248	2N5486
J4338	2N5457	LS3686	2N5686	MD2219	IT129	MEF5249	2N5484
J4339	2N5457	LS3687	2N5687	MD2219A	IT129	MEF5295	2N5485
J43391	ITE4391	LS3819	2N5484	MD2219	IT129	MEF5286	2N5486
J4392	ITE4392	LS3821	2N5457	MD2219A	IT129	MEF5561	U401
J4393	ITE4393	LS3822	2N5458	MD2363	IT129	MEF5562	U402
J4415	ITE4415	LS3823	2N5458	MD2365A	IT129	MEF5563	U403
J4655	ITE4656	LS3821	2N5921	MD2369A	IT129	MEM511	3N172
J4657	ITE4657	LS3822	2N5922	MD2904	IT139	MEM511A	3N172
J4889	ITE4868	LS3995	ITE4416	MD2904A	IT129	MEM511C	3N172
J4889	ITE4869	LS3997	ITE4416	MD2905	IT139	MEM512	3N172
J4889	ITE4860	LS3998	ITE4416	MD2974	IT120	MEM517A	3N172
J48891	ITE4861	LS3999	ITE4416	MD2974	IT120	MEM517B	3N172
J48897	2N4557	LS4220	J204	MD2975	IT120	MEM517C	3N172
J4887A	2N4867A	LS4221	J202	MD2978	IT120	MEM550	3N189
J4887RR	2N4867	LS4222	J203	MD2979	IT120	MEM550C	3N189
J4888	2N4868	LS4223	J202	MD3008	IT120	MEM550F	3N189
J4888A	2N4868A	LS4224	J202	MD3250	IT132	MEM551	3N189
J4888RR	2N4868	LS4338	2N5457	MD3250A	IT131	MEM551C	3N189
J4889	2N4869	LS4339	2N5457	MD3251	IT132	MEM555	3N172
J4889A	2N4869A	LS4340	2N5457	MD3251A	IT131	MEM555C	3N172
J4889RR	2N4869	LS4341	2N5458	MD3409	IT132	MEM560	3N151
J5103	2N5494	LS4341	2N5458	MD3410	IT129	MEM560C	3N151
J5104	2N5495	LS4352	ITE4392	MD3467	IT139	MEM561	3N163
J5105	2N5466	LS4393	ITE4393	MD3725	IT129	MEM551C	3N153
J6163	2N5496	LS4416	ITE4416	MD3762	IT139	MEM552	2N4351
K114-18	2N5555	LS4495	ITE4091	MD4957	IT132	MEM552C	2N4351
K210-18	2N5337	LS4497	ITE4092	MD5000	IT132	MEM553	2N4351
K211-18	2N5337	LS4498	ITE4093	MD5000A	IT132	MEM553C	2N4351
K212-18	2N5387	LS4499	ITE4091	MD5000B	IT132	MEM711	M116
K300-18	2N5387	LS4490	ITE4092	MD7000	IT129	MEM712	M116
K304-18	2N5466	LS4481	ITE4093	MD7001	IT139	MEM712A	M118
K305-18	2N5484	LS5103	2N5484	MD7002	IT122	MEM713	3N170
K306-18	J308	LS5104	2N5485	MD7002A	IT122	MEM806	3N163

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
MEM805A MEM807 MEM807A MEM814 MEM816	SN1163 SN1172 SN1172 SN1161 SN1172	MPF840 MPF841 MPF842 MPF102 MPF103	2N5520 2N5521 2N5522 2N5486 2N5487	NKT80111 NKT80112 NKT80113 NKT80211 NKT80212	2N4220 2N4220 2N3821 2N4339 2N4339	SA2718 SA2719 SA2720 SA2721 SA2722	IT122 IT120 IT121 IT122 IT120
MEM817 MEM823 MEM824 MEM854A MEM854B	SN1172 MF8523 SN1188 SN1188 SN1188	MPF104 MPF105 MPF106 MPF107 MPF108	2N5487 2N5489 2N5485 2N5486 2N5486	NKT80213 NKT80214 NKT80215 NKT80216 NKT80217	2N4339 2N4339 2N4339 2N4339 2N4220	SA2723 SA2724 SA2726 SA2727 SA2738	IT121 IT122 IT122 IT122 IT120A
MEM855 MEM855A MEM855B MF810 MF803	SN1180 SN1180 SN1180 2N4338	MPF109 MPF111 MPF112 MPF161 MPF208	2N5484 2N5485 2N5489 2N5388 2N5382	NKT80422 NKT80423 NKT80424 NPC108 NPC211N	2N4220 2N4220 2N4220 2N5484 2N4338	SA2739 SDF1001 SDF1002 SDF1003 SDF1004 SDF1005	IT120 2N5432 2N5433 2N5434 2N5434 2N5430
MF818 MF82000 MF82001 MF82004 MF82005	2N4658 2N4416 2N4416 2N4933 2N4929	MPF209 MPF256 MPF4391 MPF4392 MPF4393	2N5821 ITE4415 ITE4391 ITE4392 ITE4393	NPC212N NPC213N NPC214N NPC215N NPC216N	2N4338 2N4338 2N4339 2N4339 2N4339	SDF501 SDF502 SDF503 SDF504 SDF505	2N5520 2N5520 2N5520 2N5520 2N5520
MFE2005 MFE2006 MFE2008 MFE2009 MFE2010	2N4031 2N4668 2N4859 2N4859 2N4859	MPF820 MPF870 MPF871 MTF101 MTF102	J310 J175 J15 2N5434 2N5484	NPD5554 NPD5555 NPD5555 NPD6301 NPD6302	IT550 IT550 IT550 2N3954 2N3954	SDF506 SDF507 SDF508 SDF509 SDF510	2N5520 2N5520 2N5520 2N5520 2N3954
MFE2011 MFE2012 MFE2012 MFE2083 MFE2084	2N5433 2N5433 2N5434 2N4338 2N4339	MTF103 MTF104 MTF104 ND5700 ND5701	2N5457 2N5459 2N5459 IT120A IT120A	NPD6303 OT3 P1004 P1005 P1027	2N3956 2N4338 2N5116 2N5115 2N5267	SDF512 SDF513 SDF514 SDF561 SDF562	2N3954 2N3954 2N3954 IT122 IT122
MFE2035 MFE2132 MFE2133 MFE3002 MFE3003	2N4340 2N4860 2N4860 2N170 2N164	NDF9401 NDF9402 NDF9403 NDF9404 NDF9405	IT500 IT501 IT502 IT503 IT504	P1028 P1028 P1059 P1066 P1087	2N5270 2N5270 2N5269 2N5115 2N5115	SDF663 SES3819 SFT601 SFT602 SFT603	IT122 2N5484 2N4338 2N4338 2N4338
MFE3020 MFE3021 MFE4007 MFE4008 MFE4009	SN1168 SN1168 2N3585 2N3686 2N3685	NDF9406 NDF9407 NDF9408 NDF9409 NDF9410	IT500 IT501 IT502 IT503 IT504	P1117E P1118E P1119E PF510 PF510	2N5640 2N5641 2N5640 2N5115 2N5101	SFT604 SI301AT SI301BT SI301CT SI301ET	2N3939 IT129 IT129 IT129 IT129
MFE4010 MF44011 MF44012 MFE423 MK10	2N2508 2N2608 2N2609 IT1700 2N4416	NF3819 NF4305 NF4305 NF4304 NF4445	2N5484 2N5487 2N5489 2N5487 2N5482	PF5102 PF5103 PF511 PF5301 PF5301-1	2N4887 2N4887 2N5114 2N4119A 2N4117A	SL360C SL362C SL2000 SL2020 SL2021	IT129 IT129 2N4340 2N3954 2N3954
MMF1 MMF2 MMF3 MMF4 MMF5	2N5197 2N3821 2N5198 2N3822 2N5199	NF4445 NF4447 NF4448 NF5000 NF501	2N5433 2N5433 2N5433 2N4224 2N4224	PF5301-2 PF5301-3 PL1091 PL1092 PL1093	2N4119A 2N4118A 2N5823 2N5823 2N5823	SL1202 SL1203 SL1204 SL1205 SL1206	2N3954 2N3954 2N3954 2N3954 2N3954
MMF6 MMT3923 MP301 MP302 MP303	2N3955A 2N3823 IT124 IT124 IT124	NF5006 NF5101 NF5102 NF5103 NF5111	2N4416 2N4867 2N4867 2N4867 2N4868	PL1094 PL3654 PL3655 PL3656 PL3687	2N3823 2N3684 2N3684 2N3685 2N3687	SU2027 SU2028 SU2029 SU2029 SU2030	2N3954 2N3954 2N3954 2N3954 2N3954
MP310 MP311 MP312 MP313 MP318	2N4045 2N4045 2N4044 IT124 IT120A	NF5163 NF520 NF521 NF522 NF523	2N4341 2N3684 2N3685 2N3686 2N3685	PN4091 PN4092 PN4093 PN4220 PN4221	IT5091 IT5092 IT5093 J204 J202	SU2020 SU2021 SU2021 SU2022 SU2023	2N3955 2N3954 2N3954 2N3954 2N3954
MP350 MP351 MP352 MP353 MP350	IT132 IT130 IT130 IT130A IT132	NF530 NF5301 NF5301-1 NF5301-2 NF5301-3	2N4341 2N4118A 2N4117A 2N4119A 2N4119A	PN4222 PN4223 PN4224 PN4242 PN4360	J203 J204 J202 2N5481 2N5480	SU2034 SU2034 SU2035 SU2035 SU2074	2N3954 2N3955 2N3954 2N3955 2N3954
MP351 MP352 MP354 MP354A MP355	IT130A IT130A 2N3654 2N3654A 2N3655	NF531 NF532 NF533 NF5457 NF5458	2N4339 2N4341 2N4339 2N5457 2N5458	PN4391 PN4392 PN4416 PN4856 PN4857	IT54381 IT54382 IT54415 2N4856 2N4857	SU2075 SU2076 SU2077 SU2077 SU2078	2N3954 2N3954 2N3954 2N3955 2N3955
MP356 MP3567 MP3568 MP3569 MP3560	2N3656 2N3657 2N3658 2N3659 2N3656	NF5459 NF5464 NF5465 NF5466 NF5466	2N5459 2N5459 2N5459 2N5459 2N5459	PN4858 PN4859 PN4860 PN4861 PN5033	2N4858 2N4858 2N4860 2N4861 2N5480	SU2078 SU2080 SU2081 SU2081 SU208A	2N3955 U404 U404 2N3954 2N3954
MP5907 MP5908 MP5909 MP5911 MP5912	2N5807 2N5828 2N5809 2N5911 2N5912	NF5838 NF5839 NF5840 NF5853 NF5854	2N5639 2N5639 2N5640 2N4860 2N4861	PTC151 PTC152 SA2253 SA2254 SA2255	2N5484 2N5485 IT122 IT122 IT122	SU2098B SU2098B SU2099A SU2099A SU2095A	2N3954 2N3957 2N3957 2N3954 2N3954
MP804 MP830 MP831 MP832 MP833	2N5620 2N5520 2N5521 2N5522 2N5523	NF580 NF581 NF582 NF583 NF584	2N5432 2N5432 2N5433 2N5434 2N5433	SA2644 SA2648 SA2710 SA2711 SA2712	IT120 IT120 IT120 IT120 IT121	SU2355 SU2356A SU2367 SU2367 SU2368	2N3955 2N3955 2N3955 2N3955 2N3955
MP835 MP836 MP837 MP838 MP839	2N3654 2N3655 2N3655 2N3656 2N3657	NF585 NF5851 NF5852 NF5853 NF5854	2N4659 U310 U310 U310 U310	SA2713 SA2714 SA2715 SA2716 SA2717	IT121 IT122 IT120 IT120 IT121	SU2358A SU2358B SU2369A SU2410 SU2411	2N3955 2N3957 2N3957 2N3954 2N3954

# DISCRETE CROSS REFERENCE (cont.)

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
SU2412 SU2652 SU2652M SU2653 SU2653M	2N5908 U401 U401 U401 U401	T05909A T05911 T05911A T05912 T05912A	2N5908 IT5911 IT5912 IT5912 IT5912	U163 U1837E U184 U1897E U1898	2N5924 2N5485 2N5397 U1897 U1898	U405 U406 U410 U411 U412	U405 U406 2N5355 2N5356 2N5358
SU2654 SU2654M SU2655 SU2655M SU2655S	U401 U401 U402 U402 U404	T0700 T0701 T0702 T0710 T0711	IT122 IT122 IT122 IT122 IT122	U1699E U197 U198 U1994E	U1699 2N4338 2N4340 2N4341 2N4416	U421 U422 U423 U424 U425	2N5908 2N5508 2N5509 2N5908 2N5908
SU2656M SX3819 SX3820 TD100 TD101	U404 2N5484 2N2603 IT129 IT129	T0713 TIS14 TIS25 TIS26 TIS27	IT122 2N4340 2N3954 2N3954 2N3955	U200 U201 U202 U2047E U221	2N4661 2N4860 2N4855 U2416 2N4381	U428 U430 U431 U440 U441	2N5908 J301(X2) J310(X2) IT5911 IT5911
TD102 TD200 TD201 TD202 TD2219	IT129 IT129 IT129 IT129 IT129	TIS24 TIS41 TIS42 TIS58 TIS59	2N5486 2N5489 2N5493 2N5484 2N5486	U222 U231 U232 U233 U234	2N4391 U231 U232 U233 U234	UC100 U231 U232 U233 U234	2N3584 2N3685 2N4340 2N3586 2N3587
TD224 TD225 TD226 TD227 TD228	IT122 IT122 IT122 IT122 IT122	TIS69 TIS69 TIS69 TIS73 TIS74	2N3955A 2N3955A 2N3955 TIE4391 TIE4392	U235 U240 U241 U242 U243	U235 2N5432 2N5433 2N5432 2N5433	UC155 U2100 U2115 U2120 U2130	2N4416 2N1153 2N1153 2N3586 2N3587
TD229 TD230 TD231 TD232 TD233	IT122 T121 T121 T122 T122	TIS75 TIS68 TIS68A TIX533 TIX535	IT4393 2N4415 2N4416 2N4392 2N4857	U244 U245 U246A U248 U249A	2N5433 2N5902 2N5905 2N5903 2N5907	UC201 U2110 U2110 U2130 U2132	2N3524 2N3687 2N4415 2N5453 2N4543
TD234 TD235 TD236 TD237 TD238	IT122 IT122 IT122 IT122 IT122	TIX536 TIX541 TIX542 TIX553 TIX578	2N4391 2N4859 2N5639 2N5459 2N4341	U250 U250A U251 U251A U252	2N5904 2N5908 2N5905 2N5909 IT5911	UC2134 UC2135 UC2138 UC2139 UC2147	2N5454 2N5454 2N5454 2N3959 2N3558
TD239 TD240 TD241 TD242 TD243	IT122 T121 T121 T120A T120A	TIX579 TN4117 TN4117A TN4118 TN4118A	2N4341 2N4117 2N4117A 2N4118 2N4118A	U253 U254 U255 U256 U257	IT5912 2N4859 2N4859 2N4860 U257	UC2148 U2149 U2150 U2140 U2141	2N3558 2N3958 2N3822 2N4865 2N4865
TD244 TD245 TD246 TD247 TD248	IT129 IT129 IT129 IT129 IT129	TN4119 TN4119A TN4338 TN4339 TN4340	2N4119 2N4119A 2N4338 2N4339 2N4340	U257/T0-71 U266 U273 U273A U274	U257/T0-71 2N4855 2N4118A 2N4118A 2N4118A	UC250 UC251 UC275B UC300 UC310	2N4091 2N4392 3N1155 2N2608 2N2607
TD250 TD2505 TD400 TD401 TD402	IT120A IT139 IT139 IT139 IT139	TN4341 TN5277 TN5278 TP5114 TP5115	2N4341 2N3441 2N4341 2N5114 2N5115	U274A U275 U275A U280 U281	2N4115A 2N4118A 2N4118A 2N5452 2N5453	UC320 UC330 UC440 UC440 UC400	2N2607 2N2607 2N2607 2N2608 2N2607
TD500 TD501 TD502 TD508 TD510	IT139 IT139 IT139 IT132 IT132	TP5116 U110 U111 U112 U113	2N5116 2N2608 2N2608 2N2608 2N2608	U282 U283 U284 U285 U290	2N5453 2N5453 2N5454 2N5454 2N5432	UC401 UC41 UC410 UC420 UC450	2N5116 2N2608 2N5269 2N5267 2N5114
TD511 TD512 TD513 TD514 TD517	IT132 IT132 IT132 IT132 IT132	U114 U177 U179 U179 U180	2N2608 2N4220 2N3921 2N3921 2N4221	U291 U295 U296 U296 U300	2N5434 2N5432 2N5432 2N5432 2N4341	UC451 UC393 UC393 UC393 UC705	2N5116 2N4116 2N4200 2N4220 2N4224
TD518 TD519 TD520 TD521 TD522	IT132 IT132 IT132 IT139 IT139	U1181 U1182 U1277 U1278 U1279	2N4220 2N3821 2N3884 2N3885 2N3885	U3001 U3002 U301 U3010 U3011	2N4339 2N4338 2N115 2N4341 2N4340	UC707 UC714 UC714E UC734 UC734E	2N4860 2N3622 2N4341 2N4416 2N4416
TD523 TD524 TD525 TD526 TD527	IT139 IT139 IT132 IT132 IT131	U1280 U1281 U1282 U1283 U1284	2N3684 2N3822 2N4341 2N4340 2N4341	U3012 U304 U305 U306 U308	2N4388 U304 U305 U306 U308	UC751 UC752 UC753 UC754 UC755	2N4349 2N3649 2N4341 2N4340 2N4341
TD528 TD532 TD5433 TD5434 TD550	IT131 2N5432 2N5433 2N5434 IT129	U1285 U1286 U1287 U1288 U1322	2N4220 2N4341 2N4092 2N4885 2N3822	U309 U310 U311 U312 U314	U309 U310 U310 2N5397 2N5555	UC756 UC805 UC807 UC814 UC851	2N4340 2N5270 2N5115 2N5270 2N2608
TD5502 TD5502A TD5503 TD5503A TD5504	2N5902 2N5902 2N5903 2N5903 2N5904	U1323 U1324 U1325 U133 U1420	2N3822 2N3887 2N3886 2N2608 2N3821	U315 U315 U317 U320 U321	2N5397 U309 U310 2N5433 2N5434	UC853 UC854 UC855 UT100 UT101	2N2608 2N2608 2N2608 2N5397 2N5397
TD5504A TD5505 TD5505A TD5506 TD5906A	2N5904 2N5905 2N5905 2N5906 2N5906	U1431 U1432 U1433 U1437 U148	2N3822 2N3822 2N3822 2N2608 2N2608	U322 U328 U329 U330 U331	2N5433 ** ** ** **	UXC2910 VCR10N VCR11N VCR12N VCR13N	IT126 2N4869 VNR11N 2N3958 2N3958
TD5907 TD5907A TD5908 TD5908A TD5909	2N5907 2N5907 2N5908 2N5908 2N5909	U149 U168 U1714 U1715 U182	2N2608 2N2609 2N4340 2N4387	U350 U401 U402 U403 U404	** U401 U402 U403 U404	VCR20N VCR21N VCR22N VCR44N VCR5P	2N4341 VCR2N VCR1N VCR2N VCR5P
TD5907 TD5908 TD5908A TD5909	2N5907 2N5908 2N5908 2N5909						

**DISCRETE CROSS REFERENCE (cont.)**

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# ANALOG SWITCH CROSS REFERENCE

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT						
AD7505/COM/CHIPS	IH6116C/D	AH5010CN	IH5010CPD	DG180AP	DG180AK	DG200AK	DG200AK
AD7505/MIL/CHIPS	IH6116M/D	AH5012CN	IH5012CPD	DG180BA	DG180BK	DG200AL	DG200AL
AD7505JD	IH6116CJ	AH5013CN	IH5013CPD	DG180BP	DG180BK	DG200AP	DG200AK
AD7505JD/883B	IH6116CJ/883B	AH5014CN	IH5014CPD	DG181AA	DG181AA	DG200SA	DG200BA
AD7505JD	IH6116CP	AH5015CN	IH5015CPD	DG181AA	DGM181AA	DG200UK	DG200BK
AD7505KD	IH6116CJ	AH5016CN	IH5016CPD	DG181AL	DG181AL	DG200BP	DG200BK
AD7505KD/883B	IH6116CJ/883B	AM5011CN	D123AP	DG181AL	DGM181AL	DG200CJ	DG200PJ
AD7505KD	IH6116M/J	D123AS	D123AK	DG181AP	DG181AK	DG201AK	DG201AK
AD7505SD	IH6116CJ/883B	D123BP	D123AU	DG181BA	DGM181AK	DG201AP	DG201BK
AD7505TD	IH6116M/J	D123AP	D123AL	DG181BA	DGM181BA	DG201CJ	DG201CJ
AD7505TD/883B	IH6116M/J/883B	D123AP	D123AL	DG181BP	DGM181BK	DG201BP	IH182MTW
AD7507/COM/CHIPS	IH6216C/D	D125AP	D125AL	DG181BP	DGM181CJ	DG201AP	IH182MJD
AD7507/MIL/CHIPS	IH6216M/D	D125SP	D125BK	DG182AA	DGM182AA	DG201BA	IH182CTW
AD7507JD	IH6216CJ	D128AL	D128AL	DG182AA	DGM182AA	DG201CJ	DG201CJ
AD7507JD/883B	IH6216CJ/883B	D129AP	D129AK	DG182AA	DGM182AA	DG201CJ	DG201CJ
AD7507JD	IH6216CJ	D129BP	D129BK	DG182AL	DGM182AL	DG281AP	IH182MJE
AD7507JD	IH6216CJ	DG123AL	DG123AP	DG182AL	DGM182AL	DG281AP	IH182MTW
AD7507JD	IH6216CJ	DG123AP	DG123AK	DG182AP	DGM182AK	DG281AP	IH182MJD
AD7507JD	IH6216CJ	DG123BP	DG123BK	DG182AP	DGM182AK	DG281AP	IH182CTW
AD7507SD	IH6216M/J	DG125AL	DG125AL	DG182BA	DGM182BA	DG2875A	IH188CTW
AD7507SD/883B	IH6216M/J/883B	DG125AP	DG125AK	DG182BA	DGM182BA	DG2875P	IH188CJU
AD7507TD	IH6216M/J	DG125BP	DG125BK	DG182BA	DGM182BA	DG290AP	IH181MJE
AD7507TD/883B	IH6216M/J/883B	DG125AK	DG125AK	DG182BP	DGM182BK	DG290BP	IH191CJU
AH0126CD	DG126AK	DG126AL	DG126AL	DG182BP	DGM182CJ	DG381AA	DGM182AA
AH0126D/883	DG126AK/883B	DG126BP	DG126BP	DG183AL	DGM183AL	DG381AK	DGM182AK
AH0126D	DG126C	DG129AL	DG129AL	DG183AP	DGM183AK	DG381AP	DGM181A
AH0126D	DG129A	DG129AP	DG129BK	DG183BP	DGM183BK	DG381AP	DGM181B
AH0126D/883	DG129A/883B	DG129BP	DG129BK	DG184AL	DGM184AL	DG381AP	DGM181B
AH0133CD	DG133AK	DG133AP	DG133AK	DG184AL	DGM184AL	DG381CJ	DGM181CJ
AH0133D	DG133AK	DG133BP	DG133BK	DG184AP	DGM184AK	DG384AK	DGM185AK
AH0133D/883	DG133AK/883B	DG134AL	DG134AL	DG184AP	DGM184AK	DG384AP	DGM185AK
AH0134CD	DG134AK	DG134AP	DG134AK	DG184AP	DGM184BK	DG384BK	DGM184BK
AH0134D	DG134AK	DG134BP	DG134BK	DG184AP	DGM184CJ	DG384BP	DGM184CJ
AH0134D/883	DG134AK/883B	DG139AL	DG139AL	DG185AL	DGM185AL	DG384CJ	DGM184CJ
AH0139CD	DG139AK	DG139AP	DG139AL	DG185AL	DGM185AL	DG387AA	DGM188AA
AH0139D	DG139AK	DG139BP	DG139BK	DG185AP	DGM185AK	DG387AK	DGM188AK
AH0139D/883	DG139AK/883B	DG140AL	DG140AL	DG185AP	DGM185AK	DG387AP	DGM188AK
AH0140CD	DG140AK	DG140AP	DG140AK	DG185BP	DGM185BK	DG3878A	DGM1878A
AH0140D/883	DG140AK/883B	DG141AL	DG141AL	DG185BP	DGM185CJ	DG3879K	DGM1878K
AH01414CD	DG141AK	DG141AP	DG141AP	DG186AA	DGM186AA	DG387BP	DGM1878K
AH01414D	DG141AK	DG141BP	DG141BK	DG186AA	DGM186AA	DG3890AP	DGM191AK
AH01414D/883	DG141AK/883B	DG142AL	DG142AL	DG186AP	DGM186AK	DG3890BP	DGM191BK
AH0142CD	DG142AK	DG142AP	DG142AK	DG186BA	DGM186BA	DG3890BP	DGM190BK
AH0142D/883	DG142AK/883B	DG142BP	DG142BK	DG186BP	DGM186BK	DG3890CJ	DGM190CJ
AH0143CD	DG143AK	DG143AL	DG143AL	DG187AA	DGM187AA	DG5040AK	IHS404MJE
AH0143D	DG143AK	DG143AP	DG143AK	DG187AA	DGM187AA	DG5040AL	IHS404MFD
AH0143D/883	DG143AK/883B	DG143BP	DG143BK	DG187AL	DGM187AL	DG5040CJ	IHS404CPE
AH0144CD	DG144AK	DG144AL	DG144AL	DG187AL	DGM187AL	DG5040CK	IHS404CJ
AH0144D	DG144AK	DG144AP	DG144AK	DG187AP	DGM187AK	DG5041AA	IHS411MTW
AH0144D/883	DG144AK/883B	DG145AL	DG145AL	DG187AP	DGM187AK	DG5041AK	IHS411MJE
AH0145CD	DG145AK	DG145AP	DG145AK	DG187BA	DGM187BA	DG5041AL	IHS411MFD
AH0145D/883	DG145AK/883B	DG145BP	DG145BK	DG187BA	DGM187BA	DG5041CJ	IHS411CPE
AH0145D	DG145AK	DG145BP	DG145BK	DG187BP	DGM187BK	DG5041CK	IHS411CJ
AH0145D/883	DG145AK/883B	DG146AL	DG146AL	DG187BP	DGM187BK	DG5042AA	IHS424MTW
AH0145D	DG146AK	DG146AP	DG146AK	DG188AA	DGM188AA	DG5042AK	IHS424MJE
AH0145D/883	DG146AK/883B	DG146BP	DG146BK	DG188AA	DGM188AA	DG5042AL	IHS424MFD
AH0145D	DG146AK	DG151AL	DG151AL	DG188AL	DGM188AL	DG5042CJ	IHS424CPE
AH01511CD	DG151AK	DG151AP	DG151AK	DG189AL	DGM189AL	DG5042CK	IHS424CJ
AH01511D/883	DG151AK/883B	DG151BP	DG151BK	DG189AP	DGM189AK	DG5043AK	IHS434MJE
AH01522D	DG152AK	DG152AL	DG152AL	DG189AP	DGM189AK	DG5043AL	IHS434MFD
AH01523D	DG152AK	DG153AP	DG152AK	DG189AP	DGM189AK	DG5043CJ	IHS434CPE
AH01523D/883	DG152AK/883B	DG153BP	DG153BK	DG189AP	DGM189AK	DG5043CK	IHS434CJ
AH0153CD	DG153AK	DG153AL	DG153AL	DG189BA	DGM189BA	DG5044AA	IHS444MTW
AH0153D	DG153AK	DG153AP	DG153AK	DG189BP	DGM189BK	DG5044AK	IHS444MJE
AH0153D/883	DG153AK/883B	DG153BP	DG153BK	DG189AP	DGM189AK	DG5044AL	IHS444MFD
AH0154CD	DG154AK	DG154AP	DG154AK	DG189AP	DGM189AK	DG5044CJ	IHS444CPE
AH0154D/883	DG154AK/883B	DG154BP	DG154AK	DG189BP	DGM189BK	DG5044CK	IHS444CJ
AH0154D	DG154AK	DG154BP	DG154BK	DG189BP	DGM189BK	DG5045AK	IHS454MJE
AH0155D	DG155AK	DG156AL	DG156AL	DG189AL	DGM189AL	DG5045AL	IHS454MFD
AH01611CD	DG161AK	DG161AP	DG161AK	DG190AL	DGM190AL	DG5045CJ	IHS454CPE
AH01611D/883	DG161AK/883B	DG161BP	DG161BK	DG190AP	DGM190AK	DG5045CK	IHS454CJ
AH01611D	DG161AK	DG161BP	DG162AL	DG190AP	DGM190AK	DG5050AR	IHS454CJ
AH01620D	DG162AK	DG162AP	DG162AK	DG190BP	DGM190BK	DG5068R	IH6116CJ
AH01620D/883	DG162AK/883B	DG162BP	DG162BK	DG190BP	DGM190CJ	DG5068CJ	IH6116CP
AH01623D	DG163AK	DG163AL	DG163AL	DG191AL	DGM191AL	DG5070AR	IH6215MJI
AH01630D	DG163AK	DG163BP	DG163BK	DG191AP	DGM191AK	DG5070BR	IH6216CJ
AH01630D	DG163AK	DG163BP	DG163BK	DG191AP	DGM191AK	DG5070CJ	IH6216CJ
AH01630D/883	DG163AK/883B	DG164AL	DG164AL	DG191AP	DGM191CJ	DG5080AP	IH6108MJE
AH01644CD	DG164AK	DG164AP	DG164AK	DG191AP	DGM191BK	DG5084AP	IH6108CJ
AH01644D	DG164AK	DG164BP	DG164BK	DG191BP	DGM191BK	DG5084CJ	IH6108CPE
AH01644D/883	DG164AK/883B	DG164BP	DG164BK	DG191BP	DGM191CJ	DG5084CP	IH6208MJE
AH0509CN	IHS009CPD	DG180AL	DG180AL	DG190AA	DGM200AA	DG5099P	IH6208CJ

\*\*CONSULT FACTORY

# ANALOG SWITCH CROSS REFERENCE (cont.)

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
DG509CJ DG5111AL DG5111AP DG5111BP G115AP	IH5208CPE DG5111AL DG5111AK DG5111BK G115AK	H1-5041-5 H1-5041-8 H1-5042-2 H1-5042-5 H1-5042-8	IHS041CJE IHS14MJE/883B IHS042CJE IHS042CJE IHS142MJE/883B	TL188CN TL188L TL188N TL188ML TL188CJ	DGM182CJ DGM182CA DGM182CJ DGM182AA IH5045CJE		
G115BP G115P G115K G116AL G116AP G116BP	G115BJ G115BK G115AL G116AK G116BJ	H1-5043-2 H1-5043-5 H1-5043-8 H1-5044-2 H1-5044-5	IHS143MJE IHS143CJE IHS143MJE/883B IHS144MJE IHS144CJE	TL188CN TL188J TL188N TL188MJ TL188CL	IHS045CPE IHS045CJE IHS045CPE IHS045MJE IH5042CTW		
G116BP G117AL G118AL G118AP G118AL	G116BK G117AL G118AL G118AK G118AL	H1-5044-8 H1-5045-3 H1-5045-6 H1-5045-9 H1-5046-2	IHS144MJE/883B IHS145MJE IHS145CJE IHS145MJE/883B IHS146MJE/883B	TL188CN TL188L TL188N TL188ML TL191CJ	IHS042CPE IHS042CTW IHS042CPE IHS042MTW IH5043CJE		
G123AL G123AP HO-0201-6 HO-0381-6 HO-0384-6	G123AL G123AK DG201C/D DG181C/D DG184C/D	H1-5046-5 H1-5046-8 H1-5047-2 H1-5047-5 H1-5047-8	IHS048CJE IHS048MJE/883B IHS047MJE IHS047CJE IHS047MJE/883B	TL191CN TL191IJ TL191N TL191MJ	IHS049CPE IHS049CJE IHS049CPE IHS049MJE		
HO-0387-5 HO-0389-8 HO-0395-6 HO-0505A-6 HO-0507-6	DGM187C/D DGM180C/D IHS16C/D IHS18C/D IHS21C/D	H1-5049-2 H1-5049-5 H1-5049-8 H1-5050-2 H1-5050-5	IHS149MJE IHS149CJE IHS149MJE/883B IHS150MJE IHS150CJE				
HO-0507A-6 HO-0508-6 HO-0508A-6 HO-0509-6 HO-0509A-6	IHS215C/D IHS109C/D IHS108C/D IHS208C/D IHS209C/D	H1-5050-8 H1-5051-2 H1-5051-5 H1-5051-8 H2-0200-2	IHS150MJE/883B IHS151MJE IHS151CJE IHS151MJE/883B DG200AA				
HO-0540-6 HO-0541-8 HO-0542-6 HO-0543-6 HO-0544-6	IHS140C/D IHS141C/D IHS142C/D IHS143C/D IHS144C/D	H2-0200-4 H2-0200-5 H2-0200-8 H2-0381-2 H2-0381-5	DG200BA DG200BA DG200AA/883B DG182AA DG181BA				
HO-0545-6 HO-0546-6 HO-0547-6 HO-0548-6 HO-0505-6	IHS145C/D IHS046C/D IHS047C/D IHS148C/D IHS150C/D	H2-0381-8 H2-0387-2 H2-0387-5 H2-0387-8 H2-0200-5	DGM181AA/883B DGM188AA DGM187AA DGM188AA/883B DG200CJ				
HO-05051-6 HO-05052-6 HO-05053-6 HO-05054-6 HO-05055-6	IHS051C/D DG200AK DG200B DG200B DG200C/D	H1-0301-5 H1-0301-8 H1-0301-5 H1-0301-5 H1-0301-5	DG201CJ DGM181CJ DGM184CJ DGM189CJ IHS116CPI				
H1-0201-6 H1-0201-7 H1-0201-8 H1-0201-9 H1-0201-9	DG200AK/883B DG201AK DG201B DG201B DG201AK/883B	H1-0302-5 H1-0307-5 H1-0307-5 H1-0307-5 H1-0307-5	IHS116CPI IHS216CPI IHS216CPI IHS216CPI H1-0508A-5				
H1-0381-2 H1-0381-3 H1-0381-8 H1-0384-3 H1-0384-5	DGM182AK DGM183AK DGM182AK/883B DGM185AK DGM184AK	H1-0308-5 H1-0308-5 H1-0308-5 H1-0308-5 H1-0308-5	IHS200CPE IHS200CPE IHS200CPE DG201AK DG201AK/883B IHS202MJE				
H1-0384-8 H1-0387-2 H1-0387-5 H1-0387-8 H1-0390-2	DGM185AK/883B DGM186AK DGM187AK DGM188AK/883B DGM191AK	LF11202D/883 LF111509D LF111508D/883 LF111509D LF111509D/883	IHS202MJE/883B IHS109MJE IHS109MJE/883B IHS202MJE IHS202MJE/883B				
H1-0390-5 H1-0390-8 H1-0505-6 H1-0506-5 H1-0506-8	DGM190AK DGM191AK/883B IHS116MJI IHS116MJI IHS116MJI/883B	LF13201D LF13201N LF13202D LF13202N LF13208N	DG201CJ DGM181CJ IHS202CJE IHS202CJE IHS105CPE				
H1-0506A-2 H1-0506A-5 H1-0506A-8 H1-0507-2 H1-0507-5	IHS116MJI IHS116MJI IHS116MJI/883B IHS216MJI IHS216CJI	LF13509D LF13509N MM450H MM451H MM452D	IHS202CJE IHS202CPE MM450H MM451H MM452J				
H1-0507-8 H1-0507A-2 H1-0507A-5 H1-0507A-8 H1-0508-2	IHS216MJI/883B IHS216MJI IHS216MJI IHS216MJI/883B IHS108MJE	MM452F MM455H MM450H MM459H MM452D	MM452F MM455H MM450H MM457H MM452D				
H1-0508-5 H1-0508-8 H1-0508A-2 H1-0508A-5 H1-0508A-8	IHS108CJE IHS208CJE/883B IHS208MJE/883B IHS108MJE IHS209MJE	MM552F MM555H SJM181BC SJM181BC SJM182BC	MM552F MM555H SJM181BC SJM181BC SJM182BC				
H1-0508-2 H1-0508-5 H1-0508-8 H1-0508A-2 H1-0508A-5	IHS209MJE/883B IHS040MJE IHS040CJE IHS040MJE/883B IHS041MJE	SJM182BC SJM182BC SJM182BC SJM191BC TL182CL	JM38510/11108BC JM38510/11108BC JM38510/11108BC JM38510/11108BC DG182BA				

# DATA ACQUISITION CROSS REFERENCE

A

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT						
AD7520JD	AD7520JD	MP7521LN	AD7521LN				
AD7520JN	AD7520JN	MP7521SD	AD7521SD				
AD7520KD	AD7520KD	MP7521TD	AD7521TD				
AD7520KN	AD7520KN	MP7521UD	AD7521UD				
AD7520LD	AD7520LD	MP7523JN	AD7523JN				
AD7520LN	AD7520LN	MP7523KN	AD7523KN				
AD7520SD	AD7520SD	MP7523LN	AD7523LN				
AD7520TD	AD7520TD	MP7523AD	AD7541AD				
AD7520UD	AD7520UD	MP7523BD	AD7541BD				
AD7521JD	AD7521JD	MP7521JN	AD7541JN				
AD7521KD	AD7521KD	MP7521SD	AD7541SD				
AD7521KN	AD7521KN	MP7521TD	AD7541TD				
AD7521LD	AD7521LD	AD7521LN					
AD7521LN	AD7521LN						
AD7521SD	AD7521SD						
AD7521TD	AD7521TD						
AD7521UD	AD7521UD						
AD7523AD	AD7523AD						
AD7523BD	AD7523BD						
AD7523CD	AD7523CD						
AD7523JN	AD7523JN						
AD7523KN	AD7523KN						
AD7523LN	AD7523LN						
AD7523SD	AD7523SD						
AD7523TD	AD7523TD						
AD7523UD	AD7523UD						
AD7530JD	AD7530JD						
AD7530JN	AD7530JN						
AD7530KD	AD7530KD						
AD7530LN	AD7530LN						
AD7531JD	AD7531JD						
AD7531JN	AD7531JN						
AD7531KD	AD7531KD						
AD7531LN	AD7531LN						
AD7531SD	AD7531SD						
AD7533AD	AD7533AD						
AD7533BD	AD7533BD						
AD7533CD	AD7533CD						
AD7533JN	AD7533JN						
AD7533KN	AD7533KN						
AD7533LN	AD7533LN						
AD7533SD	AD7533SD						
AD7533TD	AD7533TD						
AD7533UD	AD7533UD						
AD7541AD	AD7541AD						
AD7541BD	AD7541BD						
AD7541JN	AD7541JN						
AD7541KN	AD7541KN						
AD7541SD	AD7541SD						
AD7541TD	AD7541TD						
DAC1020LCD	DAC1020LCD	AD7520LD					
DAC1221LCD	DAC1221LCD	AD7520UD					
DAC1221LD	DAC1221LD	AD7520KD					
DAC1222LCD	DAC1222LCD	AD7520DO					
DAC1222LD	DAC1222LD	AD7520JN					
DAC1218LCD	DAC1218LCD	AD7541BD					
DAC1218LCN	DAC1218LCN	AD7541LN					
DAC1219LCD	DAC1219LCD	AD7541AD					
DAC1219LCN	DAC1219LCN	AD7541JN					
DAC1220LCD	DAC1220LCD	AD7521LD					
DAC1220LCN	DAC1220LCN	AD7521UD					
DAC1221LCD	DAC1221LCD	AD7521KD					
DAC1221LD	DAC1221LD	AD7521DO					
DAC1222LCD	DAC1222LCD	AD7521JN					
DAC1222LD	DAC1222LD	AD7521SD					
MP7520JD	MP7520JD	AD7520JN					
MP7520JN	MP7520JN	AD7520LN					
MP7520KD	MP7520KD	AD7520SD					
MP7520KN	MP7520KN	AD7520DO					
MP7520LD	MP7520LD	AD7520UD					
MP7520LN	MP7520LN	AD7520KD					
MP7520SD	MP7520SD	AD7520JN					
MP7520DO	MP7520DO	AD7520LN					
MP7520UD	MP7520UD	AD7520SD					
MP7521JD	MP7521JD	AD7521JN					
MP7521JN	MP7521JN	AD7521LN					
MP7521KD	MP7521KD	AD7521SD					
MP7521KN	MP7521KN	AD7521DO					
MP7521LD	MP7521LD	AD7521UD					

\*\*CONSULT FACTORY

# WATCH & CLOCK CROSS REFERENCE

A

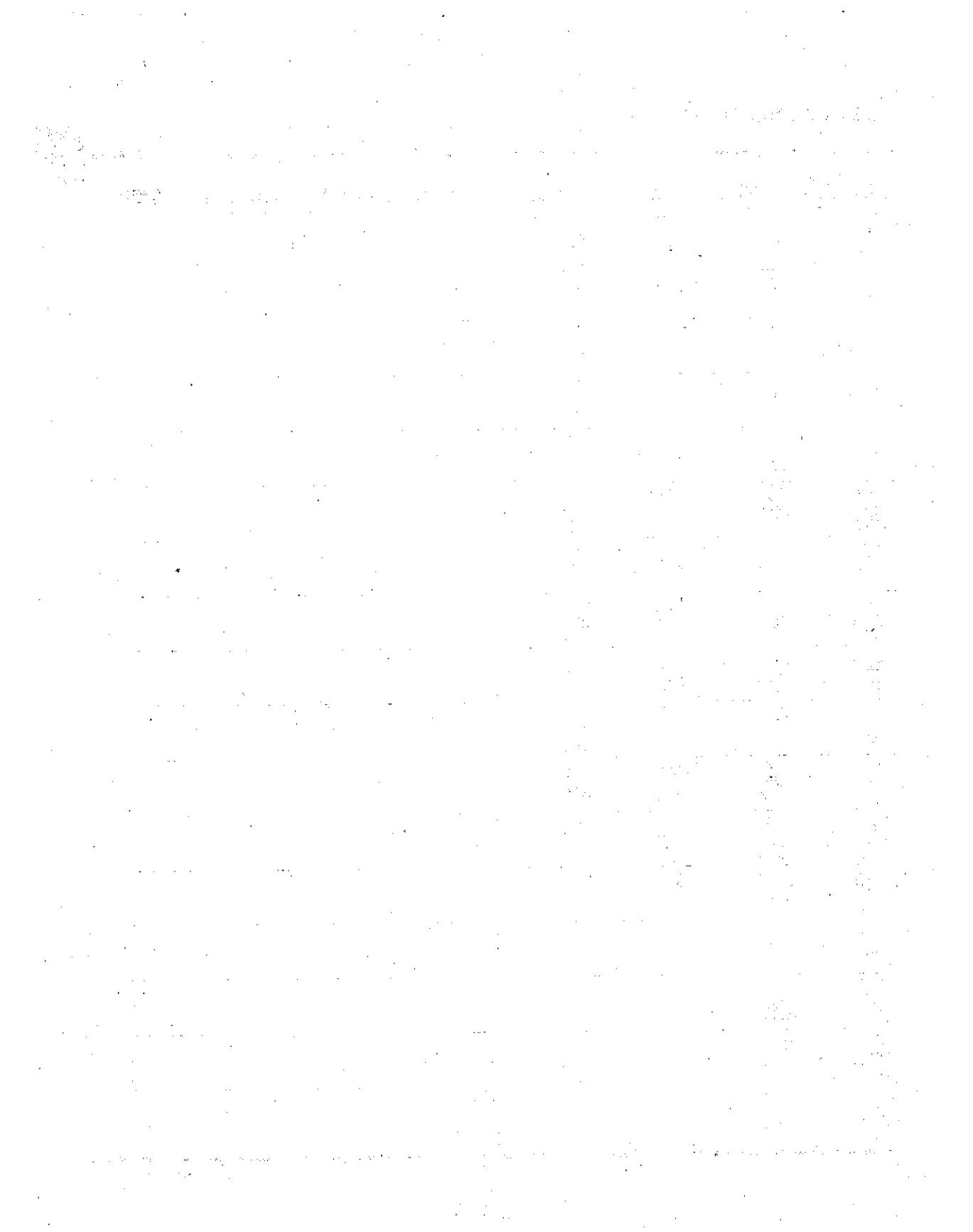
ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
CD22001H CD22015E E1115 E1151 E1426	ICM1424C ICM7051A CM1115A CM1115B CM7050U						
HD43871 HD43871 KS5183 KS5240B01H KS5240B01J	ICM7050G ICM7050H ICM7269 ICM7245B ICM7245A						
KS5240B01H KS5240B01J KS5240B2CH KS5240BU01E M5001	ICM7245D ICM7245E ICM7245F ICM7245U ICM7269						
MS8434P MS8435P MS8435-001P MS8437-001P MB101	ICM7038D CM1115B CM7050G ICM7070L ICM7245B						
MB103 MB105 MB107 MB108 MB143	ICM7245E ICM7245I ICM7245D ICM7245E ICM7245A						
MB144 MB510 MB511 MB512 MB513	ICM7245F ICM1115B ICM7050H ICM7050H ICM7050G						
MC521 MC522 MC531 MC533 MC541	ITS968 ITS968 ICM7050H ICM7050H ICM7052						
MB542 MB7B MCC14440 MCC14483 MU41	ICM7052 ICM7245U ICM1424C ICM7210 ICM1424C						
MU6 MN5091 MN5092A MN5093 MN5292	ICM7220 ICM7038B ICM7038E ICM7051A ICM7050G						
MSM5001 MSM5011 MSM5977 S1424 SCL54301	ICM7259 ICM1424C ICM1424C ICM1424C ICM1424C						
SCL6479 SM5011 SM5510 SM5530B TC8031P	ICM7269 ICM7050G ICM1115B ICM7070P ICM7038A						
TC8032P TC8051P TC8052P TC8055PA TC8057P	ICM7038F ICM7038B ICM7038E ICM1115B ICM7038D						
UCN-4111M UCN-4122M UCN-4134M UPD1952P UPD1962D	ICM7038C ICM7038A ICM7038B ICM7220MFA ICM7050G						
UPD1963C UPD815C UPD815C UPD820C UPD833C	ICM7050 ICM7038E ICM7038B ICM1115B ICM7223						

# LINEAR CROSS REFERENCE

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
723 725 741 748 AD101	UA723 UA723 UA741 UA748 LM101	MC1741 MC1748 MW590 MP55010 NE590	UA741 UA748 AD590 ICL8069 AC590				
AD108 AD301 AD308 AD503 AD532	LM108 LM301 LM308 AD503 AD532	NE592 CP-05 CP-07 CP-08 PM208	NE592 CP-05 CP-07 CP-08 LM308				
AD534 AD539 AC741 AM2502 AM2503	AD534 AD539 UA741 AM2502 AM2503	RC723 RC733 RC741 RC748 RM723	UA723 UA733 UA741 UA748 UA723				
AM2504 AM5402 AM5402 CA101 CA107	AM2504 HA2505 HA2525 LM101 LM107	AM741 RM748 SC748 SG101 SG105	UA741 UA748 UA748 LM101 LM105				
CA111 CA301 CA307 CA308 CA311	LM111 LM301 LM307 LM308 LM311	SG107 SG108 SG110 SG111 SG2502	LM107 LM108 LM110 LM111 AM2502				
CA723 CA741 CA748 DS503 DM2502	UA723 UA741 UA748 AD503 AM2502	SG2503 SG301 SG305 SG307 SG308	AM2503 LM301 LM305 LM307 LM308				
DM2503 DM2504 H22500 H22502 H22505	AM2503 AM2504 HA2500 HA2502 HA2505	SG311 SG3250 SG3253 SG3253 SG3241	LM311 LM4250 UA723 LM733 UA741				
H22507 H22510 H22512 H22515 H22517	HA2507 HA2510 HA2512 HA2515 HA2517	SG748 SS5741 SU535 TL503 TL592	UA748 UA741 SU538 AD503 NE592				
H22520 H22522 H22525 H22527 H22600	HA2520 HA2522 HA2525 HA2527 HA2600	TT-590 UA101 UA102 UA105 UA107	AD580 LM101 LM102 LM105 LM107				
HA2602 HA2605 HA2607 HA2620 HA2622	HA2602 HA2605 HA2607 HA2620 HA2622	UA108 UA110 UA111 UA301 UA302	LM108 LM110 LM111 LM301 LM302				
HA2625 HA2627 HA2720 LH0042 LH2101	HA2625 HA2627 ICL8021 LH0042 LH2101	UA305 UA307 UA308 UA310 UA311	LM305 LM307 LM308 LM310 LM311				
LH2108 LH2110 LH2111 LH2301 LH2308	LH2108 LH2110 LH2111 LH2301 LH2308	UA723 UA733 UA740 UA741 UA748	UA723 UA733 UA740 UA741 UA748				
LH2310 LH2311 LM100 LM101 LM102	LH2310 LH2311 LM100 LM101 LM102	UA777 UHP-503 VR-8059 WG-8038 XR8038	UA777 AD503 ICL8069 ICL8038 ICL8039				
LM105 LM107 LM108 LM110 LM111	LM105 LM107 LM108 LM110 LM111						
LM300 LM301 LM302 LM305 LM307	LM300 LM301 LM302 LM305 LM307						
LM308 LM310 LM311 LM4250 LM723	LM308 LM310 LM311 LM4250 UA723						
LM733 LM740 LM741 LM748 MC1723	UA733 UA740 UA741 UA748 UA723						

\*\*CONSULT FACTORY



# Discretes

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<b>JFET Single Switches</b>					
<b>N-Channel</b>	<b>Page</b>	2N5457-59	1-44	3N170/1	1-59
2N3970-72	1-18	2N5484-86	1-46	IT1750	1-76
2N4091-93	1-22	ITE4416	1-31	M116	1-84
2N4391-93	1-30	J201-4	1-80	<b>P-Channel</b>	
2N4856-61	1-32	J308-10	1-82	3N161	1-56
2N5432-34	1-42	U308-10	1-89	3N163/64	1-57
2N5638-40	1-49	<b>P-Channel</b>		3N172/73	1-60
ITE4091-3	1-22	2N2607-9	1-9	IT1700	1-75
ITE4391-3	1-30	2N5460-65	1-45	<b>Dual P-Channel</b>	
J105-7	1-77	U304-6	1-88	3N165/66	1-58
J111-13	1-78	<b>JFET Dual</b>		3N188-91	1-61
U200-2	1-85	<b>Amplifiers</b>			
U1897-99	1-92	<b>N-Channel</b>		<b>Bipolar Dual</b>	
<b>P-Channel</b>		2N3921/22	1-16	<b>Amplifiers</b>	
2N3993/4	1-19	2N3954-58	1-17	<b>NPN Devices</b>	
2N5018/19	1-36	2N5196-99	1-40	2N4044/45	1-20
2N5114-16	1-37	2N5452-54	1-43	2N4100	1-23
IT100/1	1-64	2N5515-24	1-47	2N4878-80	1-34
J174-77	1-79	2N5902-9	1-50	IT120-22	1-65
<b>JFET Single</b>		2N5911/12	1-51	IT124	1-66
<b>Amplifiers</b>		2N6483-85	1-52	IT126/7	1-67
<b>N-Channel</b>		IMF6485	1-54	LM114	1-83
2N3684-87	1-10	IT500-5	1-71	<b>PNP Devices</b>	
2N3821/22	1-13	A050 (IT 500)	1-73	2N3810/11	1-11
2N3823	1-14	IT550	1-74	2N5117-19	1-39
2N3824	1-15	IT5911/12	1-51	IT130-32	1-68
2N4117-19	1-25	U231-35	1-86	IT136-39	1-69
2N4220-22	1-26	U257	1-87		
2N4223/24	1-27	U401-6	1-90		
2N4338-41	1-28	<b>MOSFET Switches/</b>		<b>Special Function</b>	
2N4416	1-31	<b>Amplifiers</b>		<b>High Speed Dual Diodes</b>	
2N4867-69	1-33	<b>N-Channel</b>		ID100/1	1-62
2N5397/98	1-41	2N4351	1-29	<b>Voltage Controlled</b>	
				Resistors	
				VCR2-7	1-92





## Amplifiers — N-Channel Junction FET (continued)

Ordering Information			$g_{fs}$ min $\mu mho$	$I_{DSS}$ min/max mA	$V_p$ min/max V	$I_{GSS}$ max pA	$BV_{GSS}$ min V	$C_{iss}$ max pF	$C_{rss}$ max pF	$e_n$ max nV/ $\sqrt{Hz}$
Preferred Part Number	Package									
2N5484	TO-92	3000	1.0	5.0	-0.3	-3.0	-1nA	-25	5	1.0
2N5485	TO-92	3500	4.0	10.0	-0.5	-4.0	-1nA	-25	5	1.0
2N5486	TO-92	4000	8.0	20.0	+2.0	-6.0	-1nA	-25	5	1.0
ITE4416	TO-92	4500	5.0	15.0		-6.0	-100	-30	4	2.0
J201	TO-92	500	0.2	1.0	-0.3	-1.5	-100	-40	4	1.0
J202	TO-92	1000	0.9	4.5	-0.8	-4.0	-100	-40	4	1.0
J203	TO-92	1500	4.0	20.0	-2.0	-10.0	-100	-40	4	1.0
J204	TO-92	1500	1.2	typ.	-0.5	-2.0	-100	-25	4	1.0
J308	TO-92	8000	12.0	60.0	-1.0	-6.5	-1nA	-25	(8)	(5.0)
J309	TO-92	10,000	12.0	30.0	-1.0	-4.0	-1nA	-25	(8)	(5.0)
J310	TO-92	8000	24.0	60.0	-2.0	-6.5	-1nA	-25	(8)	(5.0)
U308	TO-52	10,000	12.0	60.0	-1.0	-6.0	-150	-25	7 typ.	4.0 typ.
U309	TO-52	10,000	12.0	30.0	-1.0	-4.0	-150	-25	7 typ.	4.0 typ.
U310	TO-52	10,000	24.0	60.0	-2.5	-6.0	-150	-25	7 typ.	4.0 typ.
										10 @ 100Hz typ.
										10 @ 100Hz typ.
										10 @ 100Hz typ.

## Amplifiers — P-Channel Junction FET

Ordering Information			$g_{fs}$ min $\mu mho$	$I_{DSS}$ min/max mA	$V_p$ min/max V	$I_{GSS}$ max nA	$BV_{GSS}$ min V	$C_{iss}$ max pF	$C_{rss}$ max pF	$e_n$ max nV/ $\sqrt{Hz}$
Preferred Part Number	Package									
2N2607	TO-18	330	-0.3	-1.5	1.0	4.0	3	30	10	—
2N2608	TO-18	1000	-0.9	-4.5	1.0	4.0	10	30	17	—
2N2609	TO-18	2500	-2.0	-10.0	1.0	4.0	30	30	30	—
2N5460	TO-92	1000	-1.0	-5.0	0.75	6.0	5	40	7	2
2N5461	TO-92	1500	-2.0	-9.0	1.0	7.5	5	40	7	2
2N5462	TO-92	2000	-4.0	-16.0	1.8	9.0	5	40	7	2
2N5463	TO-92	1000	-1.0	-5.0	0.75	6.0	5	60	7	2
2N5464	TO-92	1500	-2.0	-9.0	1.0	7.5	5	60	7	2
2N5465	TO-92	2000	-4.0	-16.0	1.8	9.0	5	60	7	2
U304	TO-18	—	-30.0	-90.0	5.0	10.0	.5	30	27	7
J305	TO-18	—	-15.0	-60.0	3.0	5.0	.5	30	27	7
U306	TO-18	—	-5.0	-25.0	1.0	4.0	.5	30	27	7



## Differential Amplifiers — Dual Monolithic P-Channel MOSFETS (Enhancement)

### Ordering Information

Preferred Part Number	Package	$V_{GS(TH)}$ min/max V	$BV_{DS}$ min/max V	$I_{DS}$ max pA	$I_{GSS}$ max pA	$G_{fs}$ min $\mu$ ho	$I_{DS(CN)}$ min/max mA	$I_{DS(ON)}$ max mA	$R_{DS(on)}$ max Ω	$V_{GS(1-2)}$ max mV
3N165	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300 100
3N166	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300
3N188	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300 Zener Protected
3N189	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300 Zener Protected
3N190	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300 100 Zener Protected
3N191	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300

1

## Differential Amplifiers — Dual NPN Bipolar Transistors

### Ordering Information

Preferred Part Number	Package	$I_B(1-2) @$		$I_C = 10\mu A$	$V_{CE} = 5V$	$BV_{CEO}$ V	$I_{CBO}$ nA	Noise dB max	$f_T$ MHz@ $I_C$ min	$C_{cbo}$ pF max	Structure
		$V_{BE(1-2)}$ mV max	$\Delta V_{BE}$ $\mu$ V/ $^{\circ}$ C max								
2N4044	TO-78	3	3	200	5	60	.1	2	200 @ 1mA	0.8	Dielec. Isol.
2N4045	TO-78	5	10	80	25	45	.1	3	150 @ 1mA	0.8	Dielec. Isol.
2N4100	TO-78	5	5	150	10	55	.1	3	150 @ 1mA	0.8	Dielec. Isol.
2N4878	TO-71	3	3	200	5	60	.1	2	200 @ 1mA	0.8	Dielec. Isol.
2N4879	TO-71	5	5	150	10	55	.1	3	150 @ 1mA	0.8	Dielec. Isol.
2N4880	TO-71	5	10	80	25	45	.1	3	150 @ 1mA	0.8	Dielec. Isol.
IT120	TO-78 TO-71	2	5	200	5	45	.1	2 typ.	220 @ 1mA	2	Junc. Isol.
IT120A	TO-78 TO-71	1	3	200	2.5	45	1	2 typ.	220 @ 1mA	2	Junc. Isol.
IT121	TO-78 TO-71	3	10	80	25	45	1	2 typ.	180 @ 1mA	2	Junc. Isol.
IT122	TO-78 TO-71	5	20	80	25	45	1	2 typ.	180 @ 1mA	2	Junc. Isol.
IT124	TO-78	5	15	1500	0.6 @ V <sub>CE</sub> = 1V	2	.1	3	100 @ 100 $\mu$ A	0.8	Junc. Isol.
IT126	TO-78 TO-71	1	3	200	2.5	60	.1	1 typ.	250 @ 10mA	4	Dielec. Isol.
IT127	TO-78 TO-71	2	5	200	5	60	.1	1 typ.	250 @ 10mA	4	Dielec. Isol.
IT128	TO-78 TO-71	3	10	150	10	45	.1	1 typ.	200 @ 10mA	4	Dielec. Isol.
IT129	TO-78 TO-71	5	20	100	20	45	.1	1 typ.	150 @ 10mA	4	Dielec. Isol.

## Differential Amplifiers — Dual PNP Bipolar Transistors

1

Ordering Information		$V_{BE}$ 1-2 mV max	$\Delta V_{BE}$ $\mu V/^\circ C$ max	$h_{FE}$ @ $I_C = 10\mu A$	$I_C = 10\mu A$	$V_{CE} = 5V$ nA max	$BV_{CEO}$ V min	$I_{CEO}$ nA max	Noise dB max	$f_T$ MHz@ $I_C$ min	$C_{ab}$ pF max	Structure
Preferred Part Number	Package											
2N5117	TO-78	3	3	100	10	45	.1	4	100 @ 0.5mA	.8	Dielec. Isol.	
2N5118	TO-78	5	5	100	15	45	.1	4	100 @ 0.5mA	.8	Dielec. Isol.	
2N5119	TO-78	5	10	50	40	45	.1	4	100 @ 0.5mA	.8	Dielec. Isol.	
IT130	TO-78 TO-71	2	5	200	5	-45	1	2 typ.	110 @ 1mA	2	Junc. Isol.	
IT130A	TO-78 TO-71	1	3	200	2.5	-60	1	2 typ.	110 @ 1mA	2	Junc. Isol.	
IT131	TO-78 TO-71	5	10	80	10	-45	1	2 typ.	90 @ 1mA	2	Junc. Isol.	
IT132	TO-78 TO-71	10	20	80	25	-45	1	2 typ.	90 @ 1mA	2	Junc. Isol.	
IT136	TO-78 TO-71	1	3	150	2.5	-60	.1	2 typ.	150 @ 10mA	4	Dielec. Isol.	
IT137	TO-78 TO-71	2	5	150	5	-60	.1	2 typ.	150 @ 10mA	4	Dielec. Isol.	
IT138	TO-78 TO-71	3	10	120	10	-55	.1	2 typ.	180 @ 10mA	4	Dielec. Isol.	
IT139	TO-78 TO-71	5	20	70	20	-45	.1	2 typ.	100 @ 10mA	4	Dielec. Isol.	

### Specialty Items

- ID-100 This product is a diode combination used to protect those P-channel MOSFET duals which are not diode protected. Their chief characteristic is <1 pA leakage when voltage across them is less than 5 mV. If voltage across diodes is adjusted to  $0V \pm 0.1mV$ , leakage is less than 0.01 pA.

VCR2N

VCR3P

VCR4N The VCR family consists of three terminal variable resistors where the resistance value between two of the terminals is controlled by the voltage potential applied to the third.

VCR5P

VCR7N

VCR11N (Dual)

Note: Intersil offers the following military qualified devices:<sup>\*</sup>

N-channel switches	N-channel amplifiers	P-channel switches	P-channel amplifiers
2N4091 JAN, JANTX, JANTXV	2N3821 JAN, JANTX, JANTXV	2N5114 JAN, JANTX, JANTXV	2N2609 JAN
2N4092 JAN, JANTX, JANTXV	2N3823 JAN, JANTX, JANTXV	2N5115 JAN, JANTX, JANTXV	
2N4093 JAN, JANTX, JANTXV		2N5116 JAN, JANTX, JANTXV	
2N4856 JAN, JANTX, JANTXV			
2N4857 JAN, JANTX, JANTXV			
2N4858 JAN, JANTX, JANTXV			

\*JAN processing consists of a sample Group B pulled from the production run.

JANTX processing consists of JAN processing plus 100% electrical read and record, and 100% burn-in.

JANTXV processing consists of JANTX processing plus 100% pre-cap visual and on-shore assembly.

**DISCRETE SELECTOR GUIDE**

	Detailed Application	Important Parameters	Recommended Part Numbers								
			Single N-Channel JFET	Single P-Channel JFET	Dual N-Channel JFET	Single N-Channel MOSFET	Single P-Channel MOSFET	Dual P-Channel MOSFET	Dual NPN Bipolar	Dual PNP Bipolar	
Amplifiers	Audio	low noise	2N4220, 2N3821	2N2607 2N5460	2N3958 IT505	2N4351 3N170-1	3N163 3N164	3N165	2N4044 2N4878	IT130	
	Buffer	low leakage, high gain	2N4221	2N2609 2N5462	2N5905 IT505	M116 IT1750	3N172 IT1700		IT120	IT136	
	Differential	good matching & drift	—	—	2N3954 U401	—	—		IT126	2N3810	
	Fet Input Op Amp	—	—	—	2N5515	—	—		—	—	
	High Impedance	low leakage	2N4117A	IT100 J176 2N5116	2N5905 IT505 U426	IT1750	IT1700		—	—	
	High Frequency	high gain, low capacitance	U308	2N5114	2N5912	2N4351	3N163	3N188	2N4044 2N4878	IT130	
		—	2N5397	J176	IT5912	3N170-1	3N164		IT120	IT136	
	Low Supply Voltage	low pinch-off voltage	2N4338 2N3687	2N5265 J177	U406 2N3958	M116	3N172		IT126	2N3810	
	Low Noise	low noise	2N4867A	2N5116 J176	2N5519 2N5199	—	—		IT140	—	
	Preamplifier	high gain	2N5397 U310	2N5116 J176	IT550 U406	—	—		2N4044	IT130	
Mixers	VHF	RF parameters,	U310	IT100	2N6485	—	—	—	—	—	
		high $g_{fs}/C_{iss}$	2N5397 J310 2N5484	J174 2N5114 2N5912	2N5912 2N5912	—	—		—	—	
	UHF	—	—	—	—	—	—	—	—	—	
Switches	Commutators	low $C_{rss}$	2N4391 ITE4391	2N3993-4 IT100-1 2N5114-6	IT550	IT1750	IT1700	3N165	—	—	
	Sample and Hold	—	—	—	—	—	—		—	—	
	Analog Gates	fast switching,	2N4091-3	2N5114-6	2N5912	3N163	3N165		—	—	
	Digital	low $rDS(on)$	2N4391-3 ITE4391-3 2N5432-4	J174-7 IT100-1	IT5912	3N170-1	3N164		3N188	—	
	Chopper	—	—	—	—	—	—		—	—	
Voltage Control Resistors	Integrator Reset	low $rDS(on)$ , high $Idss$	J111-3 J105-7	—	—	—	—	—	—	—	
	Gain Control Amplitude Stability Attenuators	high $V_{GS(off)}$	VCR2N VCR4N VCR7N	VCR3P	VCR11N	—	—		—	—	
Protection Diodes	Signal Clipping and Clamping	low leakage current	—	—	—	—	—	ID100-1	IT139	—	



# 2N2607-2N2609

## 2N2609 JAN

### P-Channel JFET

1

#### APPLICATIONS

- Low-level Choppers
- Data Switches
- Commutators

#### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source Voltage	30 V
Gate-Drain Voltage	30 V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Power Dissipation	300 mW
Derate above 25°C	2 mW/°C

PIN CONFIGURATION		CHIP TOPOGRAPHY																
TO-18																		
		5510 (for 2N2607, 8)																
		5503 (for 2609, 2809 JAN)																
<b>ORDERING INFORMATION*</b>																		
<table border="1"> <thead> <tr> <th>TO-18</th> <th>WAFER</th> <th>DICE</th> </tr> </thead> <tbody> <tr> <td>2N2607</td> <td>2N2607/W</td> <td>2N2607/D</td> </tr> <tr> <td>2N2608</td> <td>2N2608/W</td> <td>2N2608/D</td> </tr> <tr> <td>2N2609</td> <td>2N2609/W</td> <td>2N2609/D</td> </tr> <tr> <td>2N2609 JAN</td> <td>—</td> <td>—</td> </tr> </tbody> </table>		TO-18	WAFER	DICE	2N2607	2N2607/W	2N2607/D	2N2608	2N2608/W	2N2608/D	2N2609	2N2609/W	2N2609/D	2N2609 JAN	—	—		
TO-18	WAFER	DICE																
2N2607	2N2607/W	2N2607/D																
2N2608	2N2608/W	2N2608/D																
2N2609	2N2609/W	2N2609/D																
2N2609 JAN	—	—																

\*When ordering wafer/dice refer to Appendix B-23.

#### ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER	2N2607		2N2608		2N2609		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max		V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0	V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 0, T <sub>A</sub> = 150°C
I <sub>GSSR</sub>	Gate Reverse Current		3		10		30	nA	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0
			3		10		30	μA	V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 0, T <sub>A</sub> = 150°C
BV <sub>GSS</sub>	Gate-Drain Breakdown Voltage	30		30		30	V	I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0	
V <sub>P</sub>	Gate-Source Pinch-Off Voltage	1	4	1	4	1	4	V	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -1 μA
I <sub>DSS</sub>	Drain Current at Zero Gate Voltage	-0.30	-1.50	-0.90	-4.50	-2	-10	mA	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 0
g <sub>fs</sub>	Small-Signal Common-Source Forward Transconductance	330		1000		2500		μmho	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 0, f = 1 kHz
C <sub>iss</sub>	Common-Source Input Capacitance		10		17		30	pF	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 1 V, f = 140 kHz
NF	Noise Figure		3					dB	V <sub>DS</sub> = -5 V, R <sub>G</sub> = 10 MΩ
					3		3		V <sub>GS</sub> = 0, R <sub>G</sub> = 1 MΩ



# 2N3684-2N3687 N-Channel JFET

1

## FEATURES

- Low Noise
- High Input Impedance
- Low Capacitance

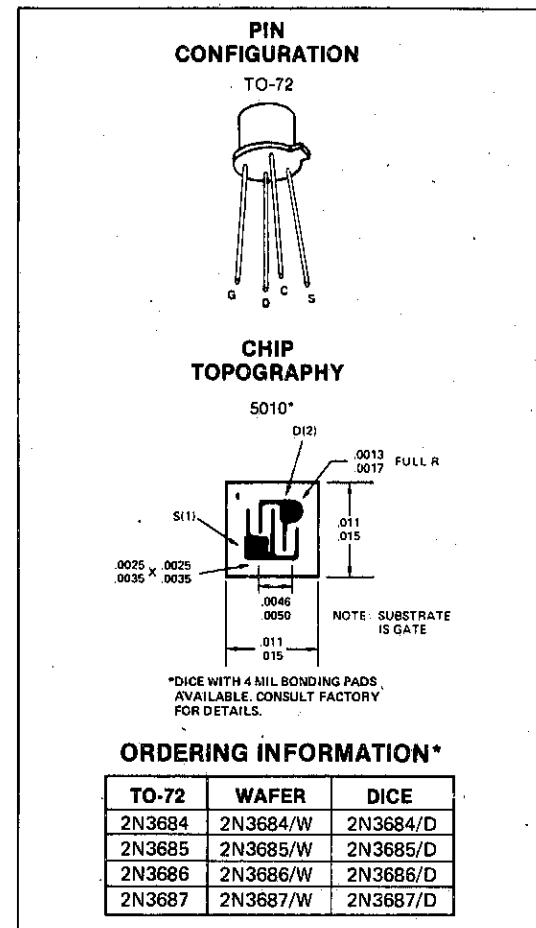
## APPLICATIONS

- Low Level Choppers
- Data Switches
- Multiplexers
- Low Noise Amplifiers

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage .....	-50V
Gate Current .....	50 mA
Storage Temperature Range .....	-65°C to +200°C
Operating Temperature Range .....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C
Power Dissipation .....	300 mW
Derate above 25°C .....	1.7 mW/°C



## ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N3684	2N3684/W	2N3684/D
2N3685	2N3685/W	2N3685/D
2N3686	2N3686/W	2N3686/D
2N3687	2N3687/W	2N3687/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER	2N3684		2N3685		2N3686		2N3687		UNITS	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{GSS}$ Gate to Source Breakdown Voltage	-50	-50	-50	-50	-50	-50	-50	-50	V	$V_{DS} = 0$ , $I_G = 1.0 \mu\text{A}$
$V_p$ Pinch-Off Voltage	2.0	5.0	1.0	3.5	0.6	2.0	0.3	1.2		$V_{DS} = 20 \text{ V}$ , $I_D = 0.001 \mu\text{A}$
$ IGS $ Total Gate Leakage Current	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	nA	$V_{GS} = -30 \text{ V}$ , $V_{DS} = 0$
	$T_A = 150^\circ\text{C}$	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	$\mu\text{A}$	
$ IDSS $ Saturation Current, Drain-to-Source	2.5	7.5	1.0	3.0	0.4	1.2	0.1	0.5	mA	$V_{GS} = 0$ , $V_{DS} = 20 \text{ V}$
$ Y_{fs} $ Forward Transadmittance	2000	3000	1500	2500	1000	2000	500	1500	$\mu\text{mhos}$	
$G_{os}$ Common Source Output Conductance			50		25		10		5	$\mu\text{mhos}$
$C_{iss}$ Common Source Input Capacitance			4.0		4.0		4.0		4.0	pF
$C_{rss}$ Common Source Short Circuit Reverse Transfer Capacitance			1.2		1.2		1.2		1.2	pF
$r_{DS(on)}$ On Resistance			600		800		1200		2400	Ohms
NF Noise Figure			0.5		0.5		0.5		0.5	dB
										$f = 100 \text{ Hz}$ , $R_G = 10 \text{ M}\Omega$ $NBW = 6 \text{ Hz}$ , $V_{DS} = 10 \text{ V}$ $V_{GS} = 0 \text{ V}$



# 2N3810/A, 2N3811/A Monolithic Dual Matched PNP Transistor

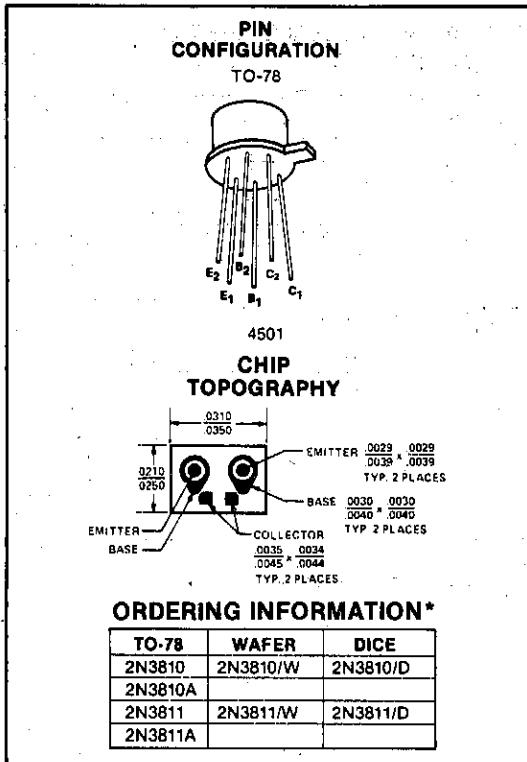
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## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Emitter-Base Voltage (Note 1) .....	-5V
Collector-Base or Collector-Emitter Voltage (Note 1) ...	-60V
Collector Current (Note 1) .....	50 mA
Storage Temperature Range .....	-65°C to +200°C
Operating Temperature Range .....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C

ONE SIDE	BOTH SIDES
500 mW	600 mW
Derate above 25°C .....	2.9 mW/°C    3.4 mW/°C



## ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

\*When ordering wafer/dice refer to Appendix B-23.

SYMBOL	PARAMETER	2N3810/A		2N3811/A		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX		IC = -10 μA, IE = 0	VCE = -5V, IC = -10 mA, IB = 0
BV <sub>CBO</sub>	Collector-Base Breakdown Voltage	-60		-60				
BV <sub>CEO</sub>	Collector-Emitter Breakdown Voltage (Note 2)	-60		-60		V	IC = -10 mA, IB = 0	IE = -10 μA, IC = 0
BV <sub>EBO</sub>	Emitter-Base Breakdown Voltage	-5		-5				
I <sub>C(off)</sub>	Collector Cutoff Current <small>TA = +150°C</small>		-10		-10	nA	V <sub>CB</sub> = -50V, IE = 0	
I <sub>E(off)</sub>	Emitter Cutoff Current		-20		-20	nA	V <sub>BE</sub> = 4V, IC = 0	
$\beta$	Static Forward Current Transfer Ratio (Note 2) <small>TA = -55°C</small>	100		225			IC = -10 μA	
		150	450	300	900		IC = -100 μA to -1 mA	
		125		250			IC = 10 mA	
		75		150			IC = 100 μA	
V <sub>BE(sat)</sub>	Base-Emitter Saturation Voltage (Note 2)		-0.7		-0.7	V	V <sub>CE</sub> = -5V, IB = -10 μA	
V <sub>CE(sat)</sub>	Collector-Emitter Saturation Voltage (Note 2)		-0.8		-0.8		IC = -100 μA, IB = -100 μA	
$h_{ie}$	Input Impedance	3	30	10	40	kΩ	IB = -10 μA, IC = -100 μA	
$h_{fe}$	Forward Current Transfer Ratio	150	600	300	900		IB = -100 μA, IC = -1 mA	
$h_{re}$	Reverse Voltage Transfer Ratio		0.25		0.25			
$h_{oe}$	Output Admittance	5	60	5	60	μmho		
$ h_{fe} $	Magnitude of small signal current gain	1	5	1	5		V <sub>CE</sub> = -5V	IC = -1mA, f = 100 MHz
		1		1				IC = -500 μA, f = 30 MHz

### NOTES:

1. Per transistor.
2. Pulse width ≤ 300 μs, duty cycle ≤ 2.0%.

# 2N3810/A, 2N3811/A

 **INTERSIL**

## ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

1

SYMBOL	PARAMETER	2N3810/A		2N3811/A		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
C <sub>obo</sub>	Output Capacitance	+4	4	+4	4		V <sub>CB</sub> = -5V, I <sub>E</sub> = 0, f = 100 MHz
C <sub>bo</sub>	Input Capacitance	8	8	8	8	pF	V <sub>CB</sub> = -0.5V, I <sub>C</sub> = 0, f = 100 KHz
$hFE_1 / hFE_2$	DC Current Gain Ratio	0.9	1.0	0.9	1.0		V <sub>CE</sub> = -5V, I <sub>C</sub> = 100 $\mu$ A
$ V_{BE1} - V_{BE2} $	Base-Emitter Voltage Differential	A devices 0.95	1.0	0.95	1.0	mV	V <sub>CE</sub> = -5V I <sub>C</sub> = 10 $\mu$ A to 10 mA
$\Delta V_{BE1} - V_{BE2}$	Base-Emitter Voltage Differential Gradient	A devices -5	-5	A devices -2.5	-2.5	$\mu$ V/ $^{\circ}$ C	I <sub>C</sub> = 100 $\mu$ A
$\Delta T$		A devices -3	-3	A devices -1.5	-1.5		V <sub>CE</sub> = -5, I <sub>C</sub> = 100 $\mu$ A
NF	Spot Noise Figure	A devices 10	10	A devices 5	5	dB	V <sub>CE</sub> = -10V, I <sub>C</sub> = -100 $\mu$ A, R <sub>G</sub> = 3 k $\Omega$ , f = 100 Hz, Noise Bandwidth = 20 Hz
			7		4		V <sub>CE</sub> = -10V, I <sub>C</sub> = -100 $\mu$ A, R <sub>G</sub> = 3 k $\Omega$ , f = 1 kHz, Noise Bandwidth = 200 kHz
			3		1.5		V <sub>CE</sub> = -10V, I <sub>C</sub> = -100 $\mu$ A, R <sub>G</sub> = 3 k $\Omega$ , f = 10 kHz, Noise Bandwidth = 2 kHz
			2.5		1.5		V <sub>CE</sub> = -10V, I <sub>C</sub> = -100 $\mu$ A, R <sub>G</sub> = 3 k $\Omega$ , Noise Bandwidth = 15.7 kHz (Note 3)
			3.5		2.5		

NOTES:

- 3 3 dB down at 10 Hz and 10 kHz.



# 2N3821, 2N3822 N-Channel JFET

## FEATURES

- Low Capacitance
- Up to 6500  $\mu\text{mho}$  Transconductance

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)	
Gate-Source Voltage	-50V
Gate-Drain Voltage	-50V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

1

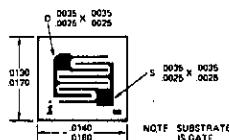
## PIN CONFIGURATION

TO-72



## CHIP TOPOGRAPHY

5003



## ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N3821	2N3821/W	2N3821/D
2N3822	2N3822/W	2N3822/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3821		2N3822		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
IGSS	Gate Reverse Current TA = 150°C	-0.1	-0.1	-0.1	-0.1	nA	VGS = -30 V, VDS = 0
BVGSS	Gate-Source Breakdown Voltage	-50	-50				Ig = -1 $\mu\text{A}$ , VDS = 0
VGS(off)	Gate-Source Cutoff Voltage	-4	-4	-6	-6	V	VDS = 15 V, ID = 0.5 nA
VGS	Gate-Source Voltage	-0.5	-2	-1	-4		VDS = 15 V, ID = 50 $\mu\text{A}$
IDSS	Saturation Drain Current	0.5	2.5	2	10	mA	VDS = 15 V, ID = 200 $\mu\text{A}$
gfs	Common-Source Forward Transconductance (Note 1)	1500	4500	3000	6500		VDS = 15 V, VGS = 0
yfs	Common-Source Forward Transadmittance	1500		3000		$\mu\text{mho}$	f = 1 kHz
gos	Common-Source Output Conductance (Note 1)		10		20		f = 100 MHz
Ciss	Common-Source Input Capacitance		6		6	pF	f = 1 kHz
Crss	Common-Source Reverse Transfer Capacitance		3		3		f = 1 MHz
NF	Noise Figure		5		5	dB	VDS = 15 V, VGS = 0, Rgen = 1 meg, BW = 5 Hz
en	Equivalent Input Noise Voltage		200		200	$\frac{nV}{\sqrt{\text{Hz}}}$	f = 10 Hz

Note 1: These parameters are measured during a 2 msec interval 100 msec after DC power is applied.



# 2N3823

## N-Channel JFET

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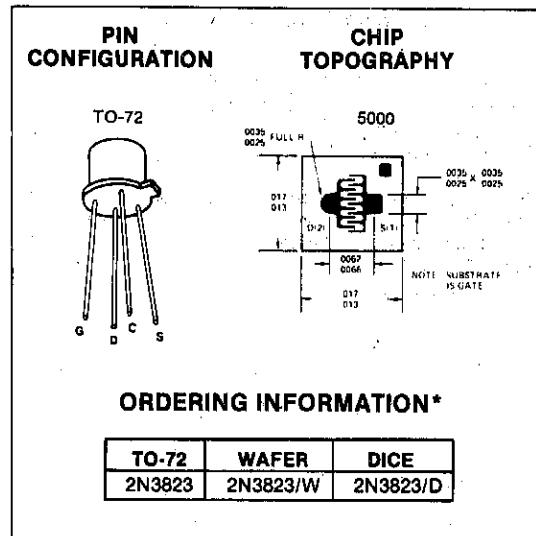
### FEATURES

- Low Noise
- Low Capacitance
- Transconductance up to 6500  $\mu\text{mho}$

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage	.....	-30V
Gate Current	.....	10 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	300 mW
Derate above 25°C	.....	1.7 mW/°C



\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS	
$I_{GSS}$	Gate Reverse Current ( $T_A = 150^\circ\text{C}$ )	-0.5	nA	$V_{GS} = -20\text{V}$ , $V_{DS} = 0$	
$BV_{GSS}$	Gate-Source Breakdown Voltage	-30	$\mu\text{A}$	$I_G = 1 \mu\text{A}$ , $V_{DS} = 0$	
$V_{GS(\text{off})}$	Gate-Source Cutoff Voltage	-8	V	$V_{DS} = 15\text{V}$ , $I_D = 0.5 \text{nA}$	
$V_{GS}$	Gate-Source Voltage	-1.0	-7.5	$V_{DS} = 15\text{V}$ , $I_D = 400 \mu\text{A}$	
$I_{DSS}$	Saturation Drain Current	4	20	$V_{DS} = 15\text{V}$ , $V_{GS} = 0$	
$g_{fs}$	Common-Source Forward Transconductance	3,500	6,500	$V_{DS} = 15\text{V}$ , $V_{GS} = 0$	$f = 1 \text{kHz}$ (Note 1)
$ Y_{fs} $	Common-Source Forward Transadmittance	3,200			$f = 100 \text{MHz}$
$g_{os}$	Common-Source Output Transconductance		35		$f = 1 \text{kHz}$ (Note 1)
$g_{iss}$	Common-Source Input Conductance		800		$f = 200 \text{MHz}$
$g_{oss}$	Common-Source Output Conductance		200	$R_G = 1 \text{k}\Omega$	$f = 1 \text{MHz}$
$C_{iss}$	Common-Source Input Capacitance		6		
$C_{rss}$	Common-Source Reverse Transfer Capacitance		2		
NF	Noise Figure		2.5	dB	$V_{DS} = 15\text{V}$ , $V_{GS} = 0$

NOTE 1: These parameters are measured during a 2 msec interval 100 msec after DC power is applied.

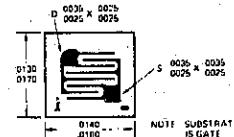
**FEATURES**

- $r_{ds} < 250$  ohms
- $I_{D(off)} < 0.1$  nA

**ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)	
Gate-Source or Gate-Drain Voltage	-50V
Gate Current	10 mA
Storage Temperature Range	-65°C to -200°C
Operating Temperature Range	-55°C to +150°C
Load Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

**PIN CONFIGURATION**      **CHIP TOPOGRAPHY**
**TO-72**

**5003**

**ORDERING INFORMATION\***

<b>TO-72</b>	<b>WAFER</b>	<b>DICE</b>
2N3824	2N3824/W	2N3824/D

\*When ordering wafer/dice refer to Appendix B-23.

**ELECTRICAL CHARACTERISTICS**
**TEST CONDITIONS:** 25°C unless otherwise noted

<b>PARAMETER</b>		<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>	<b>TEST CONDITIONS</b>	
I <sub>GSS</sub>	Gate Reverse Current		-0.1	nA		V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0
			-0.1	μA		
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-50		V	I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0	
I <sub>D(off)</sub>	Drain Cutoff Current		0.1	nA		V <sub>DS</sub> = 15V, V <sub>GS</sub> = -8V
			0.1	μA		
V <sub>ds(on)</sub>	Drain-Source ON Resistance	250		Ω	V <sub>GS</sub> = 0V, I <sub>D</sub> = 0	f = 1 kHz
C <sub>iss</sub>	Common-Source Input Capacitance	6		pF	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0	f = 1 MHz
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	3			V <sub>GS</sub> = -8V, V <sub>DS</sub> = 0	



# 2N3921, 2N3922 Monolithic Dual N-Channel JFET

## FEATURES

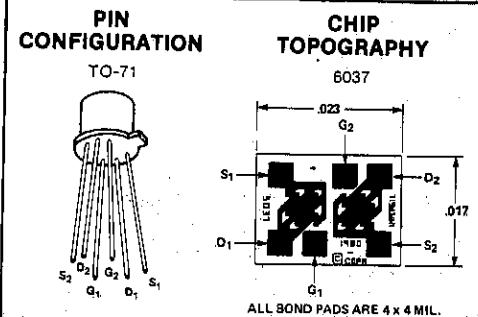
- Low Drain Current
- High Output Impedance
- Matched  $V_{GS}$ ,  $\Delta V_{GS}$ , and  $g_{fs}$

1

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	-50V
Gate Current (Note 1)	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Load Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C



## ORDERING INFORMATION\*

TO-71	WAFER	DICE
2N3921	2N3921/W	2N3921/D
2N3922	2N3922/W	2N3922/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: ( $25^\circ\text{C}$  unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I <sub>GSSR</sub>	Gate Reverse Current		-1	nA		
BV <sub>DGO</sub>	Drain-Gate Breakdown Voltage		50			
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage		-3	V		
V <sub>GS</sub>	Gate-Source Voltage	-0.2	-2.7			
I <sub>G</sub>	Gate Operating Current		-250	pA		
I <sub>DSS</sub>	Saturation Drain Current (Note 1)	1	10	mA		
g <sub>fs</sub>	Common-Source Forward Transconductance (Note 2)	1500	7500	μmho		
g <sub>os</sub>	Common-Source Output Conductance		35			
C <sub>iss</sub>	Common-Source Input Capacitance		18	pF		
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance		6			
g <sub>fs</sub>	Common-Source Forward Transconductance	1500		μmho		
g <sub>oss</sub>	Common-Source Output Conductance		20		V <sub>DG</sub> = 10V, I <sub>D</sub> = 700 μA	f = 1 kHz
NF	Spot Noise Figure		2	dB	V <sub>DG</sub> = 10V, V <sub>GS</sub> = 0	f = 1 kHz, R <sub>G</sub> = 1 meg

MATCHING CHARACTERISTICS	2N3921		2N3922		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX		
V <sub>Gs1</sub> -V <sub>Gs2</sub>	Differential Gate-Source Voltage		5		mV	
Δ V <sub>Gs1</sub> -V <sub>Gs2</sub>	Gate-Source Differential Voltage Change with Temperature		10		μV/°C	
AT				25		V <sub>DG</sub> = 10V, I <sub>D</sub> = 700 μA, TA = 0°C, TB = 100°C
g <sub>fs2</sub>	Transconductance Ratio	0.95	1.0	0.95	1.0	f = 1 kHz

NOTES: 1. Per transistor.

2. Pulse test duration = 2 ms.

# 2N3954-2N3958

## Monolithic Dual N-Channel JFET

1

### FEATURES

- Low Offset and Drift
- Low Capacitance
- Low Noise
- Superior Tracking Ability
- Low Output Conductance

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

#### Gate-Source or Gate-Drain

Breakdown Voltage (Note 1) ..... 50V

Any Pin to Case Voltage ..... 100V

Gate Current (Note 1) ..... 50 mA

Storage Temperature ..  $-65^\circ\text{C}$  to  $+200^\circ\text{C}$

Operating Temperature ..  $-55^\circ\text{C}$  to  $+150^\circ\text{C}$

#### Lead Temperature

(Soldering, 10 sec.) .....  $+300^\circ\text{C}$

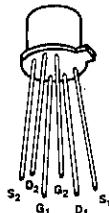
ONE BOTH  
SIDE SIDES

Power Dissipation 250 mW 500 mW

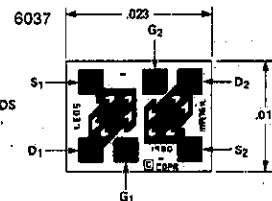
Derate above  $25^\circ\text{C}$  2.8 mW/ $^\circ\text{C}$  4.3 mW/ $^\circ\text{C}$

### PIN CONFIGURATION

TO-71



### CHIP TOPOGRAPHY



### ORDERING INFORMATION\*

TO-71	WAFER	DICE
2N3954	2N3954/W	2N3954/D
2N3954A	2N3954A/W	2N3954A/D
2N3955	2N3955/W	2N3955/D
2N3955A	2N3955A/W	2N3955A/D
2N3956	2N3956/W	2N3956/D
2N3957	2N3957/W	2N3957/D
2N3958	2N3958/W	2N3958/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER	2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$ I_{GSSR} $	Gate Reverse Current	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	nA	$V_{GS} = -30\text{ V}$ , $V_{DS} = 0$	
		$T_A = 125^\circ\text{C}$		-500	-500	-500	-500	-500	-600	-500	-500	-500	-500	-500	nA		
$B/V_{GSS}$	Gate-Source Breakdown Voltage	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50		$V_{DS} = 0$ , $I_G = -1\text{ }\mu\text{A}$	
$V_{GS(\text{off})}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	V	$V_{DS} = 20\text{ V}$ , $I_D = 1\text{ nA}$	
$V_{GS(f)}$	Gate-Source Forward Voltage	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0		$V_{DS} = 0$ , $I_G = 1\text{ mA}$	
$V_{GS}$	Gate-Source Voltage	-4.2	-4.2	-4.2	-4.2	-4.2	-4.2	-4.2	-4.2	-4.2	-4.2	-4.2	-4.2	-4.2		$V_{DS} = 20\text{ V}$ , $I_D = 50\text{ }\mu\text{A}$	
$I_G$	Gate Operating Current	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	nA	$V_{DS} = 20\text{ V}$ , $I_D = 200\text{ }\mu\text{A}$	
		$T_A = 125^\circ\text{C}$		-250	-250	-250	-250	-250	-250	-250	-250	-250	-250	-250	nA		
$ I_{DSS} $	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	mA	$V_{DS} = 20\text{ V}$ , $V_{GS} = b$	
$\%f_s$	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000		$f = 1\text{ kHz}$ $f = 200\text{ MHz}$	
$g_{os}$	Common-Source Output Conductance	35	35	35	35	36	35	35	35	35	35	35	35	35		$f = 1\text{ kHz}$	
$C_{iss}$	Common-Source-Input Capacitance	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	pF	$V_{GS} = 0$	
$C_{rss}$	Common-Source Reverse Transfer Capacitance	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2		$f = 1\text{ MHz}$	
$C_{dg0}$	Drain-Gate Capacitance	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5		$V_{DG} = 10\text{ V}$ , $I_S = 0$	
$NF$	Common-Source Spot Noise Figure	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	dB	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$ , $R_G = 10\text{ M}\Omega$	
$ I_{G1}-I_{G2} $	Differential Gate Current	10	10	10	10	10	10	10	10	10	10	10	10	10	nA	$T = 125^\circ\text{C}$	
$ I_{DSS1}-I_{DSS2} $	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95		$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$	
$ V_{GS1}-V_{GS2} $	Differential Gate-Source Voltage	5.0	5.0	10.0	5.0	5.0	15	5.0	20	5.0	25	5.0	25	5.0	mV	$V_{DS} = 20\text{ V}$ , $I_D = 200\text{ }\mu\text{A}$	
$\Delta V_{GS1}-V_{GS2} $	Gate-Source Differential Voltage Change with Temperature	0.8	0.4	2.0	1.2	4.0	6.0	8.0	10.0	7.5	10.0					$T = 25^\circ\text{C}$ to $-55^\circ\text{C}$	
$\Delta T$		1.0	0.5	2.5	1.5	5.0	7.5	10.0								$T = 25^\circ\text{C}$ to $125^\circ\text{C}$	
$g_{fs1}/g_{fs2}$	Transconductance Ratio	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0		$f = 1\text{ kHz}$

NOTE 1: Per transistor.



# 2N3970-2N3972

## N-Channel JFET

### FEATURES

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- Low  $r_{DS(on)}$
- $I_D(off) < 250 \text{ pA}$
- Fast Switching

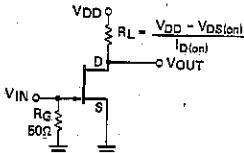
### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)	
Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering; 10 sec.)	+300°C
Power Dissipation	1.8W
Derate above 25°C	10 mW/°C

### ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETER	2N3970		2N3971		2N3972		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
BV <sub>GSS</sub> Gate Reverse Breakdown Voltage	-40		-40		-40		V	$I_G = -1\mu\text{A}, V_{DS} = 0$
$I_{DGO}$ Drain Reverse Current			250	250	250	250	pA	$V_{DG} = 20\text{V}, I_S = 0$
	$T_A = 150^\circ\text{C}$		500	500	500	500	nA	
$I_{D(off)}$ Drain Cutoff Current			250	250	250	250	pA	$V_{DG} = 20\text{V}, V_{GS} = -12\text{V}$
	$T_A = 150^\circ\text{C}$		500	500	500	500	nA	
$V_{GS(off)}$ Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	$V_{DS} = 20\text{V}, I_D = 1\text{nA}$
$I_{DSS}$ Saturation Drain Current	50	150	25	75	5	30	mA	$V_{DS} = 20\text{V}, V_{GS} = 0$
(Pulse width 300μs, duty cycle ≤ 3%)								
$V_{DS(on)}$ Drain-Source ON Voltage					2		V	$I_D = 5\text{ mA}$
				1.5				$I_D = 10\text{ mA}$
		1						$I_D = 20\text{ mA}$
$r_{DS(on)}$ Static Drain-Source ON Resistance	30		60		100		$\Omega$	$V_{GS} = 0, I_D = 1\text{ mA}$
$r_{ds(on)}$ Drain-Source ON Resistance	30		60		100			$V_{GS} = 0, I_D = 0$
$C_{iss}$ Common-Source Input Capacitance	25		25		25			$f = 1\text{ kHz}$
$C_{rss}$ Common-Source Reverse Transfer Capacitance	6		6		6		pF	$V_{DS} = 20\text{V}, V_{GS} = 0$
								$V_{DS} = 0, V_{GS} = -12\text{V}$
								$f = 1\text{ MHz}$
$t_d$ Turn-On Delay Time		10		15		40		$V_{DD} = 10\text{V}, V_{GS(on)} = 0$
$t_r$ Rise Time		10		15		40	ns	$I_{D(on)}$
$t_{off}$ Turn-Off Time		30		60		100		$V_{GS(off)}$
								$R_L$
								2N3970 20 mA
								-10V 450Ω
								2N3971 10 mA
								-5V 850Ω
								2N3972 5 mA
								-3V 1.6kΩ



$V_{DD} = \frac{V_{DD} - V_{DS(on)}}{I_{D(on)}}$

INPUT PULSE

RISE TIME 0.25 ns

FALL TIME 0.75 ns

PULSE WIDTH 200 ns

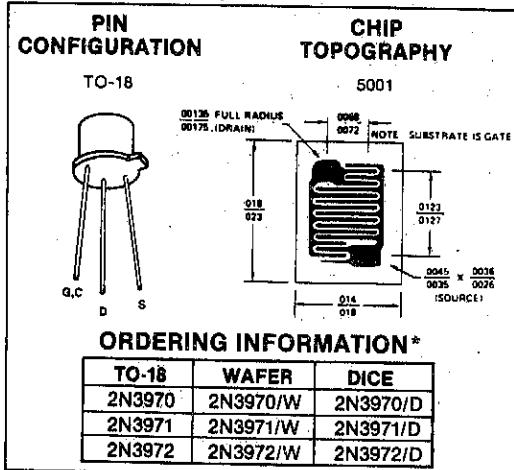
PULSE RATE 550 pps

SAMPLING SCOPE

RISE TIME 0.4 ns

INPUT RESISTANCE 10 M

INPUT CAPACITANCE 1.5 pF



### ORDERING INFORMATION\*

TO-18	WAFER	DICE
2N3970	2N3970/W	2N3970/D
2N3971	2N3971/W	2N3971/D
2N3972	2N3972/W	2N3972/D

\*When ordering wafer/dice refer to Appendix B-23.

## FEATURES

- Low  $r_{DS(on)}$
- High  $Y_{fs}/C_{iss}$  Ratio (High-Frequency Figure-of-Merit)

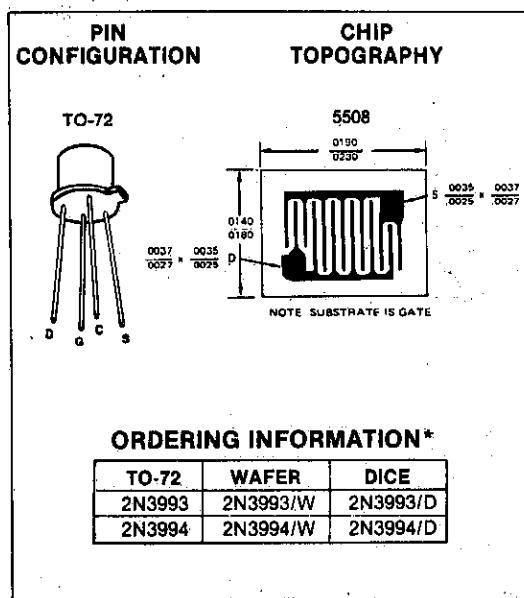
## APPLICATIONS

Used in high-speed commutator and chopper applications. Also ideal for "Virtual Gnd" switching; needs no ext. translator circuit to switch  $\pm 10$  VAC. Can be driven direct from T<sup>2</sup>L or CMOS logic.

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Drain-Gate Voltage	.....	-25V
Drain-Source Voltage	.....	-25V
Continuous Forward Gate Current	.....	-10 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	300 mW
Derate above 25°C	.....	1.7 mW/°C



\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature (unless otherwise noted)

SYMBOL	PARAMETER	2N3993		2N3994		UNIT	TEST CONDITIONS (Note 3)
		MIN	MAX	MIN	MAX		
BVGSS	Gate-Source Breakdown Voltage	25		25		V	$I_G = 1 \mu\text{A}, V_{DS} = 0$
IDGO	Drain Reverse Current		-1.2	-1.2	nA	$V_{DG} = -15 \text{ V}, I_S = 0$	
			-1.2	-1.2	$\mu\text{A}$	$V_{DG} = -15 \text{ V}, I_S = 0, T_A = 150^\circ\text{C}$	
IDSS	Zero-Gate-Voltage Drain Current	-10		-2		mA	$V_{DS} = -10 \text{ V}, V_{GS} = 0, (\text{See Note 1})$
ID(off)	Drain Cutoff Current			-1.2	nA	$V_{DS} = -10 \text{ V}, V_{GS} = 6 \text{ V}$	
				-1	$\mu\text{A}$	$V_{DS} = -10 \text{ V}, V_{GS} = 6 \text{ V}, T_A = 150^\circ\text{C}$	
			-1.2		nA	$V_{DS} = -10 \text{ V}, V_{GS} = 10 \text{ V}$	
			-1		$\mu\text{A}$	$V_{DS} = -10 \text{ V}, V_{GS} = 10 \text{ V}, T_A = 150^\circ\text{C}$	
		4	9.5	1	5.5	V	$V_{DS} = -10 \text{ V}, I_D = -1 \mu\text{A}$
rds(on)	Small-Signal Drain-Source On-State Resistance		150		300	$\Omega$	$V_{GS} = 0, I_D = 0, f = 1 \text{ kHz}$
Yfs	Small-Signal Common-Source Forward Transfer Admittance	6	12	4	10	mmho	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ kHz}, (\text{See Note 1})$
Ciss	Common-Source Short-Circuit Input Capacitance			16		pF	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}, (\text{See Note 2})$
Crss	Common-Source Short-Circuit Reverse Transfer Capacitance			5	pF		$V_{DS} = 0, V_{GS} = 6 \text{ V}, f = 1 \text{ MHz}$
			4.5		pF		$V_{DS} = 0, V_{GS} = 10 \text{ V}, f = 1 \text{ MHz}$

NOTES: 1. These parameters must be measured using pulse techniques.  $t_p = 100 \text{ ms}$ , duty cycle  $\leq 10\%$ .

2. This parameter must be measured with bias voltage applied for less than 5 seconds to avoid overheating.

3. The case should be connected to the source for all measurements.

**INTERSIL**

# 2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880 Dielectrically Isolated Dual NPN Transistor

**1**

## FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good  $h_{FE}$  Match
- Tight  $V_{BE}$  Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers.

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ C$  unless otherwise noted)

### Collector-Base or Collector-Emitter Voltage (Note 1)

2N4044, 2N4878	.....	60V
2N4100, 2N4879	.....	55V
2N4045, 2N4880	.....	45V

### Collector-Collector Voltage

..... 100V

### Emitter-Base Voltage (Note 2)

..... 7V

### Collector Current (Note 1)

..... 10 mA

### Storage Temperature Range

..... -65°C to +200°C

### Operating Temperature Range

..... -55°C to +150°C

### Lead Temperature (Soldering, 10 sec.)

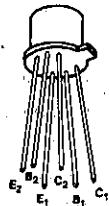
..... +300°C

TO-71                    TO-78

	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power				
Dissipation ..	300 mW	500 mW	400 mW	750 mW
Derate above 25°C (mW/°C) ....	1.7	2.9	2.3	4.3

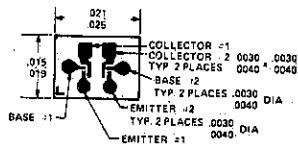
## PIN CONFIGURATION

TO-71  
TO-78



## CHIP TOPOGRAPHY

4000



## ORDERING INFORMATION\*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ C$ unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
$h_{FE}$	DC Current Gain	200	600	150	600	80	800	V	$I_C = 10 \mu A, V_{CE} = 5V$
		225		175		100			$I_C = 1.0 \text{ mA}, V_{CE} = 5V$
	$T_A = -55^\circ C$	75		50		30			$I_C = 10 \mu A, V_{CE} = 5V$
									$I_C = 1.0 \text{ mA}, I_B = 0.1 \text{ mA}$
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7		
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35		
$I_{CBO}$	Collector Cutoff Current		0.1		0.1		0.1*	nA	$I_E = 0, V_{CB} = 45V, 30V^*$
		$T_A = 150^\circ C$		0.1		0.1	0.1*		$\mu A$
$I_{EBO}$	Emitter Cutoff Current		0.1		0.1		0.1	nA	$I_C = 0, V_{EB} = 5V$
$C_{obo}$	Output Capacitance		0.8		0.8		0.8	pF	$I_E = 0, V_{CB} = 5V$

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
$C_{te}$	Emitter Transition Capacitance	1	1	1	1	1	pF	$I_C = 0, V_{EB} = 0.5V$
$C_{C1}, C_2$	Collector to Collector Capacitance	0.8	0.8	0.8	0.8	0.8	pF	$V_{CC} = 0$
$I_{C1}, I_{C2}$	Collector to Collector Leakage Current	5	5	5	5	5	pA	$V_{CC} = \pm 100V$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60	55	45	45	45	V	$I_C = 1mA, I_B = 0$
$f_T$	Current Gain Bandwidth Product	200	150	150	150	150	MHz	$I_C = 1mA, V_{CE} = 10V$
$f_T$	Current Gain Bandwidth Product	20	15	15	15	15	MHz	$I_C = 10\mu A, V_{CE} = 10V$
NF	Narrow Band Noise Figure	2	3	3	3	3	dB	$I_C = 10\mu A, V_{CE} = 5V, f = 1kHz$ $R_G = 10 \text{ kohms}$ $BW = 200 \text{ Hz}$
$BV_{CBO}$	Collector Base Breakdown Voltage	60	55	45	45	45	V	$I_C = 10\mu A, I_E = 0$
$BV_{EBO}$	Emitter Base Breakdown Voltage	7	7	7	7	7	V	$I_E = 10\mu A, I_C = 0$

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

$h_{FE1}/h_{FE2}$	DC Current Gain Ratio (Note 3)	0.9	1	0.85	1	0.8	1		$I_C = 10\mu A \text{ to } 1mA, V_{CE} = 5V$
$ V_{BE1}-V_{BE2} $	Base Emitter Voltage Differential	3	3	5	5	5	5	mV	$I_C = 10\mu A, V_{CE} = 5V$
$ I_{B1}-I_{B2} $	Base Current Differential	5	5	10	10	25	25	nA	$I_C = 10\mu A, V_{CE} = 5V$
$ \Delta(V_{BE1}-V_{BE2}) /\Delta T$	Base Emitter Voltage Differential Change with Temperature	3	3	5	5	10	10	$\mu V/\text{ }^\circ C$	$I_C = 10\mu A, V_{CE} = 5V$ $T_A = -55 \text{ }^\circ C \text{ to } +125 \text{ }^\circ C$
$ \Delta(I_{B1}-I_{B2}) /\Delta T$	Base Current Differential Change with Temperature	0.3	0.3	-0.5	-0.5	1	1	nA/ $\text{ }^\circ C$	

SMALL SIGNAL CHARACTERISTICS

PARAMETER	TYPICAL VALUE	UNIT	TEST CONDITIONS
$h_{ib}$	Input Resistance	28	ohms
$h_{rb}$	Voltage Feedback Ratio	43	$\times 10^{-3}$
$h_{fe}$	Small Signal Current Gain	250	
$h_{ob}$	Output Conductance	60	$\mu \text{mhos}$
$h_{ie}$	Input Resistance	9.6	k ohms
$h_{re}$	Voltage Feedback Ratio	42	$\times 10^{-3}$
$h_{oe}$	Output Conductance	12	$\mu \text{mhos}$

NOTES:

1. Per transistor.
2. The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10  $\mu$ amps.
3. The lowest of two  $h_{FE}$  readings is taken as  $h_{FE1}$  for purposes of this ratio.



# ITE4091-ITE4093 2N4091-2N4093, JANTX\* N-Channel JFET

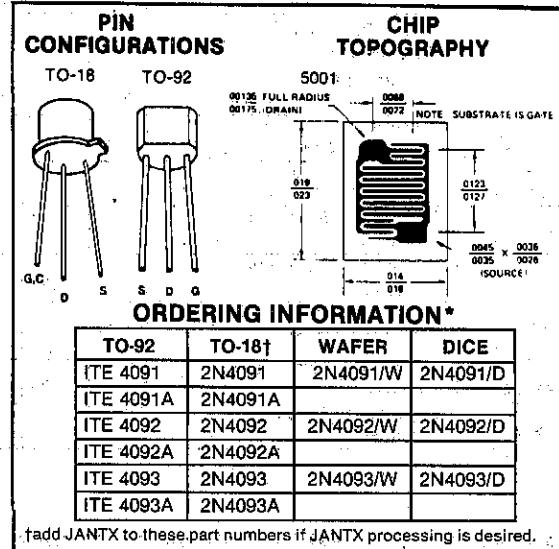
## FEATURES

- Low  $r_{DS(on)}$
- $I_D(OFF) < 100 \mu A$  (JAN TX Types)
- Fast Switching

1

## ABSOLUTE MAXIMUM RATINGS

	TO-18	TO-92
Power Dissipation	1.8W	360 mW
Derate above $25^\circ C$	$1.7 \text{ mW}/^\circ C$	$3.0 \text{ mW}/^\circ C$
Gate-Source or Gate-Drain Voltage	... -40V	...
Gate Current	... 10mA	...
Storage Temperature Range	... $-65^\circ C$ to $+200^\circ C$	...
Operating Temperature Range	... $-55^\circ C$ to $+150^\circ C$	...
Lead Temperature (Soldering, 10 sec.)	... $+300^\circ C$	...



\*Add JANTX to these part numbers if JANTX processing is desired.

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ C$ unless otherwise noted)

PARAMETER	2N/ITE 4091						2N/ITE 4092						2N/ITE 4093						Test Conditions
	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Min.	Max.	Min.	Max.	Unit	Min.	Max.	Unit	Min.	Max.	Unit	
$VB_{GS}$	Gate-Source Breakdown Voltage	-40	-40	-40	-40	-	V	-	-	-	-	-	-	-	-	-	-	-	$I_G = -1 \mu A, V_{DS} = 0$
$I_{DG0}$	Drain Reverse Current (Not JANTX Specified) $T_A = 150^\circ C$	200	200	200	200	200	pA	-	-	-	-	-	-	-	-	-	-	-	$V_{GD} = -20V, I_S = 0$
$I_{GSS}$	Gate Reverse Current (JANTX, ITE devices only); $T_A = 150^\circ C$	-100	-100	-100	-100	-100	pA	-	-	-	-	-	-	-	-	-	-	-	$V_{GS} = -20V, V_{DS} = 0$
$I_{D(OFF)}$	JANTX: $T_A = 25^\circ C$	100	100	100	100	100	pA	-	-	-	-	-	-	-	-	-	-	-	$V_{DS} = 20V, V_{GS} = -12V(4091)$
	JANTX, $T_A = 150^\circ C$	200	200	200	200	200	pA	-	-	-	-	-	-	-	-	-	-	-	$V_{GS} = -8V(4092)$
	JANTX, $T_A = 150^\circ C$	400	400	400	400	400	nA	-	-	-	-	-	-	-	-	-	-	-	$V_{GS} = -8V(4093)$
$V_P$	Gate-Source Pinch-Off Voltage	-5	-10	-2	-7	-1	-5	V	-	-	-	-	-	-	-	-	-	-	$V_{DS} = 20V, I_D = 1 nA$
$I_{DSS}$	Drain Current at Zero Gate Voltage	30	-	15	-	8	-	mA	-	-	-	-	-	-	-	-	-	-	$V_{DS} = 20V, V_{GS} = 0,$ Pulse Test Duration = 2 ms
$V_{DS(ON)}$	Drain-Source ON Voltage	-	-	-	-	-	0.2	V	-	-	-	-	-	-	-	-	-	-	$I_D = 2.5 \text{ mA}$
		-	-	-	-	-	0.2	V	-	-	-	-	-	-	-	-	-	-	$I_D = 4 \text{ mA}$
		-	-	-	-	-	0.2	V	-	-	-	-	-	-	-	-	-	-	$I_D = 6.6 \text{ mA}$
$r_{DS(on)}$	Static Drain-Source ON Resistance	30	-	50	-	80	-	$\Omega$	-	-	-	-	-	-	-	-	-	-	$V_{GS} = 0, I_D = 1 \text{ mA}$
$r_{ds(on)}$	Static Drain-Source ON Resistance	30	-	50	-	80	$\Omega$	$\Omega$	-	-	-	-	-	-	-	-	-	-	$V_{GS} = 0, I_D = 1 \text{ mA}, f = 1 \text{ kHz}$
$C_{iss}$	Common-Source Input Capacitance	16	-	16	-	16	-	pF	-	-	-	-	-	-	-	-	-	-	$V_{DS} = 20V, V_{GS} = 0, f = 1 \text{ MHz}$
$C_{rss}$	JANTX Only	5	-	.5	-	5	-	pF	-	-	-	-	-	-	-	-	-	-	$V_{DS} = 0, V_{GS} = -20V, f = 1 \text{ MHz}$
	Common-Source Reverse Transfer Capacitance	5	-	.5	-	5	-	pF	-	-	-	-	-	-	-	-	-	-	$V_{DS} = -0, V_{GS} = -20V, f = 1 \text{ MHz}$
$t_d(ON)$	Turn-ON Delay Time	15	-	15	-	20	-	ns	-	-	-	-	-	-	-	-	-	-	$V_{DD} = 3V, V_{GS(ON)} = 0$
$t_r$	Rise Time	10	-	20	-	40	-	ns	-	-	-	-	-	-	-	-	-	-	$I_{D(on)} = 5.6 \text{ mA}, V_{GS} = -12V$
$t_{off}$	Turn-OFF-Time	40	-	60	-	80	-	ns	-	-	-	-	-	-	-	-	-	-	$I_{D(on)} = 4 \text{ mA}, V_{GS} = -8V$
																		$I_{D(on)} = 2.5 \text{ mA}, V_{GS} = -8V$	



# 2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880 **Dielectrically Isolated Dual NPN Transistor**

1

## FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good  $h_{FE}$  Match
- Tight  $V_{BE}$  Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers.

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

### Collector-Base or Collector-Emitter Voltage (Note 1)

2N4044, 2N4878	60V
2N4100, 2N4879	55V
2N4045, 2N4880	45V

### Collector-Collector Voltage

100V

### Emitter-Base Voltage (Note 2)

7V

### Collector Current (Note 1)

10 mA

### Storage Temperature Range

-65°C to +200°C

### Operating Temperature Range

-55°C to +150°C

### Lead Temperature (Soldering, 10 sec.)

+300°C

### TO-71                  TO-78

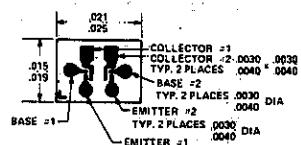
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation ..	300 mW	500 mW	400 mW	750 mW
Derate above 25°C (mW/°C) ....	1.7	2.9	2.3	4.3

## PIN CONFIGURATION

TO-71  
TO-78

## CHIP TOPOGRAPHY

4000



## ORDERING INFORMATION\*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044		2N4100		2N4045		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
$h_{FE}$	DC Current Gain	200	600	150	600	80	800	V	$I_C = 10 \mu A, V_{CE} = 5 V$
		225		175		100			$I_C = 1.0 \text{ mA}, V_{CE} = 5 V$
	$T_A = -55^{\circ}\text{C}$	75		50		30			$I_C = 10 \mu A, V_{CE} = 5 V$
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7		
$V_{CE(sat)}$	Collector Saturation Voltage	0.35		0.35		0.35			$I_C = 1.0 \text{ mA}, I_B = 0.1 \text{ mA}$
$I_{CBO}$	Collector Cutoff Current	0.1		0.1		0.1*		nA	$I_E = 0, V_{CB} = 45 V, 30 V^*$
		$T_A = 150^{\circ}\text{C}$	0.1		0.1		0.1*		
$I_{EBO}$	Emitter Cutoff Current		0.1		0.1		0.1	nA	$I_C = 0, V_{EB} = 5 V$
Cobo	Output Capacitance		0.8		0.8		0.8	pF	$I_E = 0, V_{CB} = 5 V$

**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

PARAMETER	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
C <sub>te</sub>	Emitter Transition Capacitance		1		1		pF	I <sub>C</sub> = 0, V <sub>EB</sub> = 0.5V
C <sub>CC1, C<sub>2</sub></sub>	Collector to Collector Capacitance		0.8		0.8		pF	V <sub>CC</sub> = 0
I <sub>C1, C<sub>2</sub></sub>	Collector to Collector Leakage Current		5		5		pA	V <sub>CC</sub> = ±100V
V <sub>CEO(sust)</sub>	Collector to Emitter Sustaining Voltage	60		55		45	V	I <sub>C</sub> = 1mA, I <sub>B</sub> = 0
f <sub>t</sub>	Current Gain Bandwidth Product	200		150		150	MHz	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 10V
f <sub>t</sub>	Current Gain Bandwidth Product	20		15		15	MHz	I <sub>C</sub> = 10µA, V <sub>CE</sub> = 10V
NF	Narrow Band Noise Figure		2		3		3	dB
BV <sub>CBO</sub>	Collector Base Breakdown Voltage	60		55		45	V	I <sub>C</sub> = 10µA, V <sub>CE</sub> = 5V
BV <sub>EBO</sub>	Emitter Base Breakdown Voltage	7		7		7	V	I <sub>E</sub> = 10µA, I <sub>C</sub> = 0

**MATCHING CHARACTERISTICS (25°C unless otherwise noted)**

h <sub>FE1</sub> /h <sub>FE2</sub>	DC Current Gain Ratio (Note 3)	0.9	1	0.85	1	0.8	1	I <sub>C</sub> = 10µA to 1mA, V <sub>CE</sub> = 5V
V <sub>BE1</sub> -V <sub>BE2</sub>	Base Emitter Voltage Differential		3		5		5	mV I <sub>C</sub> = 10µA, V <sub>CE</sub> = 5V
I <sub>B1</sub> -I <sub>B2</sub>	Base Current Differential		5		10		25	nA I <sub>C</sub> = 10µA, V <sub>CE</sub> = 5V
Δ(V <sub>BE1</sub> -V <sub>BE2</sub> )/ΔT	Base Emitter Voltage Differential Change with Temperature		3		5		10	µV/°C I <sub>C</sub> = 10µA, V <sub>CE</sub> = 5V
Δ(I <sub>B1</sub> -I <sub>B2</sub> )/ΔT	Base Current Differential Change with Temperature		0.3		0.5		1	nA/°C TA = -55°C to +125°C

**SMALL SIGNAL CHARACTERISTICS**

PARAMETER		TYPICAL VALUE	UNIT	TEST CONDITIONS
<i>h</i> <sub>ib</sub>	Input Resistance	28	ohms	I <sub>C</sub> = 1mA, V <sub>CB</sub> = 5V
<i>h</i> <sub>rb</sub>	Voltage Feedback Ratio	43	×10 <sup>-3</sup>	
<i>h</i> <sub>fe</sub>	Small Signal Current Gain	250		
<i>h</i> <sub>ob</sub>	Output Conductance	60	µmhos	
<i>h</i> <sub>eb</sub>	Input Resistance	9.6	k ohms	
<i>h</i> <sub>re</sub>	Voltage Feedback Ratio	42	×10 <sup>-3</sup>	
<i>h</i> <sub>oe</sub>	Output Conductance	12	µmhos	

**NOTES:**

1. Per transistor.
2. The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10 µamps.
3. The lowest of two h<sub>FE</sub> readings is taken as h<sub>FE1</sub> for purposes of this ratio.

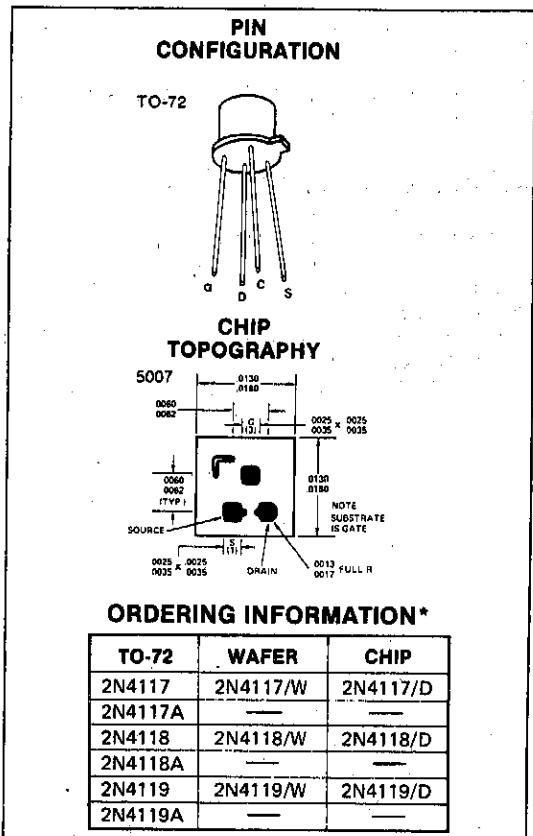
**FEATURES**

- Low Leakage
- Low Capacitance

**ABSOLUTE MAXIMUM RATINGS**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage .....	-40V
Gate Current .....	50 mA
Storage Temperature Range .....	-65°C to +200°C
Operating Temperature Range .....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C
Power Dissipation .....	300 mW
Derate above 25°C .....	1.7 mW/°C



\*When ordering wafer/dice refer to Appendix B-23.

**ELECTRICAL CHARACTERISTICS** ( $25^\circ\text{C}$  unless otherwise noted)

PARAMETER	2N4117		2N4118		2N4119		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-40	-40	-40	-40	-40	V	$I_G = -1 \mu\text{A}, V_{DS} = 0$
$I_{GSSR}$	Gate Reverse Current A devices	-10	-10	-10	-10	-10	pA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$
		-1	-1	-1	-1	-1		
	$T_A = +100^\circ\text{C}$ A devices	-25	-25	-25	-25	-25	nA	
		-2.5	-2.5	-2.5	-2.5	-2.5		
V <sub>GS</sub> (off)	Gate-Source Pinch-Off Voltage	-0.6	-1.8	-1	-3	-2	-6	V
$I_{DSS}$	Drain Current at Zero Gate Voltage (Note 1)	0.02	0.09	0.08	0.24	0.20	0.60	mA
$g_{fs}$	Common-Source Forward Transconductance (Note 1)	70	210	80	250	100	330	$\text{V}_{DS} = 10 \text{ V}$ , $f = 1 \text{ kHz}$
$g_{fs}$	Common-Source Forward Transconductance	60		70		90		$V_{GS} = 0, f = 30 \text{ MHz}$
$g_{os}$	Common-Source Output Conductance		3		5		10	$\text{V}_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ kHz}$
$C_{iss}$	Common-Source Input Capacitance		3		3		3	$\text{V}_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ kHz}$
$C_{rss}$	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5	$\text{V}_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ kHz}$

NOTE: 1. Pulse test: Pulse duration of 2 ms used during test.



# 2N4220 - 2N4222

## N-Channel JFET

### FEATURES

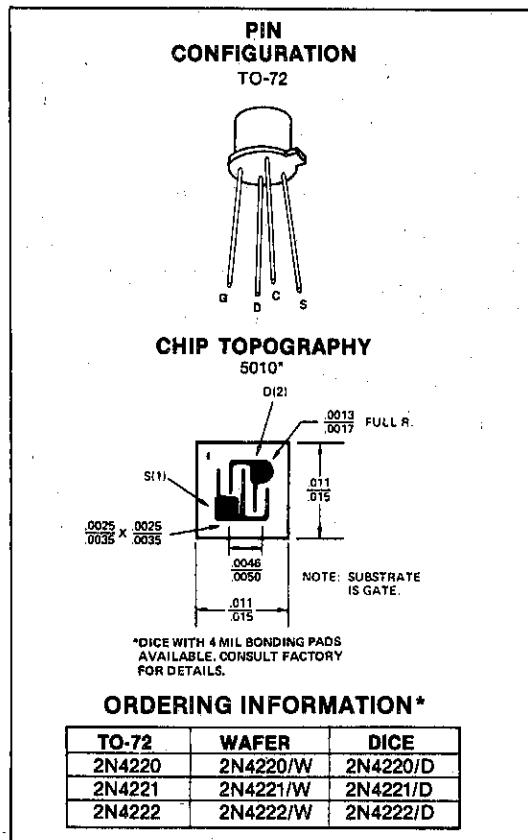
- $C_{rss} < 2 \text{ pF}$
- Moderately High Forward Transconductance

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### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-30V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C



### ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N4220	2N4220/W	2N4220/D
2N4221	2N4221/W	2N4221/D
2N4222	2N4222/W	2N4222/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER	2N4220		2N4221		2N4222		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX <sub>+</sub>		
$I_{GSSR}$	Gate Reverse Current $T_A = 150^\circ\text{C}$	-0.1	-0.1	-0.1	-0.1	-0.1	nA	$V_{GS} = -15 \text{ V}, V_{DS} = 0$
$BV_{GSS}$	Gate-Source Breakdown Voltage	-30	-30	-30	-30	-30	$\mu\text{A}$	$I_G = -10 \mu\text{A}, V_{DS} = 0$
$V_{GSToff}$	Gate-Source Cutoff Voltage	-4	-6	-6	-8	-8	V	$V_{DS} = 15 \text{ V}, I_D = 0.1 \text{ nA}$
$V_{GS}$	Gate-Source Voltage	-0.5	-2.5	-1	-5	-2	-6	V
								$I_D = 50 \mu\text{A}$ (2N4220) $I_D = 200 \mu\text{A}$ (2N4221) $I_D = 500 \mu\text{A}$ (2N4222)
$I_{DSS}$	Saturation Drain Current (Note 3)	0.6	3	2	6	5	15	mA
$g_{fs}$	Common-Source Forward Transconductance (Note 1)	1000	4000	2000	5000	2500	6000	
$ V_{fs} $	Common-Source Forward Transadmittance	750		750		750		$f = 1 \text{ kHz}$
$g_{os}$	Common-Source Output Conductance (Note 1)		10		20		40	$f = 100 \text{ MHz}$
$C_{iss}$	Common-Source Input Capacitance		6		6		6	$f = 1 \text{ kHz}$
$C_{rss}$	Common-Source Reverse Transfer Capacitance		2		2		2	$f = 1 \text{ MHz}$

NOTE 1: Pulse test duration 2 ms.



# 2N4223, 2N4224 N-Channel JFET

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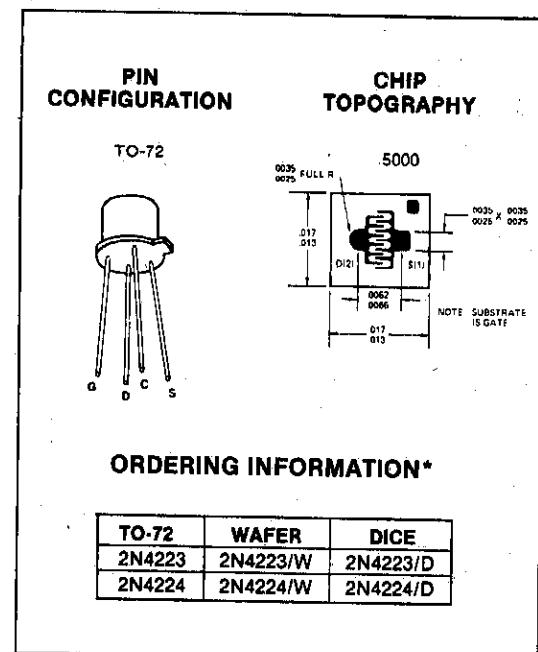
## FEATURES

- $NF = 3$  dB Typical at 200 MHz
- $C_{rss} < 2$  pF

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	.....	-30V
Gate Current	.....	10 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	300 mW
Derate above 25°C	.....	1.7 mW/°C



## ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N4223	2N4223/W	2N4223/D
2N4224	2N4224/W	2N4224/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N4223		2N4224		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX			
$I_{GSSR}$	Gate Reverse Current (TA = +150°C)	-0.25	-0.25	-0.5	nA	$V_{GS} = -20\text{ V}$ , $V_{DS} = 0$	
$BV_{GSS}$	Gate-Source Breakdown Voltage	-30	-30	-30	μA	$I_G = -10\text{ μA}$ , $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.1	-8	-0.1	V	$V_{DS} = 15\text{ V}$	$I_D = 0.25\text{ nA}$ (2N4223) $I_D = 0.5\text{ nA}$ (2N4224)
$V_{GS}$	Gate-Source Voltage	-1.0	-7.0	-1.0			$I_D = 0.3\text{ mA}$ (2N4223) $I_D = 0.2\text{ mA}$ (2N4224)
$ I_{DSS} $	Saturation Drain Current (Note 1)	3	18	2	mA	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0$	
$g_{fs}$	Common-Source Forward Transconductance (Note 1)	3000	7000	2000	μmho		$f = 1\text{ kHz}$
$C_{iss}$	Common-Source Input Capacitance (Output Shorted)		6		pF	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0$	
$C_{rss}$	Common-Source Reverse Transfer Capacitance		2				$f = 1\text{ MHz}$
$ Y_{fs} $	Common-Source Forward Transadmittance	2700		1700	μmho		
$g_{iss}$	Common-Source Input Conductance (Output Shorted)		800			$V_{DS} = 15\text{ V}$ , $V_{GS} = 0$	
$g_{oss}$	Common-Source Output Conductance (Input Shorted)		200				$f = 200\text{ MHz}$
$G_{ps}$	Small Signal Power Gain	10			dB	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0$ , $R_{gen} = 1\text{k}\Omega$	
$NF$	Noise Figure		5				

Note 1: Pulse test, duration 2 msec.



# 2N4338-2N4341 N-Channel JFET

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## FEATURES

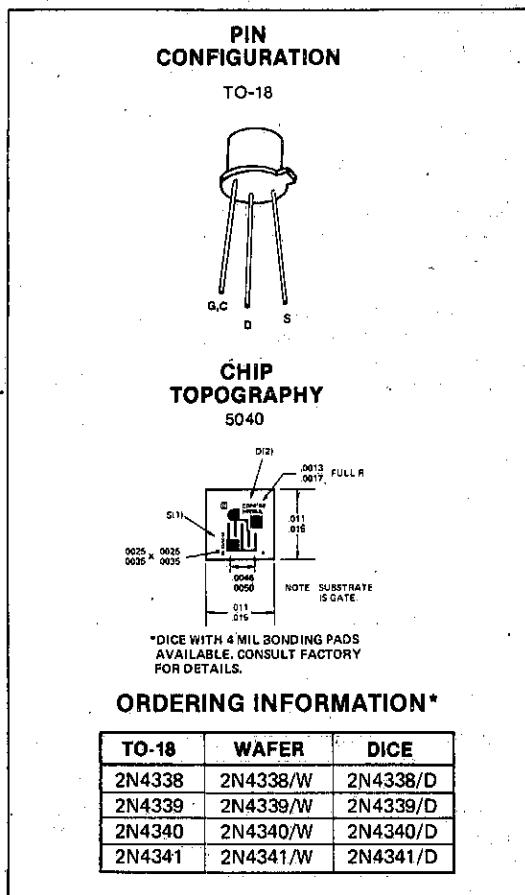
- Exceptionally High Figure of Merit
- Radiation Immunity
- Extremely Low Noise and Capacitance
- High Input Impedance

## APPLICATIONS

- Low-level Choppers
- Data Switches
- Multiplexers and Low Noise Amplifiers

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)	
Gate-Source or Gate-Drain Voltage	-50V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C



\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N4338		2N4339		2N4340		2N4341		UNITS	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
IGSS	Gate Reverse Current [TA=150°C]	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	nA	VGS = -30 V, VDS = 0	
BVGSS	Gate-Source Breakdown Voltage	-50	-50	-50	-50	-50	-50	-50	μA	Ig = -1 μA, VDS = 0	
VGS(off)	Gate-Source Cutoff Voltage	-0.3	-1	-0.6	-1.8	-1	-3	-2	V	VDS = 15 V, ID = 0.1 μA	
ID(off)	Drain Cutoff Current	0.05 (-5)	0.05 (-5)	0.05 (-5)	0.05 (-5)	0.05 (-5)	0.07 (-10)	0.07 (-10)	nA (V)	VDS = 15 V, VGS = (-)	
IDSS	Saturation Drain Current	0.2	0.6	0.5	1.5	1.2	3.6	3	mA	VDS = 15 V, VGS = 0	
gfs	Common-Source Forward Transconductance	600	1800	800	2400	1300	3000	2000	4000	μmho	VDS = 15 V, VGS = 0
gos	Common-Source Output Conductance		5		15		30		60	μmho	f = 1 kHz
rDS(on)	Drain-Source ON Resistance		2500		1700		1500		800	ohm	
Ciss	Common-Source Input Capacitance		7		7		7		7	pF	VDS = 15 V, VGS = 0
Crss	Common-Source Reverse Transfer Capacitance		3		3		3		3	pF	f = 1 MHz
NF	Noise Figure		1		1		1		1	dB	VDS = 15 V, VGS = 0 Rgen = 1 meg, BW = 200 Hz
											f = 1 kHz

# 2N4351

## N-Channel Enhancement Mode MOS FET

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### FEATURES

- Low ON Resistance
- Low Capacitance
- High Gain
- High Gate Breakdown Voltage
- Low Threshold Voltage

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Drain-Source Voltage or Drain-Gate Voltage	25V
Peak Gate-Source Voltage (Note 1)	$\pm 125\text{V}$
Drain Current	100 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	375 mW
Derate above 25°C	3 mW/°C

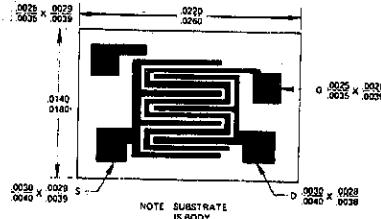
### PIN CONFIGURATION

TO-72



### CHIP TOPOGRAPHY

1003



### ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N4351	2N4351/W	2N4351/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

Substrate connected to source.

PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$BV_{DSS}$	Drain-Source Breakdown Voltage	25	V	$I_D = 10 \mu\text{A}, V_{GS} = 0$
$I_{GSS}$	Gate Leakage Current	10	pA	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0$
$I_{DSS}$	Zero-Gate-Voltage Drain Current	10	nA	$V_{DS} = 10 \text{ V}, V_{GS} = 0$
$V_{GS(th)}$	Gate-Source Threshold Voltage	.1	.5	$V_{DS} = 10 \text{ V}, I_D = 10 \mu\text{A}$
$I_{D(on)}$	"ON" Drain Current	3	mA	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$
$V_{DS(on)}$	Drain-Source "ON" Voltage	1	V	$I_D = 2 \text{ mA}, V_{GS} = 10 \text{ V}$
$r_{DS(on)}$	Drain-Source Resistance	300	ohms	$V_{GS} = 10 \text{ V}, I_D = 0, f = 1 \text{ kHz}$
$ y_{fs} $	Forward Transfer Admittance	1000	$\mu\text{mho}$	$V_{DS} = 10 \text{ V}, I_D = 2 \text{ mA}, f = 1 \text{ kHz}$
$C_{rss}$	Reverse Transfer Capacitance	1.3	pF	$V_{DS} = 0, V_{GS} = 0, f = 140 \text{ kHz}$
$C_{iss}$	Input Capacitance	5.0		$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 140 \text{ kHz}$
$C_{d(sub)}$	Drain-Substrate Capacitance	5.0		$V_{D(SUB)} = 10 \text{ V}, f = 140 \text{ kHz}$
$t_{d(on)}$	Turn-On Delay	45	ns	
$t_r$	Rise Time	65		
$t_{d(off)}$	Turn-Off Delay	60		
$t_f$	Fall Time	100		

Note 1. Device must not be tested at  $\pm 125\text{V}$  more than once or longer than 300 ms.



# ITE4391-ITE4393 2N4391-2N4393 N-Channel JFET

## FEATURES

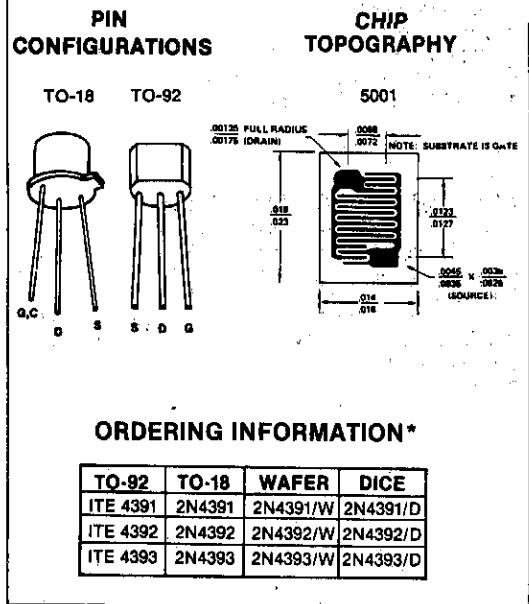
- $r_{ds(on)} < 30 \text{ ohms}$  (2N4391)
- $I_D(\text{off}) < 100 \mu\text{A}$
- Switches  $\pm 10 \text{ VAC}$  with  $\pm 15 \text{V}$  Supplies (2N4392, 2N4393)

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## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ \text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage	.....	-40V
Gate Current	.....	50 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
	TO-18	TO-92
Power Dissipation	..... 1.8W	..... 380 mW
Derate above 25°C	..... 1.7 mW/°C	..... 3.0 mW/°C



## ORDERING INFORMATION\*

TO-92	TO-18	WAFER	DICE
ITE 4391	2N4391	2N4391/W	2N4391/D
ITE 4392	2N4392	2N4392/W	2N4392/D
ITE 4393	2N4393	2N4393/W	2N4393/D

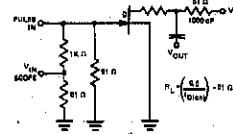
\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ \text{C}$ unless otherwise noted)

PARAMETER		4391		4392		4393		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
$I_{GSS}$	Gate Reverse Current	-100	-100	-100	-100	-100	-100	pA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$	
		$TA = 150^\circ \text{C}$		-200	-200	-200	-200	nA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$	
$BV_{GSS}$	Gate-Source Breakdown Voltage	-40	-40	-40	-40	-40	-40	V	$I_G = 1 \mu\text{A}, V_{DS} = 0$	
$I_D(\text{off})$	Drain Cutoff Current	100	100	100	100	100	100	pA	$V_{GS} = -5 \text{ V} (4393)$	
		$TA = 150^\circ \text{C}$		200	200	200	200	nA	$V_{DS} = 20 \text{ V}$	
$V_{GS(f)}$	Gate-Source Forward Voltage	1	1	1	1	1	1		$V_{GS} = -7 \text{ V} (4392)$	
$V_{GS(\text{off})}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	$V_{DS} = 20 \text{ V}, I_D = 1 \text{nA}$	
$I_{DSS}$	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	
$V_{DS(on)}$	Drain Source ON-Voltage			0.4	0.4		0.4	V	$I_D = 3 \text{ mA} (4393)$	
$r_{DS(on)}$	Static Drain-Source ON Resistance	30	60	60	100	100	100	$\Omega$	$I_D = 6 \text{ mA} (4392)$	
$r_{ds(on)}$	Drain-Source ON Resistance	30	60	60	100	100	100	$\Omega$	$I_D = 12 \text{ mA} (4391)$	
$C_{iss}$	Common-Source Input Capacitance	14	14	14	14	14	14		$V_{GS} = 0, I_D = 1 \text{ mA}$	
$C_{rss}$	Common-Source Reverse Transfer Capacitance					3.5	3.5	pF	$V_{GS} = -5 \text{ V}$	
					3.5				$V_{GS} = -7 \text{ V}$	
$t_d$	Turn-ON Delay Time	15	15	15	15	15	15		$V_{DS} = 20 \text{ V}, V_{GS(\text{on})} = 0$	
$t_r$	Rise Time	5	5	5	5	5	5	ns	$I_D(\text{on}) = 12 \text{ mA}$	
$t_{off}$	Turn-OFF Delay Time	20	35	35	60	60	60		$V_{GS(\text{off})} = -12 \text{ V}$	
$t_f$	Fall Time	15	20	20	30	30	30		4391 12 mA	
									4392 6 mA	
									4393 3 mA	
									-7	
									-5	

### NOTE:

- Pulse test required;  
pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 3\%$



### INPUT PULSE

RISE TIME < 0.5 ns  
FALL TIME < 0.5 ns  
PULSE DUTY CYCLE 1%

### SAMPLING SCOPE

RISE TIME 0.4 ns  
INPUT RESISTANCE 50  $\Omega$



# ITE4416, 2N4416/A N-Channel JFET

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## FEATURES

- Low Noise
- Low Feedback Capacitance
- Low Output Capacitance
- High Transconductance
- High Power Gain

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage

2N4416, ITE4416 ..... -30V

2N4416A ..... -35V

Gate Current ..... 10 mA

Storage Temperature Range

2N4416/2N4416A ..... -65°C to +200°C

ITE4416 ..... -55°C to +125°C

Operating Temperature Range

2N4416/2N4416A ..... -65°C to +200°C

ITE4416 ..... -55°C to +125°C

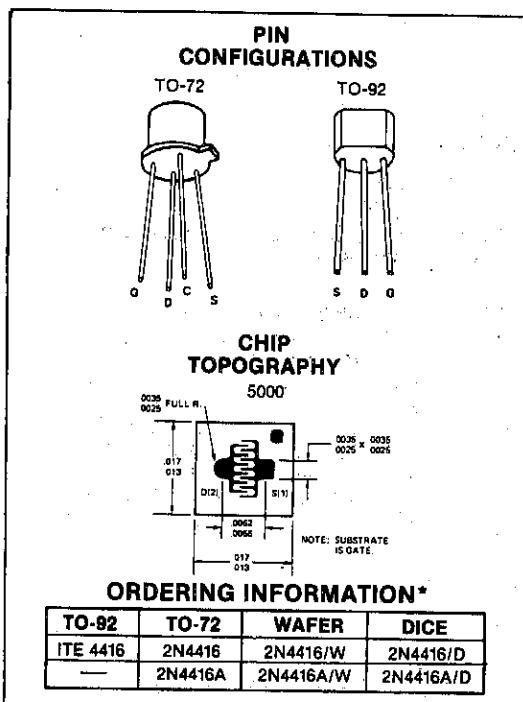
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Power Dissipation ..... 300 mW

Derate above 25°C .....

2N4416/2N4416A ..... 1.7 mW/°C

ITE4416 ..... 3.0 mW/°C



\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS		
V <sub>GS(f)</sub>	Gate-Source Forward Voltage		-1	V	I <sub>G</sub> = 1 mA, V <sub>DS</sub> = 0		
I <sub>GSS</sub>	Gate Reverse Current		-0.1	nA	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0		
		$T_A = 150^\circ\text{C}$		μA			
B/V <sub>GSS</sub>	Gate-Source Breakdown Voltage	2N4416/ITE4416	-30		I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0		
		2N4416A	-35				
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	2N4416/ITE4416	-6	V	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 nA		
		2N4416A	-2.5				
		-6					
I <sub>DSS</sub>	Drain Current at Zero Gate Voltage	5	15	mA	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0	f = 1 kHz	
g <sub>fs</sub>	Common-Source Forward Transconductance	4500	7500	μmho			
g <sub>os</sub>	Common-Source Output Conductance		50	μmho			
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance		0.8	pF			
C <sub>iss</sub>	Common-Source Input Capacitance		4	pF	f = 1 MHz		
C <sub>oss</sub>	Common-Source Output Capacitance		2	pF			
PARAMETER		100 MHz		400 MHz	UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX		
g <sub>iss</sub>	Common-Source Input Conductance		100		1000		
b <sub>iss</sub>	Common-Source Input Susceptance		2500		10,000		
g <sub>oss</sub>	Common-Source Output Conductance		75		100		
b <sub>oss</sub>	Common-Source Output Susceptance		1000		4000		
g <sub>fs</sub>	Common-Source Forward Transconductance			4000			
G <sub>ps</sub>	Common-Source Power Gain	18		10			
NF	Noise Figure		2		4	dB	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 mA
							V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 mA, R <sub>G</sub> = 1 kΩ



# 2N4856-2N4861 2N4856-2N4858 JAN, JTX, JTXY\* N-Channel JFET

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## FEATURES

- Low  $r_{DS(on)}$
- $I_D(\text{off}) < 250 \mu\text{A}$
- Switches  $\pm 10\text{V}$  Signals with  $\pm 15\text{V}$  Supplies (2N4858, 2N4861)

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage

2N4856-58 ..... -40V  
2N4859-61 ..... -30V

Gate Current ..... 50 mA

Storage Temperature ..... -65°C to +200°C

Operating Temperature Range ..... -55°C to +150°C

Led Temperature (Soldering, 10 sec.) ..... +300°C

Power Dissipation ..... 1.8W

Derate above 25°C ..... 10 mW/°C

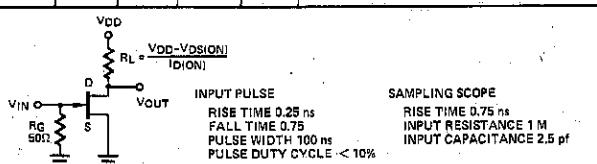
## ELECTRICAL CHARACTERISTICS

(25°C unless otherwise noted)

PARAMETER			2N4856,59		2N4857,60		2N4858,61		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX	V		I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0		
BVGSS	Gate-Source Breakdown Voltage	2N4856-58 2N4859-61	-40 -30		-40 -30		-40 -30	V		I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0	
I <sub>GSSR</sub>	Gate-Reverse Current	TA = 150°C	-250 -500		-250 -500		-250 -500	pA	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0		
I <sub>D(off)</sub>	Drain Cutoff Current	TA = 150°C	-250 500		250 500		250 500	pA	V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0		
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage		-4	-10	-2	-6	-0.8	-4	V	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 0.5 nA	
IDSS	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0	
V <sub>DS(on)</sub>	Drain-Source ON Voltage		0.75 (20)		0.50 (10)		0.50 (5)	V (mA)		V <sub>GS</sub> = 0, I <sub>D</sub> = 1	
R <sub>d(on)</sub>	Drain-Source ON Resistance		25		40		60	ohm	V <sub>GS</sub> = 0, I <sub>D</sub> = 0	f = 1 kHz	
C <sub>iss</sub>	Common-Source Input Capacitance		18		18		18	pF	V <sub>DS</sub> = 0, V <sub>GS</sub> = -10 V	f = 1 MHz	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance		8		8		8				
t <sub>d</sub>	Turn-ON Delay Time		6		6		10	ns			
t <sub>r</sub>	Rise Time			3		4		10			
t <sub>off</sub>	Turn-OFF Time			25		50		100			

### NOTE:

1. Pulse test required, pulsed width = 100 μs, duty cycle ≤ 10%.





# 2N4867/A-2N4869/A N-Channel JFET

## FEATURES

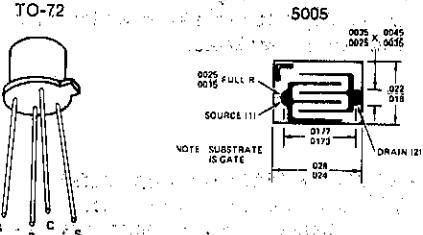
- Low Noise Voltage
- Low Leakage
- High Gain

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

## PIN CONFIGURATION CHIP TOPOGRAPHY



## ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N4867	2N4867/W	2N4867/D
2N4867A	2N4867A/W	2N4867A/D
2N4868	2N4868/W	2N4868/D
2N4868A	2N4868A/W	2N4868A/D
2N4869	2N4869/W	2N4869/D
2N4869A	2N4869A/W	2N4869A/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER		2N4867		2N4868		2N4869		UNIT	TEST CONDITIONS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0
I <sub>GSSR</sub>	Gate Reverse Current <small>T<sub>A</sub> = 150°C</small>	-0.25	-0.25	-0.25	-0.25	-0.25	-0.25	nA	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0	
B <sub>VGSS</sub>	Gate-Source Breakdown Voltage	-40	-40	-40	-40	-40	-40	µA	I <sub>G</sub> = -1 µA, V <sub>DS</sub> = 0	
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-5	V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 µA	
I <sub>DSS</sub>	Saturation Drain Current <small>Note 1)</small>	0.4	1.2	1	3	2.5	7.5	mA	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0	
g <sub>fs</sub>	Common-Source Forward Transconductance (Note 1)	700	2000	1000	3000	1300	4000	µmho	f = 1 kHz	
g <sub>os</sub>	Common-Source Output Conductance			1.5		4		pF		
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance			5		5			V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0	
C <sub>iss</sub>	Common-Source Input Capacitance			25		25		pF	f = 1 MHz	
E <sub>n</sub>	Short Circuit Equivalent Input Noise Voltage <small>A devices</small>			20		20		nV	f = 10 Hz	
				10		10		√Hz	f = 1 kHz	
				10		10			f = 10 Hz	
NF	Spot Noise Figure			5		5		dB	f = 1 kHz	
				1		1			V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 R <sub>gen</sub> = 20 kΩ, (2N4867 Series) R <sub>gen</sub> = 5 kΩ, (2N4867A Series)	

NOTE: 1. Pulse test duration = 2 ms.

# **INTERSIL 2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880 Dielectrically Isolated Dual NPN Transistor**

1

## FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good  $h_{FE}$  Match
- Tight  $V_{BE}$  Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers.

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

### Collector-Base or Collector-Emitter Voltage (Note 1)

2N4044, 2N4878 .....	60V
2N4100, 2N4879 .....	55V
2N4045, 2N4880 .....	45V

### Collector-Collector Voltage .....

100V

### Emitter-Base Voltage (Note 2) .....

7V

### Collector Current (Note 1) .....

10 mA

### Storage Temperature Range .....

-65°C to +200°C

### Operating Temperature Range .....

-55°C to +150°C

### Lead Temperature (Soldering, 10 sec.) .....

+300°C

### TO-71

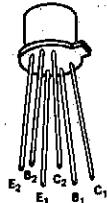
### TO-78

	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power				
Dissipation ..	300 mW	500 mW	400 mW	750 mW

Derate  
above 25°C  
(mW/ $^\circ\text{C}$ ) .... 1.7      2.9      2.3      4.3

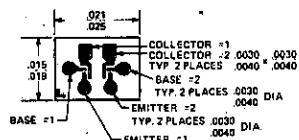
## PIN CONFIGURATION

TO-71  
TO-78



## CHIP TOPOGRAPHY

4000



## ORDERING INFORMATION\*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
$h_{FE}$	DC Current Gain	200	600	150	600	80	800	V	$I_C = 10 \mu\text{A}, V_{CE} = 5\text{V}$
		225		175		100			$I_C = 1.0 \text{mA}, V_{CE} = 5\text{V}$
		$T_A = -55^\circ\text{C}$		75		50			$I_C = 10 \mu\text{A}, V_{CE} = 5\text{V}$
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7	V	$I_C = 1.0 \text{mA}, I_B = 0.1 \text{mA}$
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35		
$I_{CBO}$	Collector Cutoff Current		0.1		0.1		0.1*	nA	$I_E = 0, V_{CB} = 45\text{V}, 30\text{V}^*$
		$T_A = 150^\circ\text{C}$		0.1		0.1		$\mu\text{A}$	
$I_{EBO}$	Emitter Cutoff Current		0.1		0.1		0.1	nA	$I_C = 0, V_{EB} = 5\text{V}$
$C_{obo}$	Output Capacitance		0.8		0.8		0.8	pF	$I_E = 0, V_{CB} = 5\text{V}$

**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

PARAMETER	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
C <sub>te</sub>	Emitter Transition Capacitance		1		1		pF	I <sub>C</sub> = 0, V <sub>EB</sub> = 0.5V
C <sub>CC1, C<sub>2</sub></sub>	Collector to Collector Capacitance		0.8		0.8		pF	V <sub>CC</sub> = 0
I <sub>C1, C<sub>2</sub></sub>	Collector to Collector Leakage Current		5		5		pA	V <sub>CC</sub> = ±100V
V <sub>CEO(sust)</sub>	Collector to Emitter Sustaining Voltage	60		55		45		V I <sub>C</sub> = 1mA, I <sub>B</sub> = 0
f <sub>t</sub>	Current Gain Bandwidth Product	200		150		150		MHz I <sub>C</sub> = 1mA, V <sub>CE</sub> = 10V
f <sub>t</sub>	Current Gain Bandwidth Product	20		15		15		MHz I <sub>C</sub> = 10μA, V <sub>CE</sub> = 10V
NF	Narrow Band Noise Figure		2		3		3	dB I <sub>C</sub> = 10μA, V <sub>CE</sub> = 5V, f = 1kHz R <sub>G</sub> = 10 kohms BW = 200 Hz
BV <sub>CBO</sub>	Collector Base Breakdown Voltage	60		55		45		V I <sub>C</sub> = 10μA, I <sub>E</sub> = 0
BV <sub>EBO</sub>	Emitter Base Breakdown Voltage	7		7		7		V I <sub>E</sub> = 10μA, I <sub>C</sub> = 0

**MATCHING CHARACTERISTICS (25°C unless otherwise noted)**

h <sub>FE1</sub> /h <sub>FE2</sub>	DC Current Gain Ratio (Note 3)	0.9	1	0.85	1	0.8	1		I <sub>C</sub> = 10μA to 1mA, V <sub>CE</sub> = 5V
V <sub>BE1</sub> -V <sub>BE2</sub>	Base Emitter Voltage Differential		3		5		5	mV	I <sub>C</sub> = 10μA, V <sub>CE</sub> = 5V
I <sub>B1</sub> -I <sub>B2</sub>	Base Current Differential		5		10		25	nA	I <sub>C</sub> = 10μA, V <sub>CE</sub> = 5V
Δ(V <sub>BE1</sub> -V <sub>BE2</sub> ) /ΔT	Base Emitter Voltage Differential Change with Temperature		3		5		10	μV/°C	I <sub>C</sub> = 10μA, V <sub>CE</sub> = 5V T <sub>A</sub> = -55°C to +125°C
Δ(I <sub>B1</sub> -I <sub>B2</sub> ) /ΔT	Base Current Differential Change with Temperature		0.3		0.5		1	nA/°C	

**SMALL SIGNAL CHARACTERISTICS**

PARAMETER	TYPICAL VALUE		UNIT	TEST CONDITIONS
h <sub>ib</sub>	Input Resistance	28	ohms	
h <sub>rb</sub>	Voltage Feedback Ratio	43	x 10 <sup>-3</sup>	I <sub>C</sub> = 1mA, V <sub>CB</sub> = 5V
h <sub>fe</sub>	Small Signal Current Gain	250		
h <sub>ob</sub>	Output Conductance	60	μmhos	
h <sub>ie</sub>	Input Resistance	9.6	k ohms	
h <sub>re</sub>	Voltage Feedback Ratio	42	x 10 <sup>-3</sup>	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V
h <sub>oe</sub>	Output Conductance	12	μmhos	

**NOTES:**

- Per transistor.
- The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10 μamps.
- The lowest of two h<sub>FE</sub> readings is taken as h<sub>FE1</sub> for purposes of this ratio.

### FEATURES

- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
- Purely Resistive

1

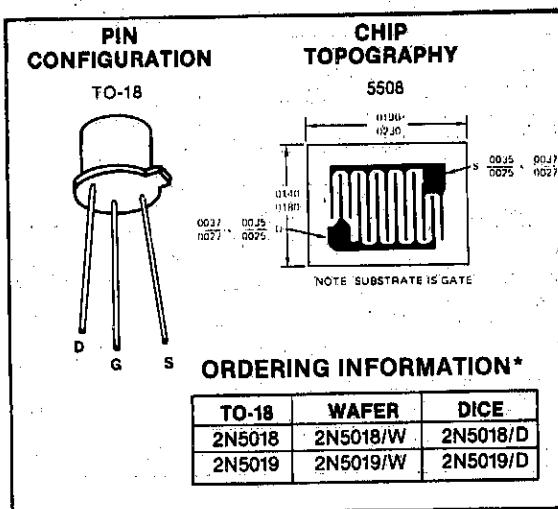
### APPLICATIONS

- Analog Switches
- Commutators
- Choppers

### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage	30V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	500 mW
Derate above 25°C	3 mW/°C

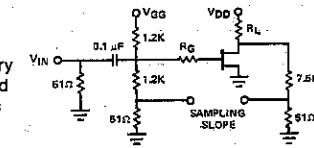


\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER	2N5018		2N5019		Unit	Test Conditions
	Min	Max	Min	Max		
BVGSS	Gate-Source Breakdown Voltage	30	30	30	V	I <sub>G</sub> = 1 $\mu$ A, V <sub>DS</sub> = 0 V <sub>GS</sub> = 15 V, V <sub>DS</sub> = 0
I <sub>GSSR</sub>	Gate Reverse Current	2	2	2	nA	V <sub>GS</sub> = 12 V (2N5018) V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 7 V (2N5019)
I <sub>D(off)</sub>	Drain Cutoff Current	-10	-10	-10	$\mu$ A	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 T <sub>A</sub> = 150°C
I <sub>DGO</sub>	Drain Reverse Current	-2	-2	-2	nA	V <sub>DG</sub> = -15 V, I <sub>S</sub> = 0 T <sub>A</sub> = 150°C
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	10	5	5	V	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -1 $\mu$ A V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0
I <sub>DSS</sub>	Saturation Drain Current	-10	-5	-5	mA	V <sub>GS</sub> = 0, I <sub>D</sub> = -6 mA (2N5018), I <sub>D</sub> = -3 mA (2N5019)
V <sub>DS(on)</sub>	Drain-Source ON Voltage	-0.5	-0.5	-0.5	V	V <sub>DS</sub> = 0, V <sub>GS</sub> = 0
r <sub>DS(on)</sub>	Static Drain-Source ON Resistance	75	150	75	$\Omega$	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0
r <sub>ds(on)</sub>	Drain-Source ON Resistance	75	150	75	$\Omega$	I <sub>D</sub> = 0, V <sub>GS</sub> = 0 f = 1 kHz
C <sub>iss</sub>	Common-Source Input Capacitance	45	45	45	pF	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 f = 1 MHz
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	10	10	10	pF	V <sub>DS</sub> = 0, V <sub>GS</sub> = -12 V (2N5018), V <sub>GS</sub> = -7 V (2N5019)
t <sub>d(on)</sub>	Turn-ON Delay Time	15	15	15	ns	V <sub>DD</sub> = -6 V, V <sub>GS(on)</sub> = 0
t <sub>r</sub>	Rise Time	20	75	75	ns	V <sub>GS(off)</sub> I <sub>D(on)</sub> R <sub>L</sub> 2N5018 12 V -6 mA 9 k $\Omega$ 2N5019 7 V -3 mA 1.8 k $\Omega$
t <sub>d(off)</sub>	Turn-Off Delay Time	15	25	25	ns	
t <sub>f</sub>	Fall Time	50	100	100	ns	

NOTE 1: Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



**INPUT PULSE**  
 RISE TIME < 1 ns  
 FALL TIME < 1 ns  
 PULSE WIDTH 100 ns  
 REPLETION RATE 1 MHz

**SAMPLING SCOPE**  
 RISE TIME 0.4 ns  
 INPUT RESISTANCE 10 M $\Omega$   
 INPUT CAPACITANCE 1.5 pF



# 2N5114-2N5116 JAN, JTX P-Channel JFET

## FEATURES

- Low ON Resistance
- $I_{D(\text{off})} < 500 \mu\text{A}$
- Switches directly from T<sup>2</sup>L Logic

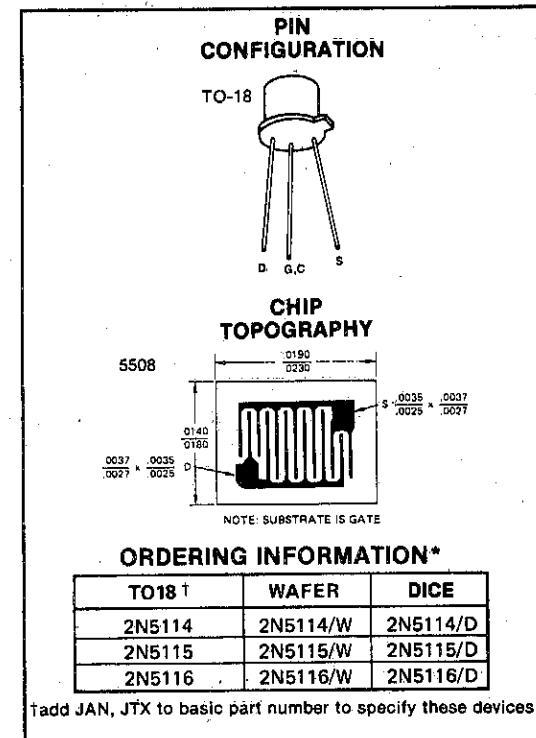
## GENERAL DESCRIPTION

Ideal for inverting switching or "Virtual Gnd" switching into inverting input of Op. Amp. No driver is required and  $\pm 10$  VAC signals can be handled using only +5V logic (T<sup>2</sup>L or CMOS).

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Drain or Gate-Source Voltage .....	30V
Gate Current .....	50 mA
Storage Temperature Range .....	-65°C to +200°C
Operating Temperature Range .....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C
Power Dissipation .....	500 mW
Derate above 25°C .....	3 mW/°C



\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER	2N5114		2N5115		2N5116		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{GSS}$	Gate-Source Breakdown Voltage	30	30	30	30	30	V	$I_G = 1 \mu\text{A}, V_{DS} = 0$
$I_{GSSR}$	Gate Reverse Current $T_A = 150^\circ\text{C}$	500	500	500	500	500	pA	$V_{GS} = 20 \text{ V}, V_{DS} = 0$
$I_{D(\text{off})}$	Drain Cutoff Current $T_A = 150^\circ\text{C}$	1.0	1.0	1.0	1.0	1.0	µA	$V_{DS} = -15 \text{ V}, V_{GS} = 2\text{N}5115 = -7 \text{ V}$ $2\text{N}5116 = -5 \text{ V}$
$V_P$	Gate-Source Pinch-Off Voltage	5	10	3	6	1	4	V
$I_{DS}$	Drain Current at Zero Gate Voltage (Note 1)	-30	-90	-15	-60	-5	-25	mA
$V_{GSSF}$	Forward Gate-Source Voltage		-1		-1		-1	
$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	75	100	100	150	150	Ω	$V_{GS} = 0, ID = -1 \text{ mA}$
$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance Jan TX only	75	100	100	175	175	Ω	$V_{GS} = 0, ID = 0, f = 1 \text{ kHz}$
$C_{iss}$	Common-Source Input Capacitance Jan TX only	25	25	25	27	27	PF	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$
$C_{rss}$	Common-Source Reverse Transfer Capacitance	7	7	7	7	7	PF	$2\text{N}5114 = 12 \text{ V}$ $V_{DS} = 0, V_{GS} = 2\text{N}5115 = 7 \text{ V}$ $2\text{N}5116 = 5 \text{ V}$ $f = 1 \text{ MHz}$

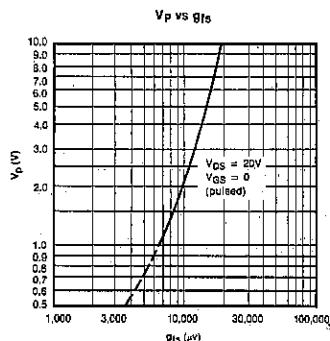
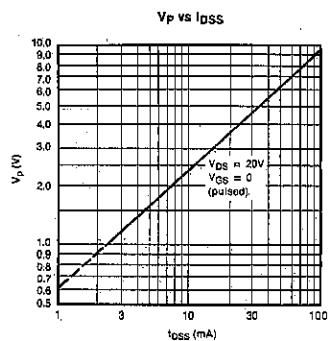
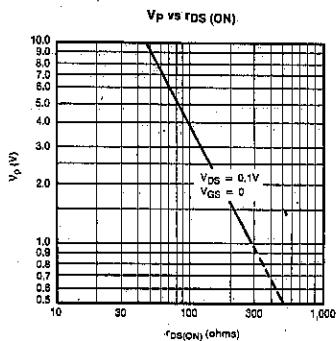
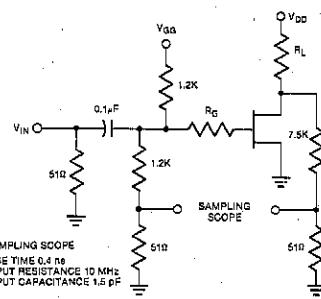
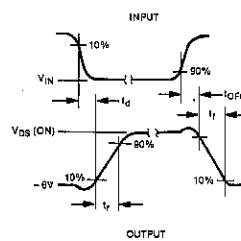
Note 1. Pulse test; duration = 2 ms.

**SWITCHING CHARACTERISTICS** (25°C unless otherwise noted)

PARAMETER	2N5114	2N5115	2N5116	JAN TX 2N5114	JAN TX 2N55115	JAN TX 2N5116	UNIT
$t_d$ Turn-ON Delay Time	6	10	12	6	10	25	ns
$t_r$ Rise Time	10	20	30	10	20	35	
$t_{off}$ Turn-OFF Delay Time	6	8	19	6	8	29	
$t_f$ Fall Time	15	30	50	(not JAN TX specified)			

1

TEST CONDITIONS			
	2N5114	2N5115	2N5116
$V_{DD}$	-10V	-6V	-6V
$V_{GG}$	20V	12V	8V
$R_L$	430Ω	910Ω	2 kΩ
$R_G$	100Ω	220Ω	390Ω
$I_{D(ON)}$	-15mA	-7mA	-3mA
$V_{IN}$	-12V	-7V	-5V




**INTERSIL**

# 2N5117-2N5119

## Dielectrically Isolated Dual PNP Transistor

**1**

### FEATURES

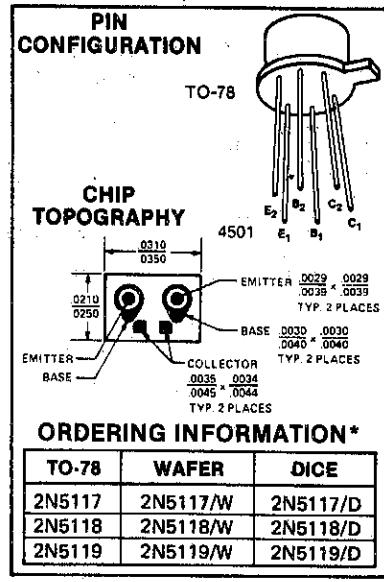
- High Gain at Low Current
- Low Output Capacitance
- Good  $h_{FE}$  Match
- Tight  $V_{BE}$  Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers.

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ C$  unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)	45V
Emitter-Base Voltage (Notes 1 and 2)	7V
Collector-Collector Voltage	100V
Collector Current (Note 1)	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	400 mW	750 mW
Derate above 25°C	2.3 mW/°C	4.3 mW/°C



\*When ordering wafer/dice refer to Appendix B-23

### ELECTRICAL CHARACTERISTICS ( $25^\circ C$ unless otherwise noted)

PARAMETER	2N5117		2N5118		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX			
$h_{FE}$	DC Current Gain	100	300	50		$I_C = 10 \mu A, V_{CE} = 5.0 V$	
		100		50		$I_C = 500 \mu A, V_{CE} = 5.0 V$	
	$T_A = -55^\circ C$	30		20		$I_C = 10 \mu A, V_{CE} = 5.0 V$	
$I_{CBO}$	Collector Cutoff Current	0.1		0.1	nA	$I_E = 0, V_{CB} = 30 V$	
	$T_A = 150^\circ C$	0.1		0.1	$\mu A$		
$I_{EB0}$	Emitter Cutoff Current	0.1		0.1	nA	$I_C = 0, V_{EB} = 5.0 V$	
$I_{C1-C2}$	Collector-Collector Leakage	5.0		5.0	pA	$V_{CC} = 100 V$	
GBW	Current Gain Bandwidth Product	100		100	MHz	$I_C = 500 \mu A, V_{CE} = 10 V$	
$C_{ob}$	Output Capacitance	0.8		0.8	pF	$I_E = 0, V_{CB} = 5.0 V$	
$C_{te}$	Emitter Transition Capacitance	1.0		1.0		$I_C = 0, V_{EB} = 0.5 V$	
$C_{C1-C2}$	Collector-Collector Capacitance	0.8		0.8		$V_{CC} = 0$	
$V_{CEO(sust)}$	Collector-Emitter Sustaining Voltage	45		45	V	$I_C = 1.0 \text{ mA}, I_B = 0$	
NF	Narrow Band Noise Figure		4.0		4.0	dB	$I_C = 10 \mu A, V_{CE} = 5.0 V$ f = 1 KHz, $R_G = 10 \text{ k}\Omega$ BW = 200 Hz
$BV_{CBO}$	Collector Base Breakdown Voltage	45		45	V	$I_C = 10 \mu A, I_E = 0$	
$BV_{EBO}$	Emitter Base Breakdown Voltage	7.0		7.0	V	$I_E = 10 \mu A, I_C = 0$	

### MATCHING CHARACTERISTICS ( $25^\circ C$ unless otherwise noted)

PARAMETER	2N5117		2N5118		2N5119		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX			
$h_{FE1}/h_{FE2}$	DC Current Gain Ratio (Note 3)	0.9	1.0					$I_C = 10 \mu A$ to $500 \mu A, V_{CE} = 5 V$	
				0.85	1.0	0.8		$I_C = 10 \mu A, V_{CE} = 5.0 V$	
$V_{BE1}-V_{BE2}$	Base-Emitter Voltage Differential		3.0				mV	$I_C = 10 \mu A$ to $500 \mu A, V_{CE} = 5 V$	
					5.0	5.0			
$I_{B1}-I_{B2}$	Base Current Differential		10.0		15		nA		
						40			
$\Delta(V_{BE1}-V_{BE2})/\Delta T$	Base Voltage Differential Change with Temperature		3.0		5.0		$\mu V/^\circ C$	$I_C = 10 \mu A, V_{CE} = 5.0 V$	$T_A = -55^\circ C$ to $+125^\circ C$
						10			
$\Delta(I_{B1}-I_{B2})/\Delta T$	Base-Current Differential Change with Temperature		0.3		0.5		nA/°C		$T_A = -55^\circ C$ to $+125^\circ C$
						1.0			

1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10  $\mu A$ .

3. Lower of two  $h_{FE}$  readings is defined as  $h_{FE1}$ .



# 2N5196-2N5199

## Dual Monolithic N-Channel JFET

### ABSOLUTE MAXIMUM RATINGS

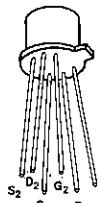
(TA = 25°C unless otherwise noted)

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Gate-Source or Gate-Drain Voltage (Note 1) .....	-50V
Gate Current (Note 1) .....	50 mA
Storage Temperature Range .....	-65°C to +200°C
Operating Temperature Range .....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C
Power Dissipation .....	250 mW ... 500 mW
Derate above 25°C .....	2.6 mW/°C .. 4.3 mW/°C

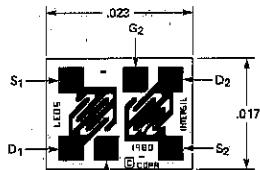
### PIN CONFIGURATION

TO-18



### CHIP TOPOGRAPHY

6037



ALL BOND PADS ARE 4x 4 MIL.

### ORDERING INFORMATION\*

TO-71	WAFER	DICE
2N5196	2N5196/W	2N5196/D
2N5197	2N5197/W	2N5197/D
2N5198	2N5198/W	2N5198/D
2N5199	2N5199/W	2N5199/D

\*When ordering wafers/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER				MIN	MAX	UNIT	TEST CONDITIONS			
					TA = 150°C			VGS = -30 V, VDS = 0		
BVGSS	Gate-Source Breakdown Voltage			-50				IG = -1 μA, VDS = 0		
VGS(off)	Gate-Source Cutoff Voltage			-0.7	-4	V		VDS = 20 V, ID = 1 nA		
VGS	Gate-Source Voltage			-0.2	-3.8			VDG = 20 V, ID = 200 μA		
IG	Gate Operating Current			-15	-15	pA		VDS = 20 V, VGS = 0		
IDSS	Saturation Drain Current (Note 2)			0.7	7	mA		VDS = 20 V, VGS = 0		
gfs	Common-Source Forward Transconductance	1000	4000					VDS = 20 V, VGS = 0		
gfs	Common-Source Forward Transconductance	700	1600					VDG = 20 V, ID = 200 μA		
gos	Common-Source Output Conductance			50		μmho		VDS = 20 V, VGS = 0		
gos	Common-Source Output Conductance			4				VDG = 20 V, ID = 200 μA		
Ciss	Common-Source Input Capacitance			6		pF		f = 1 MHz		
Crss	Common-Source Reverse Transfer Capacitance			2				f = 100 Hz, RC = 10 MΩ		
NF	Spot Noise Figure			0.5		dB		f = 1 kHz		
ε <sub>i</sub>	Equivalent Input Noise Voltage			20		μV / √Hz				

PARAMETER	2N5196		2N5197		2N5198		2N5199		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
IG1-IG2	Differential Gate Current		5		5		5		nA	VDG = 20 V, ID = 200 μA	125°C
IDSS1 / IDSS2	Saturation Drain Current Ratio (Note 2)	0.95	1	0.95	1	0.95	1	0.95		VDS = 20 V, VGS = 0 V	
gfs1 / gfs2	Transconductance Ratio (Note 2)	0.97	1	0.97	1	0.95	1	0.95			f = 1 kHz
IVGS1-VGS2	Differential Gate-Source Voltage		5		5		10		mV		
Δ VGS1-VGS2  / ΔT	Gate-Source Differential Voltage Change with Temperature (Note 3)		5		10		20		μV/°C		
Igos1-Igos2	Differential Output Conductance	1		1		1		1	μmho		

NOTES: 1. Per transistor.

2. Pulse test required, pulsed width = 300 μs, duty cycle < 3%.

3. Measured at endpoints TA and TB.



# 2N5397, 2N5398 N-Channel JFET

## FEATURES

- $G_{ps} = 15$  dB Minimum (Common Gate) at 450 MHz
- Low Noise
- Low Capacitance

1

## ABSOLUTE MAXIMUM RATINGS

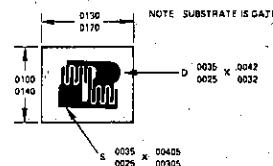
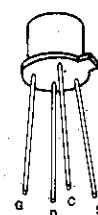
( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Drain-Gate Voltage	.....	-25V
Drain-Source Voltage	.....	-25V
Continuous Forward Gate Current	.....	-10 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	300 mW
Derate above 25°C	.....	1.7 mW/°C

## PIN CONFIGURATION      CHIP TOPOGRAPHY

TO-72

5011



## ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N5397	2N5397/W	2N5397/D
2N5398	2N5398/W	2N5398/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER	2N5397		2N5398		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX			
$I_{GSSR}$	Gate Reverse Current	$T_A = +150^\circ\text{C}$	-0.1	-0.1	nA	$V_{GS} = -15\text{ V}, V_{DS} = 0$	
$BV_{GSS}$	Gate-Source Breakdown Voltage	-25	-25		μA	$V_{DS} = 0, I_G = 1\text{-}\mu\text{A}$	
$V_{GS(\text{off})}$	Gate-Source Cutoff Voltage	-1.0	-6.0	-1.0		$V_{DS} = 10\text{ V}, I_D = 1\text{nA}$	
$I_{DSS}$	Saturation Drain Current (Note 1)	10	30	5	mA	$V_{DS} = 10\text{ V}, V_{GS} = 0$	
$V_{GS(f)}$	Gate-Source Forward Voltage		1	1	V	$V_{DS} = 0, I_G = 1\text{mA}$	
$g_{fs}$	Common-Source Forward Transconductance (Note 1)	6000	10,000	5500	10,000	μmho	$V_{DS} = 10\text{ V}, I_D = 10\text{ mA}$
$g_{oss}$	Common-Source Output Conductance		200		400		$V_{DS} = 10\text{ V}, V_{GS} = 0$
$C_{rss}$	Common-Source Reverse Transfer Capacitance			1.2		pF	$V_{DS} = 10\text{ V}, I_D = 10\text{ mA}$
$C_{iss}$	Common-Source Input Capacitance			5.0	5.5		$V_{DG} = 10\text{ V}, V_{GS} = 0$
$g_{iss}$	Common-Source Input Conductance			2000			$V_{DG} = 10\text{ V}, I_D = 10\text{ mA}$
$g_{oss}$	Common-Source Output Conductance				3000	μmho	$V_{DG} = 10\text{ V}, V_{GS} = 0$
$g_{fs}$	Common-Source Forward Transconductance (Note 1)	5500	9000	400	500		$V_{DG} = 10\text{ V}, I_D = 10\text{ mA}$
$G_{ps}$	Common-Source Power Gain (neutralized)	15				dB	$V_{DG} = 10\text{ V}, V_{GS} = 0$
NF	Common-Source, Spot Noise Figure (neutralized)			3.5			$V_{DG} = 10\text{ V}, I_D = 10\text{ mA}$

Note 1: Pulse test duration = 2ms



# 2N5432-2N5434

## N-Channel JFET

### FEATURES

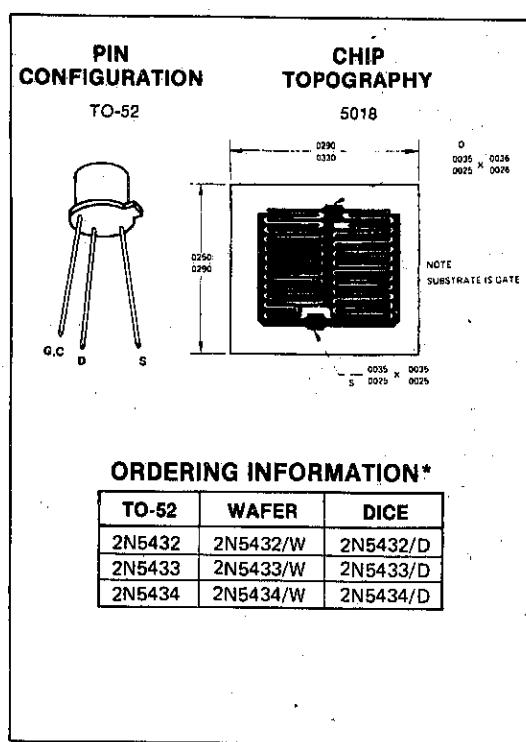
- Low  $r_{ds(on)}$
- Excellent Switching
- Low Cutoff Current

1

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source Voltage .....	-25V
Gate-Drain Voltage .....	-25V
Gate Current .....	100mA
Drain Current .....	400 mA
Storage Temperature Range .....	-65°C to +200°C
Operating Temperature Range .....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C
Power Dissipation .....	300 mW
Derate above 25°C .....	2.3 mW/°C

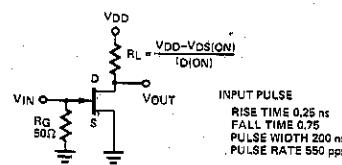


\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER		2N5432		2N5433		2N5434		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
$I_{GSSR}$	Gate Reverse Current $T_A = 150^\circ\text{C}$	-200	-200	-200	-200	-200	-200	pA	$V_{GS} = -15\text{ V}$ , $V_{DS} = 0$	
$BV_{GSS}$	Gate Source Breakdown Voltage	-25	-25	-25	-25	-25	-25	V	$I_G = -1\text{ }\mu\text{A}$ , $V_{DS} = 0$	
$I_{D(off)}$	Drain Cutoff Current $T_A = 150^\circ\text{C}$	200	200	200	200	200	200	pA	$V_{DS} = 5\text{ V}$ , $V_{GS} = -10\text{ V}$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	$V_{DS} = 5\text{ V}$ , $I_D = 3\text{ nA}$	
$I_{DS}$	Saturation Drain Current (Note 1)	150		100		30		mA	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0$	
$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5	7	10			ohm		
	Drain-Source ON Voltage		50	70	100			mV	$V_{GS} = 0$ , $I_D = 10\text{ mA}$	
$r_{ds(on)}$	Drain-Source ON Resistance		5	7	10			ohm	$V_{GS} = 0$ , $I_D = 0$	
$C_{iss}$	Common-Source Input Capacitance	30		30		30			$f = 1\text{ kHz}$	
$C_{rss}$	Common-Source Reverse Transfer Capacitance		15		15		15	pF	$V_{DS} = 0$ , $V_{GS} = -10\text{ V}$	
$t_d$	Turn-ON Delay Time		4		4		4			
$t_r$	Rise Time		1		1		1	ns		
$t_{off}$	Turn-OFF Delay Time		6		6		6			
$t_f$	Fall Time		30		30		30			

NOTE: 1. Pulse test required, pulsed width 300  $\mu\text{s}$ , duty cycle  $\leq 3\%$ .



INPUT PULSE  
RISE TIME 0.25 ns  
FALL TIME 0.75 ns  
PULSE WIDTH 200 ns  
PULSE RATE 550 ppm

#### SAMPLING SCOPE

145Ω (2N5432)  
 $R_L = 143\Omega$  (2N5433)  
 $R_L = 140\Omega$  (2N5434)

# 2N5452-2N5454

## Dual Monolithic N-Channel JFET

### FEATURES

- Low Offset Voltage
- Low Drift
- Low Capacitance
- Low Output Conductance

### GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

### ABSOLUTE MAXIMUM RATINGS

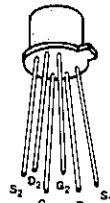
( $T_A = 25^\circ\text{C}$  unless otherwise noted)

#### Gate-Source or Gate Drain

	ONE SIDE	BOTH SIDES
Voltage (Note 1)	.....	-50V
Gate Current (Note 1)	.....	50 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	250 mW	500 mW
Derate above 25°C	2.9 mW/°C	4.3 mW/°C

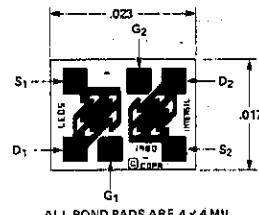
### PIN CONFIGURATION

TO-71



### CHIP TOPOGRAPHY

6037



### ORDERING INFORMATION\*

TO-71	WAFER	DICE
2N5452	2N5452/W	2N5452/D
2N5453	2N5453/W	2N5453/D
2N5454	2N5454/W	2N5454/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	2N5452	2N5453	2N5454	UNITS	TEST CONDITIONS	
	MIN	MAX	MIN	MAX		
$I_{GSSR}$	Gate Reverse Current, $T_A = 150^\circ\text{C}$	-100 -200	-100 -200	-100 -200	pA	$V_{GS} = -30\text{ V}$ , $V_{DS} = 0$
$BV_{GSS}$	Gate-Source Breakdown Voltage	-50	-50	-50	V	$V_{DS} = 0$ , $I_G = 1\text{ }\mu\text{A}$
$V_{GS(\text{off})}$	Gate-Source Cutoff Voltage	-1	-4.5	-1		$V_{DS} = 20\text{ V}$ , $I_D = 1\text{ nA}$
$V_{GS}$	Gate-Source Voltage	-0.2	-4.2	-0.2		$V_{DS} = 20\text{ V}$ , $I_D = 50\text{ }\mu\text{A}$
$V_{GS(\text{f})}$	Gate-Source Forward Voltage	2	2	2		$V_{DS} = 0$ , $I_G = 1\text{ mA}$
$IDSS$	Saturation Drain Current	0.5	5.0	0.5	mA	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$
$g_{fs}$	Common-Source Forward Transconductance	1000 1000	3000 1000	1000 1000	$\mu\text{mho}$	$f = 1\text{ kHz}$ $f = 100\text{ MHz}$ $f = 1\text{ kHz}$
$g_{os}$	Common-Source Output Conductance	3.0 1.0	3.0 1.0	3.0 1.0	$\mu\text{mho}$	$V_{DS} = 20\text{ V}$ , $I_D = 200\text{ }\mu\text{A}$
$C_{iss}$	Common-Source Input Capacitance	4.0	4.0	4.0	pF	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$
$C_{rss}$	Common-Source Reverse Transfer Capacitance	1.2	1.2	1.2	pF	$f = 1\text{ MHz}$
$C_{dg0}$	Drain-Gate Capacitance	1.5	1.5	1.5		$V_{DG} = 10\text{ V}$ , $I_S = 0$
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage	.20	.20	.20	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$
NF	Common-Source Spot Noise Figure	0.5	0.5	0.5	.dB	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$ $R_G = 10\text{ M}\Omega$
$ IDSS1 / DSS2 $	Drain Saturation Current Ratio	0.95	1.0	0.95		$f = 100\text{ Hz}$
$ V_{GS1}-V_{GS2} $	Differential Gate-Source Voltage	5.0	10.0	15.0	mV	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$
$\Delta V_{GS1}-V_{GS2} $	Gate-Source Voltage Differential Change with Temperature	0.4 0.5	0.8 1.0	2.0 2.5		$T = 25^\circ\text{C}$ to $+55^\circ\text{C}$ $T = 25^\circ\text{C}$ to $+125^\circ\text{C}$
$g_{fs1}/g_{fs2}$	Transconductance Ratio	0.97	1.0	0.97		
$ g_{os1}-g_{os2} $	Differential Output Conductance	0.25	0.25	0.25	$\mu\text{mhos}$	$f = 1\text{ kHz}$

NOTE: 1. Per transistor.



# 2N5457-2N5459 N-Channel JFET

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Drain-Gate Voltage	25V
Drain-Source Voltage	25V
Continuous Forward Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

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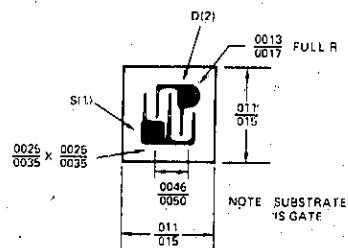
## PIN CONFIGURATION

TO-92



## CHIP TOPOGRAPHY

5010\*



\*DICE WITH 4 MIL BONDING PADS  
AVAILABLE. CONSULT FACTORY  
FOR DETAILS.

## ORDERING INFORMATION\*

TO-92	WAFER	DICE
2N5457	2N5457/W	2N5457/D
2N5458	2N5458/W	2N5458/D
2N5459	2N5459/W	2N5459/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
BVGSS	Gate-Source Breakdown Voltage	-25	-60		V	IG = -10 μA, VDS = 0
IGSS	Gate Reverse Current		.05	-1.0	nA	VGS = -15 V, VDS = 0
				-200		VGS = -15 V, VDS = 0, TA = 100°C
VGS(off)	Gate-Source Cutoff Voltage	2N5457	-0.5	-6.0	V	VDS = 15 V, ID = 10 nA
	2N5458	-1.0	-7.0			
	2N5459	-2.0	-8.0			
VGS	Gate-Source Voltage	2N5457	2.5		V	VDS = 15 V, ID = 100 μA
	2N5458	3.5				VDS = 15 V, ID = 200 μA
	2N5459	4.5				VDS = 15 V, ID = 400 μA
IDSS	Zero-Gate-Voltage Drain Current	2N5457	1.0	3.0	mA	VDS = 15 V, VGS = 0
	2N5458	2.0	6.0	9.0		
	2N5459	4.0	9.0	16		
IVFSL	Forward Transfer Admittance	2N5457	1000	3000	5000	μmho
	2N5458	1500	4000	5500		VDS = 15 V, VGS = 0, f = 1 kHz
	2N5459	2000	4500	6000		
IVOSL	Output Admittance		10	50	μmho	VDS = 15 V, VGS = 0, f = 1 kHz
Ciss	Input Capacitance		4.5	7.0	pF	VDS = 15 V, VGS = 0, f = 1 MHz
Crss	Reverse Transfer Capacitance		1.5	3.0	pF	VDS = 15 V, VGS = 0, f = 1 MHz
NF	Noise Figure			3.0	dB	VDS = 15 V, VGS = 0, RG = 1 MHz BW = 1 Hz, f = 1 kHz

Pulse test required. PW ≤ 630 ms, duty cycle ≤ 10%



# 2N5460-2N5465

## P-Channel JFET

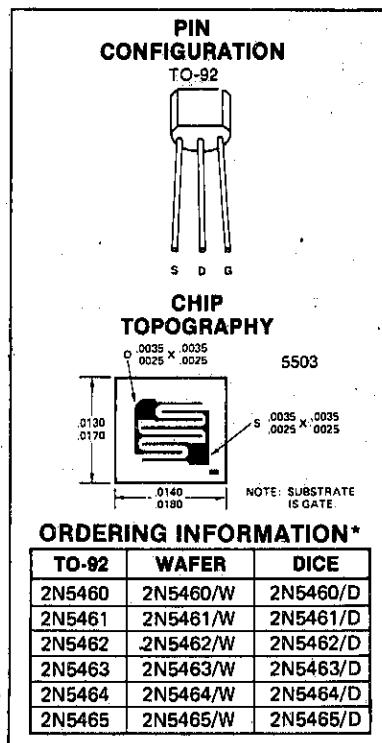
1

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

#### Drain-Gate or Source-Gate Voltage

2N5460 - 2N5462	.....	40V
2N5463 - 2N5465	.....	60V
Gate Current	.....	10 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	310 mW
Derate above 25°C	.....	2.8 mW/°C



### ORDERING INFORMATION\*

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

\*When ordering wafer/dice refer to Appendix B-23.

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS			
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	2N5460, 2N5461, 2N5462	40		V	$I_G = 10 \mu\text{A dc}, V_{DS} = 0$	$V_{DS} = 15 \text{ Vdc}, I_D = 1.0 \mu\text{A dc}$	$V_{DS} = 0$	$V_{GS} = 20\text{V}$
		2N5463, 2N5464, 2N5465	60						
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	2N5460, 2N5463	0.75	8.0	V	$V_{DS} = 15 \text{ Vdc}, I_D = 1.0 \mu\text{A dc}$	$V_{GS} = 30\text{V}$	$V_{GS} = 20\text{V}$	$V_{GS} = 30\text{V}$
		2N5461, 2N5464	1.0	7.6					
		2N5462, 2N5465	1.8	9.0					
I <sub>GSSR</sub>	Gate Reverse Current	2N5460, 2N5461, 2N5462		5.0	mA	$I_G = 10 \mu\text{A dc}, V_{GS} = 0$	$V_{GS} = 20\text{V}$	$V_{GS} = 30\text{V}$	$V_{GS} = 20\text{V}$
		2N5463, 2N5464, 2N5465		5.0					
		2N5460, 2N5461, 2N5462		1.0					
	$T_A = 100^\circ\text{C}$	2N5463, 2N5464, 2N5465		1.0					
I <sub>DSS</sub>	Zero-Gate Voltage Drain Current	2N5460, 2N5463	-1.0	-5.0	mA	$V_{DS} = -15\text{V}$	$V_{GS} = 0$	$I_D = 0.1 \text{ mA}$	$I_D = -0.2 \text{ mA}$
		2N5461, 2N5464	-2.0	-9.0					
		2N5462, 2N5465	-4.0	-16					
V <sub>GS</sub>	Gate-Source Voltage	2N5460, 2N5463	0.5	4.0	V	$V_{DS} = -15\text{V}$	$I_D = -0.4 \text{ mA}$	$I_D = -0.1 \text{ mA}$	$I_D = -0.2 \text{ mA}$
		2N5461, 2N5464	0.8	4.5					
		2N5462, 2N5465	1.5	6.0					
g <sub>fs</sub>	Forward Transadmittance	2N5460, 2N5463	1000	4000	$\mu\text{mho}$	$V_{DS} = -15\text{V}$	$V_{GS} = 0\text{V}$	$f = 1.0 \text{ kHz}$	$f = 1.0 \text{ kHz}$
		2N5461, 2N5464	1500	5000					
		2N5462, 2N5465	2000	6000					
g <sub>os</sub>	Output Admittance			75	$\mu\text{mho}$	$f = 100 \text{ Hz}$	$BW = 1.0 \text{ Hz}$	$R_G = 1.0 \text{ M}\Omega$	$f = 100 \text{ Hz}$
	Input Capacitance		5.0	7	$\text{pF}$				
C <sub>rss</sub>	Reverse Transfer Capacitance		1.0	2.0	$\text{pF}$	$f = 100 \text{ Hz}$	$BW = 1.0 \text{ Hz}$	$R_G = 1.0 \text{ M}\Omega$	$f = 100 \text{ Hz}$
	Common-Source Noise Figure		1.0	2.5	$\text{dB}$				
e <sub>n</sub>	Equivalent Short-Circuit Input Noise Voltage		60	115	$\text{nV}/\sqrt{\text{Hz}}$	$f = 100 \text{ Hz}$	$BW = 1.0 \text{ Hz}$	$R_G = 1.0 \text{ M}\Omega$	$f = 100 \text{ Hz}$



# 2N5484-2N5486 N-Channel JFET

## FEATURES

- Up to 400 MHz Operation
- Economy Packaging
- $C_{rss} < 1.0 \text{ pF}$

1

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise specified)

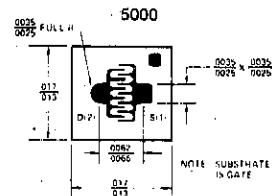
Drain-Gate Voltage	.....	25V
Source Gate Voltage	.....	25V
Drain Current	.....	30 mA
Forward Gate Current	.....	10 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	310 mW
Derate above 25°C	.....	2.8 mW/°C

## PIN CONFIGURATION

TO-92



## CHIP TOPOGRAPHY



## ORDERING INFORMATION\*

TO-92	WAFER	DICE
2N5484	2N5484/W	2N5484/D
2N5485	2N5485/W	2N5485/D
2N5486	2N5486/W	2N5486/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER	2N5484		2N5485		2N5486		UNITS	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX			
$I_{GSSR}$	Gate Reverse Current, $T_A = 100^\circ\text{C}$	-1.0 -200 <sup>a</sup>	-1.0 -200	-1.0 -200	-1.0 -200	-1.0 -200	nA	$V_{GS} = -20 \text{ V}$ , $V_{DS} = 0$	
$BV_{GSS}$	Gate-Source Breakdown Voltage	-25	-25	-25	-25	-25	V	$I_G = -1 \mu\text{A}$ , $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-3.0	-0.5	-4.0	-2.0	-6.0	$V_{DS} = 15 \text{ V}$ , $I_D = 10 \text{ nA}$	
$ I_{DSS} $	Saturation Drain Current	1.0	5.0	4.0	10 <sup>b</sup>	8.0	20	$V_{DS} = 15 \text{ V}$ , $V_{GS} = 0$ (Note 1)	
$g_{fs}$	Common-Source Forward Transconductance	3000	6000	3500	7000	4000	8000	$V_{DS} = 15 \text{ V}$ , $V_{GS} = 0$	f = 1 kHz
$g_{os}$	Common-Source Output Conductance		50		60		75		f = 100 MHz
$R_{(v_{fs})}$	Common-Source Forward Transconductance	2800			3000	3500			f = 400 MHz
$R_{(v_{os})}$	Common-Source Output Conductance		75			100			f = 100 MHz
$R_{(v_{is})}$	Common-Source Input Conductance		100			1000	1000		f = 400 MHz
$C_{iss}$	Common-Source Input Capacitance	5.0		5.0		5.0			f = 100 MHz
$C_{rss}$	Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0	$R_G = 1 \text{ M}\Omega$	f = 1 MHz
$C_{oss}$	Common-Source Output Capacitance		2.0		2.0		2.0		$V_{DS} = 15 \text{ V}$ , $V_{GS} = 0$ , $R_G = 1 \text{ M}\Omega$
$NF$	Noise Figure	2.5		2.5		2.5			$f = 100 \text{ MHz}$
		3.0		2.0		2.0			$f = 400 \text{ MHz}$
$G_{ps}$	Common-Source Power Gain		4.0		4.0		$V_{DS} = 15 \text{ V}$ , $I_D = 4 \text{ mA}$	$f = 100 \text{ MHz}$	
		16	25	18	30	18	30	$f = 400 \text{ MHz}$	
				10	20	10	20		

NOTE: Pulse test required. Pulse width = 300 $\mu\text{s}$ , duty cycle  $\leq 3\%$ .



# 2N5515-2N5524

## Monolithic Dual N-Channel JFET

1

### FEATURES

- Tight Temperature Tracking
- Tight Matching
- High Common Mode Rejection
- Low Noise

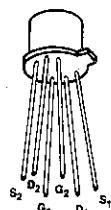
### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise specified)

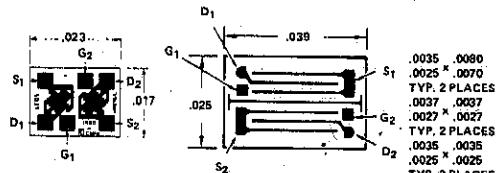
Gate-Source or Gate-Drain Voltage .....	-40V
Gate Current (Note 1) .....	50 mA
Storage Temperature Range .....	-65°C to +200°C
Operating Temperature Range .....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C
ONE SIDE      BOTH SIDES	
Power Dissipation .....	250 mW ... 500 mW
Derate above 25°C ....	3.8 mW/°C ... 7.7 mW/°C

### PIN CONFIGURATION

TO-71



### CHIP TOPOGRAPHY

(2N5515-19)  
6037(2N5520-24)  
6019

ALL BOND PADS ARE 4 x 4 MIL.

### ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N5515	2N5515/W	2N5515/D
2N5516	2N5516/W	2N5516/D
2N5517	2N5517/W	2N5517/D
2N5518	2N5518/W	2N5518/D
2N5519	2N5519/W	2N5519/D
2N5520		
2N5521		
2N5522		
2N5523		
2N5524		

\*When ordering wafer/dice refer to Appendix B-23.

NOTE: Per transistor.

# 2N5515 thru 2N5524

 **INTERSIL**

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I <sub>GSSR</sub>	Gate Reverse Current <small>T<sub>A</sub> = 150°C</small>	-250	-250	pA	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0	
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-40			I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0	
V <sub>P</sub>	Gate-Source Pinch-Off Voltage	-0.7	-4	V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA	
I <sub>DSS</sub>	Drain Current at Zero Gate Voltage (Note 1)	0.5	7.5	mA		
g <sub>fs</sub>	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho		f = 1 kHz
g <sub>oss</sub>	Common-Source Output Conductance		10		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance		5	pF		f = 1 MHz
C <sub>iss</sub>	Common-Source Input Capacitance		25			
		2N5515-19	30			f = 10 Hz
		2N5520-24	15	nV/√Hz		f = 1 kHz
		2N5515-24	10			
I <sub>G</sub>	Gate Current <small>T<sub>A</sub> = 125°C</small>	-100	-100	pA	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA	
V <sub>GS</sub>	Gate Source Voltage	-0.2	-3.8	V		
g <sub>fs</sub>	Common-Source Forward Transconductance (Note 1)	500	1000	μmho		f = 1 kHz
g <sub>oss</sub>	Common-Source Output Conductance		1	μmho		

## MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I <sub>DSS1</sub>	Drain Current Ratio at	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0
I <sub>DSS2</sub>	Zero Gate Voltage (Note 1)											
I <sub>G1</sub> - I <sub>G2</sub>	Differential Gate Current (+125°C)	10		10		10		10		10	nA	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA
g <sub>f1</sub>	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA f = 1 kHz
g <sub>f2</sub>	(Note 1)											
B <sub>oss1</sub> - B <sub>oss2</sub>	Differential Output Conductance		0.1		0.1		0.1		0.1	0.1	μmho	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA f = 1 kHz
V <sub>GS1</sub> - V <sub>GS2</sub>	Differential Gate-Source Voltage		5		5		10		15	15	mV	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA
Δ V <sub>GS1</sub> - V <sub>GS2</sub>   ΔT	Gate-Source Voltage Differential Drift (T <sub>A</sub> = -55°C to +125°C)		5		10		20		40	80	μV/°C	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA
CMRR	Common-Mode Rejection Ratio (Note 2)	-100		100		90					dB	V <sub>DD</sub> = 10 to 20 V, I <sub>D</sub> = 200 μA

### NOTES:

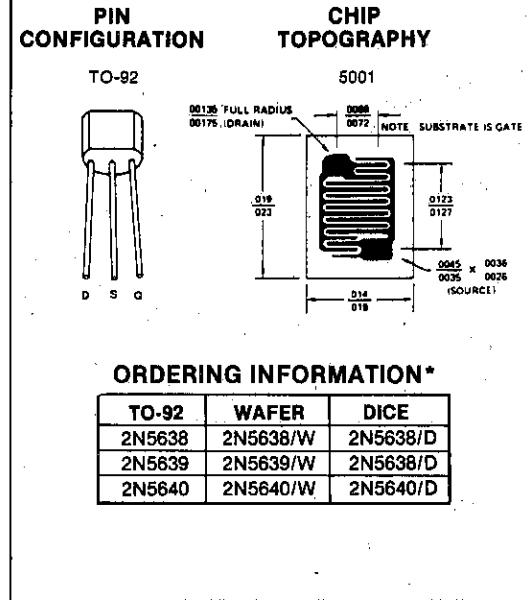
1. Pulse duration of 28 ms used during test.
2. CMRR = 20 Log<sub>10</sub>ΔV<sub>DD</sub>/Δ|V<sub>GS1</sub> - V<sub>GS2</sub>|, (ΔV<sub>DD</sub> = 10V)

**FEATURES**

- Economy Packaging
- Fast Switching
- Low Drain-Source 'ON' Resistance

**ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise specified)	
Drain-Source Voltage	30V
Drain-Gate Voltage	30V
Source-Gate Voltage	30V
Forward Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	310 mW
Derate above 25°C	2.8 mW/°C

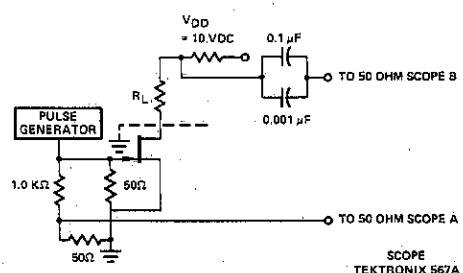
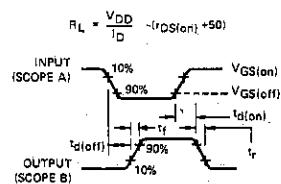


\*When ordering wafer/dice refer to Appendix B-23.

**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

PARAMETER	2N5638		2N5639		2N5640		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX			
BV <sub>GSS</sub>	Gate Reverse Breakdown Voltage	-30	-30	-30	-30	-30	V	I <sub>G</sub> = -10 μA, V <sub>DS</sub> = 0	
I <sub>GSSR</sub>	Gate Reverse Current TA = 100°C	-1.0	-1.0	-1.0	-1.0	-1.0	nA	V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0	
I <sub>D(off)</sub>	Drain Cutoff Current TA = 100°C	1.0	1.0	1.0	1.0	1.0	μA	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = -12 V (2N5638) V <sub>GS</sub> = -8 V (2N5639), V <sub>GS</sub> = -6 V (2N5640)	
I <sub>DS</sub>	Saturation Drain Current	60	25	6.0	6.0	6.0	mA	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 (Note 1)	
V <sub>DSON</sub>	Drain-Source ON Voltage	0.5	0.5	0.5	0.5	0.5	V	V <sub>GS</sub> = 0, I <sub>D</sub> = 12 mA (2N5638); I <sub>D</sub> = 6 mA (2N5639), I <sub>D</sub> = 3 mA (2N5640)	
R <sub>DSON</sub>	Static Drain-Source ON Resistance	30	60	100	100	100	Ω	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	t = 1 kHz
r <sub>dson</sub>	Drain-Source ON Resistance	30	60	100	100	100	Ω	V <sub>GS</sub> = 0, I <sub>D</sub> = 0	
C <sub>iss</sub>	Common-Source Input Capacitance	10	10	10	10	10	pF	V <sub>GS</sub> = -12 V, V <sub>DS</sub> = 0	f = 1 MHz
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	4.0	4.0	4.0	4.0	4.0	pF		
t <sub>d(on)</sub>	Turn-On Delay Time	4.0	6.0	8.0	8.0	8.0	ns	V <sub>DD</sub> = 10 V I <sub>D(on)</sub> = 12 mA (2N5638) V <sub>GS(on)</sub> = 0 I <sub>D(on)</sub> = 6 mA (2N5639) V <sub>GS(off)</sub> = -10 V I <sub>D(on)</sub> = 3 mA (2N5640)	
t <sub>r</sub>	Rise Time	5.0	8.0	10	10	10	ns		
t <sub>d</sub>	Turn-Off Delay Time	5.0	10	15	15	15	ns		
t <sub>f</sub>	Fall Time	10	20	30	30	30	ns	R <sub>G</sub> = 50 Ω	

NOTE: 1. Pulse test; PW ≤ 300μs, duty cycle ≤ 3.0%.



SCOPE  
TEKTRONIX 567A  
OR EQUIVALENT



# 2N5902-2N5909

## Monolithic Dual N-Channel JFET

### FEATURES

- Tight Tracking
- Good Matching

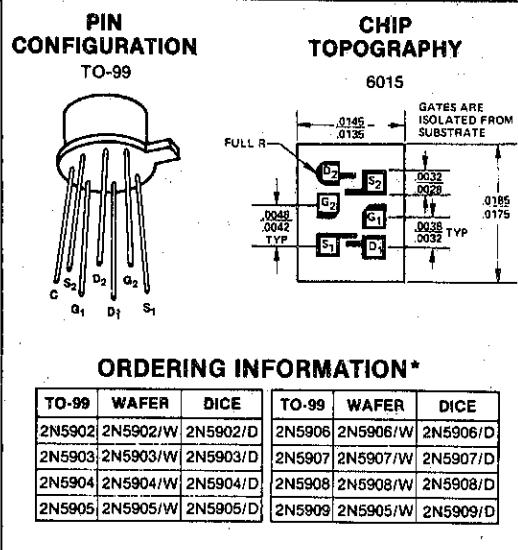
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### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Gate-Drain or Gate-Source

	ONE SIDE	BOTH SIDES
Power Dissipation	367 mW	500 mW
Derate above $25^\circ\text{C}$	3 mW/ $^\circ\text{C}$	4 mW/ $^\circ\text{C}$
Voltage (Note 1)	-40V	
Gate Current (Note 1)	10 mA	
Storage Temperature Range	-65°C to +200°C	
Operating Temperature Range	-55°C to +150°C	
Lead Temperature (Soldering, 10 sec.)	+300°C	



### ORDERING INFORMATION\*

TO-99	WAFER	DICE	TO-99	WAFER	DICE
2N5902	2N5902/W	2N5902/D	2N5906	2N5906/W	2N5906/D
2N5903	2N5903/W	2N5903/D	2N5907	2N5907/W	2N5907/D
2N5904	2N5904/W	2N5904/D	2N5908	2N5908/W	2N5908/D
2N5905	2N5905/W	2N5905/D	2N5909	2N5909/W	2N5909/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER		2N5902-5		2N5906-9		UNIT	TEST CONDITIONS					
		MIN	MAX	MIN	MAX							
I <sub>GSSR</sub>	Gate Reverse Current $T_A = 125^\circ\text{C}$	-5	-10	-2	-5	pA	$V_{GS} = -20\text{ V}, V_{DS} = 0$					
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-40	-40				$I_G = -1\text{ }\mu\text{A}, V_{DS} = 0$					
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ nA}$					
V <sub>GS</sub>	Gate-Source Voltage	-4	-4	-4	-4		$VDG = 10\text{ V}, I_D = 30\text{ }\mu\text{A}$					
I <sub>G</sub>	Gate Operating Current $T_A = 125^\circ\text{C}$	-3	-3	-1	-1	pA						
I <sub>DSS</sub>	Saturation Drain Current	30	500	30	500	μA						
g <sub>fs</sub>	Common-Source Forward Transconductance	70	250	70	250		$V_{DS} = 10\text{ V}, V_{GS} = 0$					
g <sub>os</sub>	Common-Source Output Conductance	5	5	5	5	μmho	$f = 1\text{ kHz}$					
C <sub>iss</sub>	Common-Source Input Capacitance	3	3	3	3	pF	$f = 1\text{ MHz}$					
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	1.5	1.5	1.5	1.5							
g <sub>fs</sub>	Common-Source Forward Transconductance	50	150	50	160	μmho	$f = 1\text{ kHz}$					
g <sub>os</sub>	Common-Source Output Conductance	1	1	1	1	μmho	$f = 100\text{ Hz}$					
ε <sub>n</sub>	Equivalent Short Circuit Input Noise Voltage	0.2		0.1		μV/√Hz	$R_G = 10\text{ M}\Omega$					
NF	Spot Noise Figure	3		1		dB						
PARAMETER		2N5902-6		2N5903-7		2N5904-8		2N5905-9		UNIT	TEST CONDITIONS	
I <sub>G1</sub> -I <sub>G2</sub>	Differential Gate Current	MIN 2.0		MIN 2.0		MIN 2.0		MIN 2.0		nA	$VDG = 10\text{ V}, I_D = 30\text{ }\mu\text{A}, T_A = 125^\circ\text{C}$	
		MAX 0.2		MAX 0.2		MAX 0.2		MAX 0.2			2N5902-5, 2N5906-9	
I <sub>DSS1</sub>	Saturation Drain Current Ratio	0.95	1	0.95	1	0.95	1	0.95	1		$V_{DS} = 10\text{ V}, V_{GS} = 0$	
I <sub>DSS2</sub>												
g <sub>fs1</sub>	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1		$f = 1\text{ kHz}$	
IV <sub>GS1</sub> -V <sub>GS2</sub>	Differential Gate-Source Voltage	5		5		10		15			$f = 1\text{ kHz}$	
ΔV <sub>BS1</sub> -V <sub>GS2</sub>   ΔT	Gate-Source Voltage Differential Drift (Measured at end points T <sub>A</sub> and T <sub>B</sub> )	5		10		20		40		μV/°C	$T_A = 25^\circ\text{C}, T_B = 125^\circ\text{C}$	
		5		10		20		40			$T_A = -55^\circ\text{C}, T_B = 25^\circ\text{C}$	
g <sub>os1</sub> -g <sub>os2</sub>	Differential Output Conductance	0.2		0.2		0.2		0.2		μmho	$f = 1\text{ kHz}$	

NOTE 1: Per transistor.

# 2N5911, 2N5912 IT5911, IT5912 Monolithic Dual N-Channel JFET

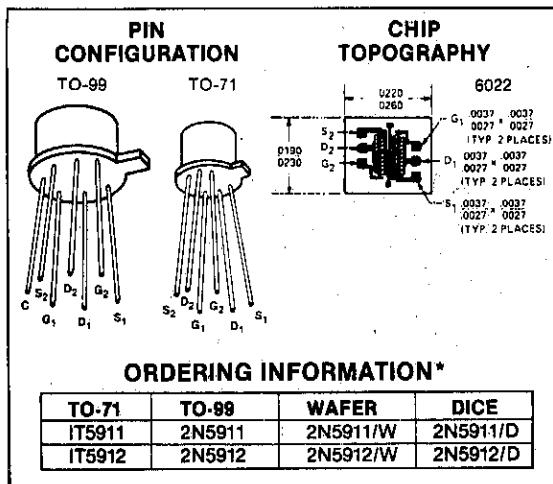
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## FEATURES

- Tight Tracking
- Low Insertion Loss
- Good Matching

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)			
Gate-Drain or Gate Source Voltage			-25V
Gate Current			50 mA
Storage Temperature Range			-65°C to +200°C
Operating Temperature Range			-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)			+300°C
TO-71	TO-99	ONE SIDE	ONE SIDE
		BOTH SIDES	BOTH SIDES
Power Dissipation		300 mW	500 mW
		1.7 mW/°C	2.9 mW/°C
		3.0 mW/°C	4.0 mW/°C



\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I <sub>GSSR</sub>	Gate Reverse Current			pA	V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0	
		T <sub>A</sub> = 150°C		nA		
BV <sub>GSS</sub>	Gate Reverse Breakdown Voltage	-25			I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0	
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	-1	-5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA	
V <sub>GS</sub>	Gate-Source Voltage	-0.3	-4			
I <sub>G</sub>	Gate Operating Current			pA	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA	
		T <sub>A</sub> = 125°C		nA		
I <sub>DSS</sub>	Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	7	40	mA	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V	
g <sub>fs</sub>	Common-Source Forward Transconductance	5000	10,000			f = 1 kHz
g <sub>fs</sub>	Common-Source Forward Transconductance	5000	10,000	μmho		f = 100 MHz
g <sub>os</sub>	Common-Source Output Conductance	100				f = 1 kHz
g <sub>oss</sub>	Common-Source Output Conductance	150				f = 100 MHz
C <sub>iss</sub>	Common-Source Input Capacitance	5		pF	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA	f = 1 MHz
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	1.2		nV/√Hz		f = 10 kHz
ε <sub>n</sub>	Equivalent Short Circuit Input Noise Voltage		20			f = 10 kHz
NF	Spot Noise Figure		1	dB	R <sub>G</sub> = 100 KΩ	
PARAMETER		IT, 2N5911	IT, 2N5912	UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	
I <sub>G1</sub> -I <sub>G2</sub>	Differential Gate Current	20	20	nA	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA	125°C
I <sub>DSS1</sub> /I <sub>DSS2</sub>	Saturation Drain Current Ratio	0.95	1	0.95	1	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 (Pulsewidth 300 μs, duty cycle ≤ 3%)
V <sub>GS1</sub> -V <sub>GS2</sub>	Differential Gate-Source Voltage	10	15	mV		
Δ V <sub>GS1</sub> -V <sub>GS2</sub>  /ΔT	Gate-Source Voltage Differential Drift (Measured at end points, T <sub>A</sub> and T <sub>B</sub> )	20	40	μV/°C	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA	T <sub>A</sub> = 25°C, T <sub>B</sub> = 125°C
g <sub>fs1</sub> /g <sub>fs2</sub>	Transconductance Ratio	0.95	1	0.95	1	T <sub>A</sub> = -55°C, T <sub>B</sub> = 25°C
						f = 1 kHz

**INTERSIL**

# 2N6483-2N6485

## Monolithic Low Noise Dual N-Channel JFET

### FEATURES

- Ultra Low Noise
- High CMRR
- Low Offset
- Tight Tracking.

1

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) .....	-50V
Gate-Gate Voltage .....	$\pm 50\text{V}$
Gate Current (Note 1) .....	50 mA
Storage Temperature Range .....	-65°C to +200°C
Operating Temperature Range .....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C

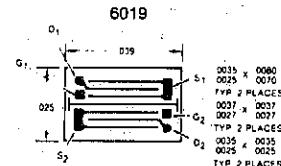
ONE SIDE BOTH SIDES

Power Dissipation .....	250 mW .....	500 mW
Derate above 25°C .....	3.8 mw/ $^\circ\text{C}$ .....	7.7 mw/ $^\circ\text{C}$

### PIN CONFIGURATION



### CHIP TOPOGRAPHY



### ORDERING INFORMATION\*

TO-71	WAFER	DICE
2N6483	2N6483/W	2N6483/D
2N6484	2N6484/W	2N6484/D
2N6485	2N6485/W	2N6485/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
$I_{GSS}$	Gate Reverse Current	200		$\mu\text{A}$	$V_{GS} = -30\text{ V}, V_{DS} = 0$
	$T_A = 150^\circ\text{C}$	200		$\mu\text{A}$	
$BV_{GSS}$	Gate Source Breakdown Voltage	50		V	$I_G = 1\text{ }\mu\text{A}, V_{DS} = 0$
	Gate Source Pinch Off Voltage	0.7	4.0		$V_{DS} = 20\text{ V}, I_D = 1\text{ nA}$
$I_{DSS}$	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	$\text{mA}$	$V_{DS} = 20\text{ V}, V_{GS} = 0$
	Common-Source Forward Transconductance (Note 2)	1000	4000	$\mu\text{mho}$	
$g_{fs}$	Common-Source Output Conductance		10		$V_{DS} = 20\text{ V}, V_{GS} = 0, f = 1\text{ KHz}$
$C_{iss}$	Common-Source Input Capacitance		20	$\text{pF}$	$V_{DS} = 20\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$
	Common-Source Reverse Transfer Capacitance		3.5		
$I_G$	Gate Current	100		$\text{pA}$	$V_{GD} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}$
	$T_A = 150^\circ\text{C}$	100		$\text{nA}$	
$V_{GS}$	Gate-Source Voltage	0.2	3.8	V	$V_{DG} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}$
	Common-Source Forward Transconductance	500	1500	$\mu\text{mho}$	$V_{DG} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}, f = 1\text{ KHz}$
$g_{os}$	Common-Source Output Conductance		1		$V_{DG} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}$
$e_n$	Equivalent Input Noise Voltage	10		$\text{nV}/\sqrt{\text{Hz}}$	$V_{DS} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}, f = 10\text{ Hz}$
		5			$V_{DS} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}, f = 1\text{ KHz}$

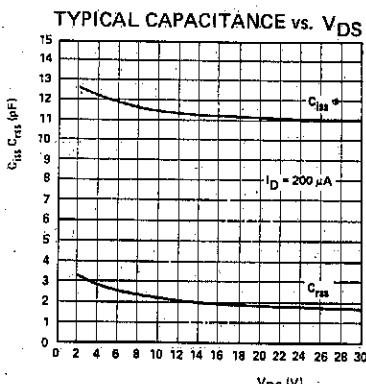
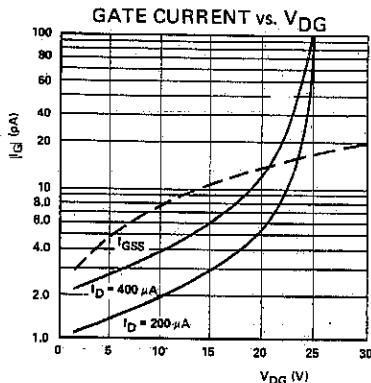
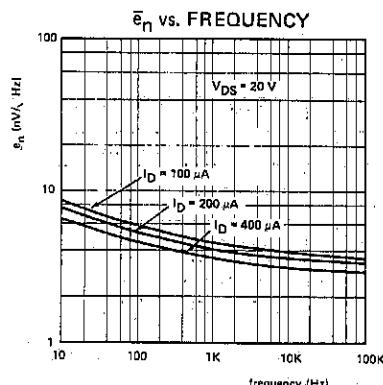
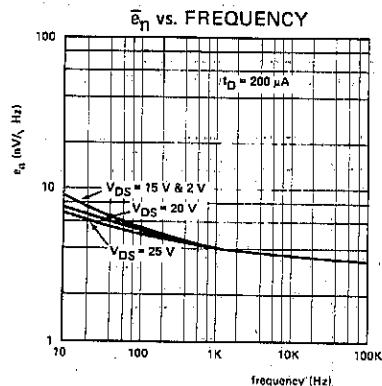
NOTES: 1. Per transistor.  
2. Pulse test required; pulse width = 2 ms.

## MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	PARAMETER	2N6483		2N6484		2N6485		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$ I_{DSS1} $	Drain Current Ratio at Zero Gate Voltage	0.95	1	0.95	1	0.95	1		$V_{DS} = 20 \text{ V}, V_{GS} = 0$ (Note 2)
$ I_{DSS2} $									
$ I_{G1} - I_{G2} $	Differential Gate Current		10		10		10	nA	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$ $T_A = +125^\circ\text{C}$
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1		$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$ , $f = 1 \text{ KHz}$ (Note 2)
$ g_{os1} - g_{os2} $	Differential Output Conductance		0.1		0.1		0.1	$\mu\text{mho}$	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$ , $f = 1 \text{ KHz}$
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		5		10		15	mV	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$
$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
CMRR	Common Mode Rejection Ratio	100		100		90		dB	$V_{DD} = 10$ to $20 \text{ V}$ , $I_D = 200 \mu\text{A}$ (Note 3)

NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.  
 2. Pulse duration of 2 ms used during test.  
 3. CMRR =  $20 \log_{10} \Delta V_{DD} / \Delta |V_{GS1} - V_{GS2}|$ , ( $\Delta V_{DD} = 10 \text{ V}$ ), not included in JEDEC registration

## TYPICAL OPERATING CHARACTERISTICS





# IMF6485

## Monolithic Low Noise Dual N-Channel JFET

### FEATURES

- Ultra Low Noise
- High CMRR
- Low Offset
- Tight Tracking

1

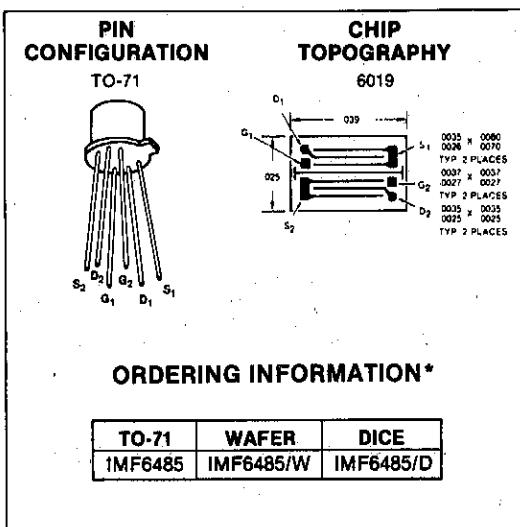
### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	3.8 mW/°C	7.7 mW/°C

### GENERAL DESCRIPTION

This N-Channel Junction FET is characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10 Hz and 1000 Hz. Tight matching specifications make this device ideal as the input stage for low frequency differential instrumentation amplifiers.



\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I <sub>GSS</sub>	Gate Reverse Current TA = 150°C	-200	-200	pA	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0,
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-50		V	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0
V <sub>p</sub>	Gate-Source Pinch-Off Voltage	-0.7	-4.0		V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA
I <sub>DSS</sub>	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	mA	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0
g <sub>fs</sub>	Common-Source Forward Transconductance (Note 2)	1000	4000	μmho	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0, f = 1 KHz
g <sub>oss</sub>	Common-Source Output Conductance		10		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0, f = 1 KHz
C <sub>iss</sub>	Common-Source Input Capacitance		20	pf	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0, f = 1 MHz
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance		3.5		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0, f = 1 MHz
I <sub>G</sub>	Gate Current TA = 150°C	-100	-100	pA	V <sub>GD</sub> = 20 V, I <sub>D</sub> = 200 μA,
V <sub>GS</sub>	Gate-Source Voltage	0.2	-3.8	V	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA
g <sub>fs</sub>	Common-Source Forward Transconductance	500	1500	μmho	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA, f = 1 KHz
g <sub>os</sub>	Common-Source Output Conductance		1		V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA
e <sub>n</sub>		15	10	nV/√Hz	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 200 μA, f = 10 Hz
					V <sub>DS</sub> = 20 V, I <sub>D</sub> = 200 μA, f = 1 KHz

#### NOTES:

1. Per transistor.
2. Pulse test required; pulse width = 2 ms.

## MATCHING CHARACTERISTICS (@ 25° C unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$ I_{DSS1} - I_{DSS2} $	Drain Current Ratio at Zero Gate Voltage	0.95	1		$V_{DS} = 20 \text{ V}$ , $V_{GS} = 0$ (Note 2)
$ I_{G1} - I_{G2} $	Differential Gate Current		10	nA	$V_{DG} = 20 \text{ V}$ , $I_D = 200 \mu\text{A}$ $T_A = +125^\circ \text{C}$
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	0.95	1		$V_{DG} = 20 \text{ V}$ , $I_D = 200 \mu\text{A}$ , $f = 1 \text{ KHz}$ (Note 2)
$ g_{os1} - g_{os2} $	Differential Output Conductance		0.1	$\mu\text{mho}$	$V_{DG} = 20 \text{ V}$ , $I_D = 200 \mu\text{A}$ , $f = 1 \text{ KHz}$
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		25	mV	$V_{DG} = 20 \text{ V}$ , $I_D = 200 \mu\text{A}$
$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$	Gate-Source Voltage Differential Drift		40	$\mu\text{V}/^\circ\text{C}$	$V_{CG} = 20 \text{ V}$ , $I_D = 200 \mu\text{A}$ $T_A = -55^\circ \text{C}$ to $+125^\circ \text{C}$
CMRR	Common Mode Rejection Ratio	90		dB	$V_{DD} = 10$ to $20 \text{ V}$ , $I_D = 200 \mu\text{A}$ (Note 3)

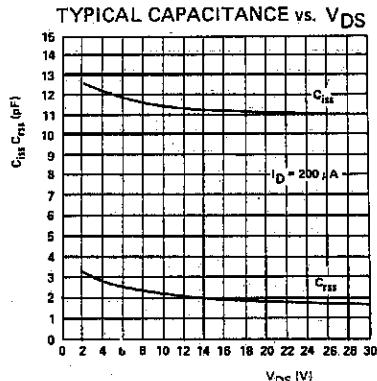
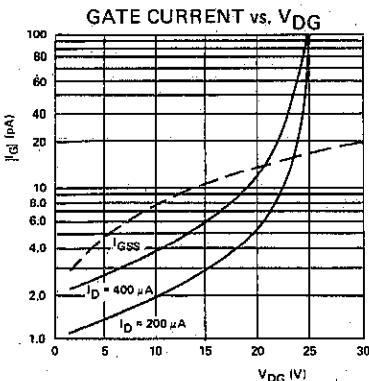
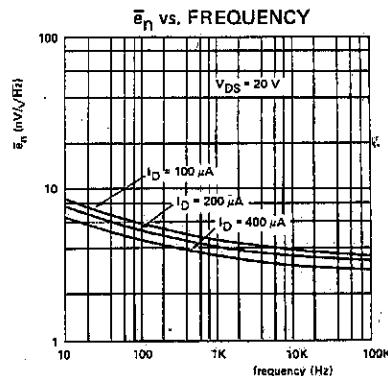
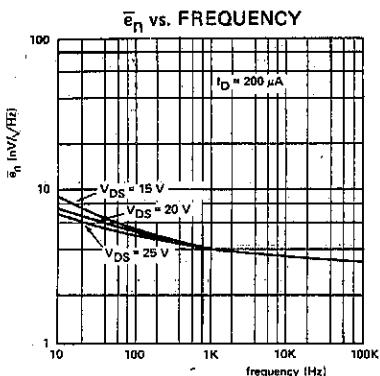
NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

2. Pulse duration of 2 ms used during test.

3. CMRR =  $20 \log_{10} \frac{\Delta V_{DD}}{\Delta V_{GS1} - V_{GS2}}$ , ( $\Delta V_{DD} = 10 \text{ V}$ )

1

## TYPICAL OPERATING CHARACTERISTICS



# Diode Protected P-Channel Enhancement Mode MOSFET

## FEATURES

- Channel Cut Off with Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces Distortion
- Independent Substrate Connection Provides Flexibility in Biasing
- Internally Connected Diode Protects Gate from Damage due to Overvoltage

**1**

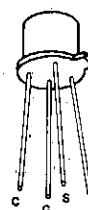
## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

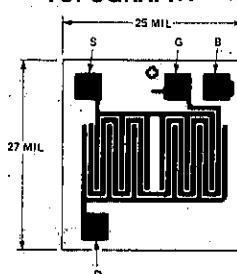
Drain-Source or Drain-Gate Voltage	40V
Drain Current	50 mA
Gate Forward Current	10 $\mu\text{A}$
Gate Reverse Current	1 mA
Storage Temperature	-65°C to +200°C
Operating Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	375 mW
Derate above 25°C	3.0 mW/ $^{\circ}\text{C}$

## PIN CONFIGURATION

TO-72



## CHIP TOPOGRAPHY



## ORDERING INFORMATION\*

TO-72	WAFER	DICE
3N161	3N161/W	3N161/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
$I_{GSS}$ Forward Gate-Terminal Current $T_A = +100^\circ\text{C}$	-100			pA	$V_{GS} = -25\text{ V}$ , $V_{DS} = 0$
$BV_{GSS}$ Forward Gate-Source Break-down Voltage	-25			V	$I_G = 0.1\text{ mA}$ , $V_{DS} = 0$ ,
$I_{DSS}$ Zero-Gate-Voltage Drain Current		-10	-1	nA	$V_{DS} = -15\text{ V}$ , $V_{GS} = 0$
$V_{GS(th)}$ Gate-Source Threshold Voltage	-1.5	-5			$V_{DS} = -15\text{ V}$ , $I_D = -10\text{ }\mu\text{A}$
$V_{GS}$ Gate-Source Voltage	-4.5	-8		V	$V_{DS} = -15\text{ V}$ , $I_D = -8\text{ mA}$
$I_{D(on)}$ On-State Drain Current	-40	-120		mA	$V_{DS} = -15\text{ V}$ , $V_{GS} = -15\text{ V}$
$ Y_{fs} $ Small-Signal Common-Source Forward Transfer Admittance	3500	6500		$\mu\text{mho}$	$f = 1\text{ kHz}$
$ Y_{os} $ Small-Signal Common-Source Output Admittance			250		
$C_{iss}$ Common-Source Short-Circuit Input Capacitance			10	pF	
$C_{rss}$ Common-Source Short-Circuit Reverse Transfer Capacitance			4		$f = 1\text{ MHz}$

# 3N163, 3N164

## P-Channel Enhancement Mode MOS FET

1

**FEATURES**

- Very High Input Impedance
- High Gate Breakdown
- Fast Switching
- Low Capacitance

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

(TA = 25°C unless otherwise noted)

## Drain-Source or Drain-Gate Voltage

3N163 .....	40V
3N164 .....	30V

## Static Gate-Source Voltage

3N163 .....	$\pm 40V$
3N164 .....	$\pm 30V$

## Transient Gate-Source Voltage (Note 2)

3N163 .....	$\pm 125V$
3N164 .....	$\pm 125V$

## Drain Current

3N163 .....	50 mA
3N164 .....	50 mA

## Storage Temperature

3N163 .....	-65°C to +200°C
3N164 .....	-65°C to +200°C

## Operating Temperature

3N163 .....	-55°C to +150°C
3N164 .....	-55°C to +150°C

## Lead Temperature (Soldering, 10 sec.)

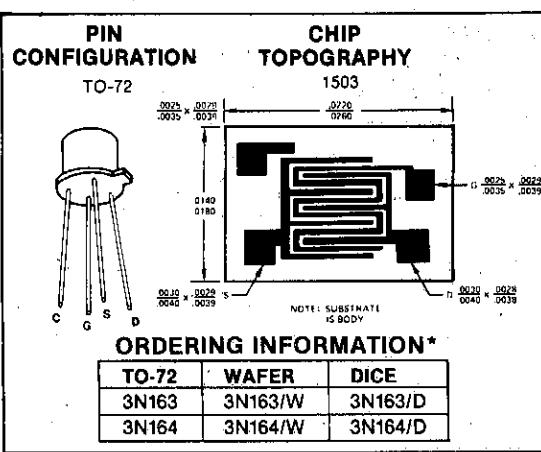
3N163 .....	+300°C
3N164 .....	+300°C

## Power Dissipation

3N163 .....	375 mW
Derate above +25°C .....	3.0 mW/°C

## NOTES:

1. See handling precautions on 3N170 data sheet.
2. Devices must not be tested at  $\pm 125V$  more than once, nor for longer than 300 ms.


**ORDERING INFORMATION\***

TO-72	WAFER	DICE
3N163	3N163/W	3N163/D
3N164	3N164/W	3N164/D

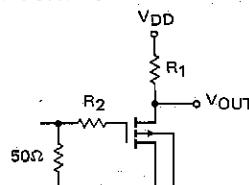
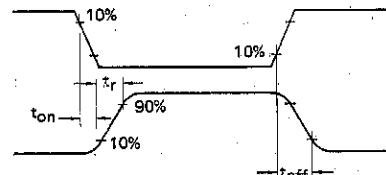
\*When ordering wafer/dice refer to Appendix B-23.

**ELECTRICAL CHARACTERISTICS (@ 25°C and V<sub>BS</sub> = 0 unless noted)**

Symbol	Parameter	3N163		3N164		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I <sub>GSSR</sub>	Gate Reverse Leakage Current		10		10		
I <sub>GSSF</sub>	Gate Forward Current		-10		-10	pA	V <sub>GS</sub> = -40V (3N163) V <sub>GS</sub> = -30V (3N164)
	T <sub>A</sub> = +125°C		-25		-25		
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	-40		-30			I <sub>D</sub> > -10 μA, V <sub>GS</sub> = 0
BV <sub>SOS</sub>	Source Drain Breakdown Voltage	-40		-30			I <sub>S</sub> > -10 μA, V <sub>GD</sub> = 0, V <sub>DB</sub> = 0
V <sub>GS(th)</sub>	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -10 μA
V <sub>GS(th)</sub>	Threshold Voltage	-2.0	-5.0	-2.0	-5.0		V <sub>DS</sub> = -15V, I <sub>D</sub> = -10 μA
V <sub>GS</sub>	Gate Source Voltage	-3.0	-6.5	-3.0	-6.5		V <sub>DS</sub> = -15V, I <sub>D</sub> = -0.5 mA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	200		400		pA	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0
I <sub>SDS</sub>	Source Drain Current	400		800		pA	V <sub>SD</sub> = 15V, V <sub>GS</sub> = V <sub>DB</sub> = 0
R <sub>DS(on)</sub>	Drain-Source on Resistance	250		300		ohms	V <sub>GS</sub> = -20V, I <sub>D</sub> = -100 μA
I <sub>on</sub>	On Drain Current	-5.0	-30.0	-3.0	-30.0	mA	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V
g <sub>f</sub>	Forward Transconductance	2000	4000	1000	4000	μmhos	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10 mA, f = 1 kHz
g <sub>os</sub>	Output Admittance	250		250			
C <sub>iss</sub>	Input Capacitance - Output Shorted	2.5		2.5		pF	
C <sub>rss</sub>	Reverse Transfer Capacitance	0.7		0.7			
C <sub>oss</sub>	Output-Capacitance Input Shorted	3.0		3.0			V <sub>DS</sub> = -15V, I <sub>D</sub> = -10 mA, f = 1 MHz

**SWITCHING CHARACTERISTICS (@ 25°C and V<sub>BS</sub> = 0)**

t <sub>on</sub>	Turn-On Delay Time	12		12		ns	V <sub>DD</sub> = -15V
t <sub>r</sub>	Rise Time	24		24			I <sub>on(av)</sub> = -10 mA
t <sub>off</sub>	Turn-Off Time	50		50			R <sub>G</sub> = R <sub>L</sub> = 1.4 kΩ

**SWITCHING TIME CIRCUIT**

**SWITCHING WAVEFORM**




# 3N165, 3N166 Dual P-Channel Enhancement Mode MOS FET

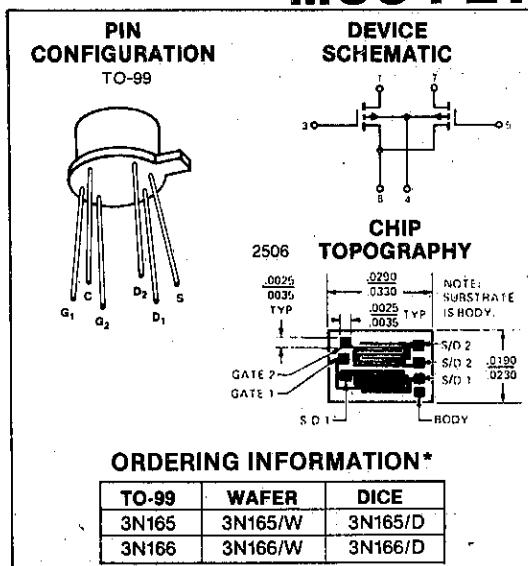
## FEATURES

- Very High Impedance
- High Gate Breakdown
- Low Capacitance

1

## ABSOLUTE MAXIMUM RATINGS (Note 1)

(TA = 25°C unless otherwise specified)	
Drain-Source or Drain-Gate Voltage (Note 2)	
3N165 .....	40V
3N166 .....	30V
Transient Gate-Source Voltage (Note 3) .....	±125
Gate-Gate Voltage .....	±80V
Drain Current (Note 2) .....	50 mA
Storage Temperature .....	-65°C to +200°C
Operating Temperature .....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C
Power Dissipation	
One Side .....	300 mW
Both Sides .....	525 mW
Total Derating above 25°C .....	4.2 mW/°C



## ORDERING INFORMATION\*

TO-99	WAFER	DICE
3N165	3N165/W	3N165/D
3N166	3N166/W	3N166/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (@ 25°C and V<sub>BS</sub> = 0 unless notes)

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
I <sub>GSSR</sub>	Gate Reverse Leakage Current		10	pA	V <sub>GS</sub> = 40V
I <sub>GSSF</sub>	Gate Forward Leakage Current		-10		V <sub>GS</sub> = -40V
	TA = +125°C		-25		
I <sub>DSS</sub>	Drain to Source Leakage Current		-200		V <sub>DS</sub> = -20V
I <sub>SDS</sub>	Source to Drain Leakage Current		-400		V <sub>SD</sub> = -20, V <sub>DB</sub> = 0
I <sub>D(on)</sub>	On Drain Current	-5	-30	mA	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V
V <sub>GS(th)</sub>	Gate Source Threshold Voltage	-2	-5	V	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10μA
V <sub>GS(th)</sub>	Gate Source Threshold Voltage	-2	-5		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -10μA
r <sub>D(on)</sub>	Drain Source ON Resistance	300		ohms	V <sub>GS</sub> = -20V, I <sub>D</sub> = -100μA
G <sub>fs</sub>	Forward Transconductance	1500	3000	μhos	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA, f = 1kHz
G <sub>os</sub>	Output Admittance		300		V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA, f = 1MHz
C <sub>iss</sub>	Input Capacitance		3.0	pF	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA, f = 1MHz
C <sub>rss</sub>	Reverse Transfer Capacitance		0.7		
C <sub>oss</sub>	Output Capacitance		3.0		
R <sub>E(Y<sub>fs</sub>)</sub>	Common Source Forward Transconductance	1200		μhos	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA, f = 100MHz

## MATCHING CHARACTERISTICS 3N165

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
Y <sub>fs1</sub> /Y <sub>fs2</sub>	Forward Transconductance Ratio	0.90	1.0		V <sub>DS</sub> = -15V, I <sub>D</sub> = -1500μA, f = 1KHz
V <sub>GS1-2</sub>	Gate-Source Threshold Voltage Differential		100	mV	V <sub>DS</sub> = -15V, I <sub>D</sub> = -500μA
ΔV <sub>GS1-2</sub> ΔT	Gate Source Threshold Voltage Differential Change with Temperature		100	μV/°C	V <sub>DS</sub> = -15V, I <sub>D</sub> = -500μA TA = -55°C to +25°C
			100		

Note 1: See handling precautions on 3N170 data sheet.

Note 2: Per transistor.

Note 3: Devices must not be tested at ±125V more than once, nor for longer than 300 ms.

# 3N170, 3N171

## N-Channel Enhancement Mode MOS FET

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### FEATURES

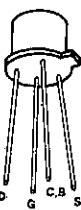
- Low Switching Voltages
- Fast Switching Times
- Low Drain-Source Resistance
- Low Reverse Transfer Capacitance

### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)	
Drain-Gate Voltage	..... ±35V
Drain-Source Voltage	..... 25V
Gate-Source Voltage	..... ±35V
Drain Current	..... 30 mA
Storage Temperature	
Range	-65°C to +200°C
Operating Temperature	
Range	-55°C to +150°C
Lead Temperature	
(Soldering, 10 sec.)	+300°C
Power Dissipation	..... 300 mW
Derate above 25°C	..... 1.7 mW/°C

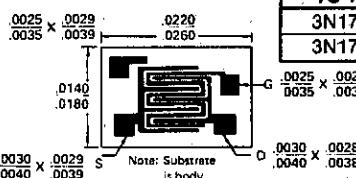
### PIN CONFIGURATION

TO-72



### CHIP TOPOGRAPHY

1003



### HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow the procedures outlined below.

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on as transient voltages may cause permanent damage to the devices.

### ORDERING INFORMATION\*

TO-72	WAFER	DICE
3N170	3N170/W	3N170/D
3N171	3N170/W	3N170/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
BVDSS	Drain-Source Breakdown Voltage	25	V	VID = 10 µA, VGS = 0
I <sub>GSS</sub>	Gate Leakage Current	10	pA	VGS = -35 V, VDS = 0
I <sub>DSS</sub>	Zero-Gate-Voltage Drain Current	100	nA	VDS = 10 V, VGS = 0
	TA = 125°C			
	TA = 125°C	1.0	µA	
V <sub>GS(th)</sub>	Gate-Source Threshold Voltage	3N170	1.0	VDS = 10 V, ID = 10 µA
	3N171	1.5	2.0	
I <sub>D(on)</sub>	"ON" Drain-Current	2.0	mA	VGS = 10 V, VDS = 10 V
V <sub>DS(on)</sub>	Drain-Source "ON" Voltage	100	V	ID = 10 mA, VGS = 10 V
r <sub>ds(on)</sub>	Drain-Source ON Resistance	200	Ω	VGS = 10 V, ID = 0, f = 1.0 kHz
Y <sub>fs</sub>	Forward Transfer Admittance	1000	µmhos	VDS = 10 V, ID = 2.0 mA, f = 1.0 kHz
C <sub>rss</sub>	Reverse Transfer Capacitance	1.3		VDS = 0, VGS = 0, f = 1.0 MHz
C <sub>iss</sub>	Input Capacitance	5.0	pF	VDS = 10 V, VGS = 0, f = 1.0 MHz
C <sub>d(sub)</sub>	Drain-Substrate Capacitance	5.0		VD(SUB) = 10 V, f = 1.0 MHz
t <sub>d(on)</sub>	Turn-On Delay Time	3.0		
t <sub>r</sub>	Rise Time	10	ns	V <sub>DD</sub> = 10 V, ID(on) = 10 mA, VGS(on) = 10 V, VGS(off) = 0, RG = 50 Ω
t <sub>d(off)</sub>	Turn-Off Delay Time	3.0		
t <sub>f</sub>	Fall Time	15		



# 3N172, 3N173

## Diode Protected P-Channel Enhancement Mode MOS FET

1

### FEATURES

- High Input Impedance
- Diode Protected Gate

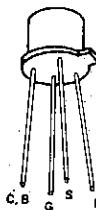
### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

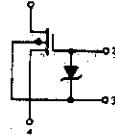
Drain-Source or Drain-Gate Voltage	
3N172	40V
3N173	30V
Drain Current	50 mA
Gate Forward Current	10 $\mu$ A
Gate Reverse Current	1 mA
Storage Temperature	-65°C to +200°C
Operating Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	375 mW
Derate above 25°C	3.0 mW/°C

### PIN CONFIGURATION

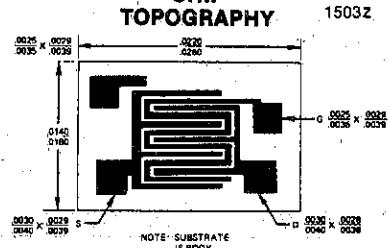
TO-72



### DEVICE SCHEMATIC



### CHIP TOPOGRAPHY



1503Z

### ORDERING INFORMATION\*

TO-72	WAFER	DICE
3N172	3N172/W	3N172/D
3N173	3N173/W	3N173/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS (@ 25°C and V<sub>BS</sub> = 0 unless noted)

PARAMETER		3N172		3N173		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I <sub>GSSR</sub>	Gate Reverse Current	-200		-500		pA	V <sub>GS</sub> = -20V
	TA = +125°C	-0.5		-1.0		μA	
BV <sub>GSS</sub>	Gate Breakdown Voltage	-40	-125	-30	-125	V	I <sub>D</sub> = -10 μA
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	-40		-30		V	I <sub>D</sub> = -10 μA
BV <sub>SDS</sub>	Source-Drain Breakdown Voltage	-40		-30		V	I <sub>S</sub> = -10 μA, V <sub>DS</sub> = 0
V <sub>GS(th)</sub>	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -10 μA
		-2.0	-5.0	-2.0	-5.0	V	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10 μA
V <sub>GS</sub>	Gate Source Voltage	-3.0	-6.5	-2.5	-6.5	V	V <sub>DS</sub> = -15V, I <sub>D</sub> = -500 μA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current		-0.4		-10	nA	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0
I <sub>SDS</sub>	Zero Gate Voltage Source Current		-0.4		-10	nA	V <sub>SD</sub> = -15V, V <sub>DB</sub> = 0, V <sub>GD</sub> = 0
r <sub>dson</sub>	Drain Source On Resistance		250		350	ohms	V <sub>GS</sub> = -20V, I <sub>D</sub> = -100 μA
I <sub>D(on)</sub>	On Drain Current	-5.0	-30	-5.0	-30	mA	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V



# 3N188-3N191

## Dual P-Channel Enhancement Mode MOSFET

### FEATURES

- Very High Input Impedance
- High Gate Breakdown 3N190-3N191
- Zener Protected gate 3N188-3N189
- Low Capacitance

### ABSOLUTE MAXIMUM RATINGS

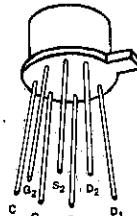
( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Drain-Source or Drain-Gate Voltage (Note 1)

3N188, 3N189	.....	40V
3N190, 3N191	.....	30V
Transient Gate-Source Voltage (Notes 1 and 2)	.....	$\pm 125\text{V}$
Gate-Gate Voltage	.....	$\pm 80\text{V}$
Drain Current (Note 1)	.....	50 mA
Storage Temperature	.....	$-65^\circ\text{C}$ to $+200^\circ\text{C}$
Operating Temperature	.....	$-55^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	.....	$+300^\circ\text{C}$
Power Dissipation		
One Side	.....	300 mW
Both Sides	.....	525 mW
Total Derating above $25^\circ\text{C}$	.....	4.2 mW/ $^\circ\text{C}$

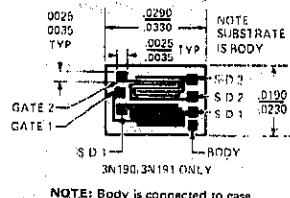
### PIN CONFIGURATION

TO-99



### CHIP TOPOGRAPHY

2506



NOTE: Body is connected to case.

### ORDERING INFORMATION\*

TO-99	WAFER	DICE
3N188	—	—
3N189	—	—
3N190	3N190/W	3N190/D
3N191	3N191/W	3N191/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS (25°C and $V_{BS} = 0$ unless otherwise noted)

PARAMETER	3N188		3N190 3N191		UNITS	TEST CONDITIONS
	MIN	MAX	MIN	MAX		
$I_{GSSR}$	Gate Reverse Current			10		
$I_{GSSF}$	Gate Forward Current				pA	
						$V_{GS} = 40\text{V}$
						$V_{GS} = -40\text{V}$
$BV_{DSS}$	Drain-Source Breakdown Voltage	-40		-40		
$BV_{SDS}$	Source-Drain Breakdown Voltage	-40		-40		
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V
		-2.0	-5.0	-2.0	-5.0	
$V_{GS}$	Gate Source Voltage	-3.0	-6.5	-3.0	-6.5	
$I_{DS(0)}$	Zero Gate Voltage Drain Current	-200		-200		
$I_{DS}$	Source Drain Current	-400		-400	pA	
$r_{DS(on)}$	Drain-Source on Resistance	300		300	ohms	
$ I_D _{on}$	On Drain Current	-5.0	-30.0	-5.0	-30.0	mA
$g_{fs}$	Forward Transconductance (Note 3)	1500	4000	1500	4000	
$Y_{os}$	Output Admittance	300		300	$\mu\text{mhos}$	
$C_{iss}$	Input Capacitance Output Shorted	4.5		4.5		
$C_{rss}$	Reverse Transfer Capacitance	1.5		1.0	pF	
$C_{oss}$	Output Capacitance Input Shorted	3.0		3.0		

### SWITCHING CHARACTERISTICS (@ 25°C and $V_{BS} = 0$ unless noted)

		MIN	MAX	UNITS	TEST CONDITIONS
$t_{on}$	Turn On Delay Time	15		ns	$V_{DD} = -15\text{V}, I_D = -5\text{mA}$
$t_r$	Rise Time	.30			$R_G = R_L = 1.4\text{k}\Omega$
$t_{off}$	Turn Off Time	50			

### MATCHING CHARACTERISTICS (@ 25°C and $V_{BS} = 0$ unless noted) 3N188 and 3N190

		MIN	MAX	UNITS	
$Y_{f11}/Y_{f22}$	Forward Transconductance Ratio	0.85	1.0		$V_{DS} = -15\text{V}, I_D = -500\text{\mu A}, f = 1\text{kHz}$
$V_{GS1-2}$	Gate Source Threshold Voltage Differential	100	mV		$V_{DS} = -15\text{V}, I_D = -500\text{\mu A}$
$\Delta V_{GS1-2}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)	100	$\mu\text{V/}^\circ\text{C}$		$V_{DS} = -15\text{V}, I_D = -500\text{\mu A}, T = -55^\circ\text{C to }+25^\circ\text{C}$
$\Delta V_{GS1-2}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)	100	$\mu\text{V/}^\circ\text{C}$		$V_{DS} = -15\text{V}, I_D = -500\text{\mu A}, T = +25^\circ\text{C to }+125^\circ\text{C}$

### NOTES:

- Per transistor
- Approximately doubles for every  $10^\circ\text{C}$  increase in  $T_A$ .



## FEATURES

- $I_R = 0.1 \text{ pA (typical)}$
- $BV_R > 30 \text{ V}$
- $C_{rss} = 0.75 \text{ pF (typical)}$

## 1

### GENERAL DESCRIPTION

The ID100 and ID101 are monolithic dual diodes intended for use in applications requiring extremely low leakage currents. Applications include interstage coupling with reverse isolation, signal clipping and clamping and protection of ultra low leakage FET differential dual and operational amplifiers.

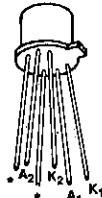
### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Diode Reverse Voltage	.....	30V
Diode to Diode Voltage	.....	$\pm 50\text{V}$
Forward Current	.....	20 mA
Reverse Current	.....	100 $\mu\text{A}$
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	300 mW
Derate above 25°C	.....	1.7 mW/°C

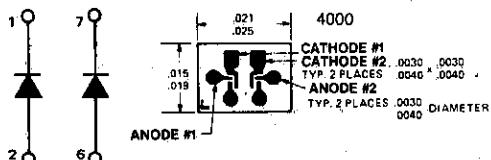
### PIN CONFIGURATIONS

TO-71  
TO-78



\*These leads must not be tied together nor connected to the circuit in any way.

### CHIP TOPOGRAPHY



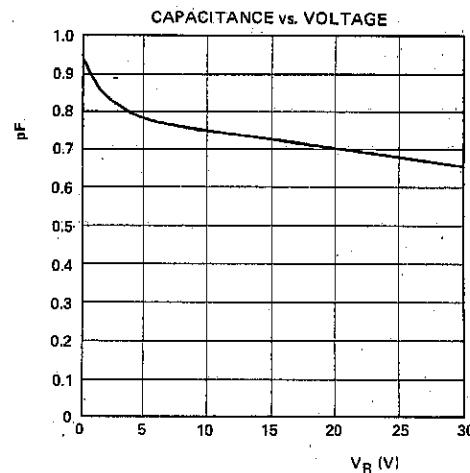
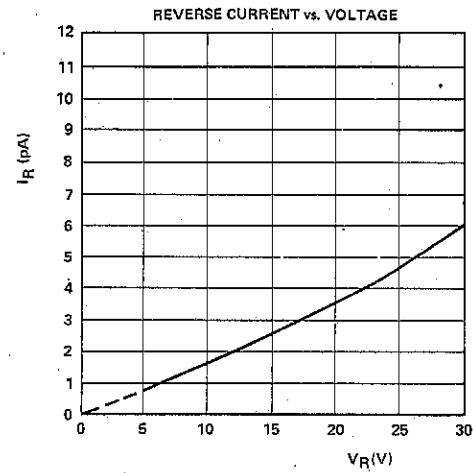
### ORDERING INFORMATION\*

TO78	TO71	WAFER	CHIP
ID100	ID101	ID100/W	ID100/D

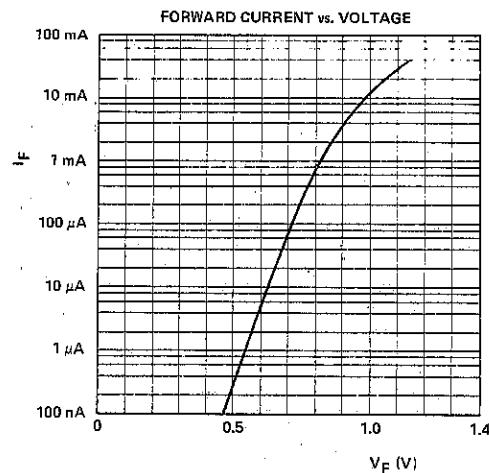
\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		ID100, ID101			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
$V_F$	Forward Voltage Drop	0.8		1.1	V	$I_F = 10 \text{ mA}$
$BV_R$	Reverse Breakdown Voltage	30			V	$I_R = 1 \mu\text{A}$
$I_R$	Reverse Leakage Current		0.1		pA	$V_R = 1 \text{ V}$
			2.0	10	nA	$V_R = 10 \text{ V}$
				10		
$ I_{R1} - I_{R2} $	Differential Leakage Current			3	pA	
$C_{rss}$	Total Reverse Capacitance		0.75	1	pF	$V_R = 10 \text{ V}, f = 1 \text{ MHz}$

**TYPICAL CHARACTERISTICS OF ID100/ID101**

1



**FEATURES**

- Interfaces Directly w/T<sup>2</sup>L Logic Elements
- $r_{DS(on)} < 75\Omega$  for 5V Logic Drive
- $I_{D(off)} < 100 \text{ pA}$

**GENERAL DESCRIPTION**

This P-channel JFET has been designed to directly interface with T<sup>2</sup>L logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of  $\pm 15 \text{ V}$  can be switched. The FET is OFF for hi level inputs ( $+5 \text{ V}$  or  $+15 \text{ V}$ ) and ON for low level inputs ( $< 0.5 \text{ V}$  for IT100;  $< 1.5 \text{ V}$  for IT101).

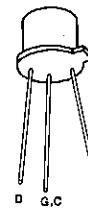
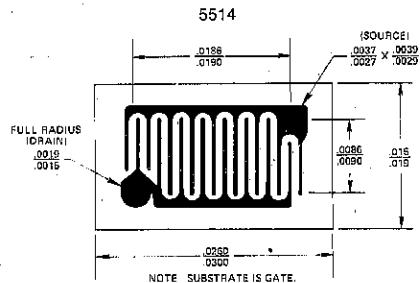
**ABSOLUTE MAXIMUM RATINGS**

( $T_A = 25^\circ \text{C}$  unless otherwise noted)

Gate-Source Voltage .....	35V
Gate-Drain Voltage .....	35V
Gate Current .....	50mA
Storage Temperature Range .....	-65° C to +200° C
Operating Temperature Range .....	-55° C to +150° C
Lead Temperature (Soldering, 10 sec.) .....	+300° C
Power Dissipation .....	300 mW
Derate above 25° C .....	1.7 mW/° C

**PIN CONFIGURATION**

TO-18


**CHIP TOPOGRAPHY**

**ORDERING INFORMATION\***

TO-18	WAFER	DICE
IT100	IT100/W	IT100/D
IT101	IT101/W	IT101/D

\*When ordering wafer/dice refer to Appendix B-23.

**ELECTRICAL CHARACTERISTICS (25° C unless otherwise noted)**

PARAMETER	IT100		IT101		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX		
$I_{DSS}$	Drain Current	-10		-20		mA
$V_P$	Pinch Off Voltage	2	4.5	4	10	V
$BV_{GSS}$	Gate-Source Breakdown Voltage	35		35		
$I_{GSSR}$	Gate Reverse Current		200		200	pA
$g_{fs}$	Transconductance	8		8		mmho
$g_{os}$	Output Conductance		1		1	
$I_{D(off)}$	Drain (OFF) Leakage		-100		-100	pA
$r_{DS(on)}$	Drain-Source "ON" Resistance		75		60	$\Omega$
$C_{iss}$	Input Capacitance		35		35	$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance		12		12	$\text{pF}$



# IT120-IT122 Monolithic Dual NPN Transistor

## FEATURES

- High  $h_{FE}$  at Low Current
- Low Output Capacitance
- Good Matching
- Tight VBE Tracking

## ABSOLUTE MAXIMUM RATINGS

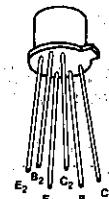
( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Collector-Base Voltage (Note 1)	.....	45V
Collector-Emitter Voltage (Note 1)	.....	45V
Emitter Base Voltage (Notes 1 and 2)	.....	7V
Collector Current (Note 1)	.....	50 mA
Collector-Collector Voltage	.....	60V
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec)	.....	+300°C

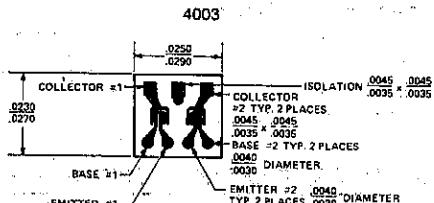
	TO-71	TO-78
Power	ONE SIDE	BOTH SIDES
	ONE SIDE	BOTH SIDES
Dissipation	400 mW	750 mW
Derate Above	26°C	1.7 mW/°C
	2.9 mW/°C	2.3 mW/°C
	4.3 mW/°C	

## PIN CONFIGURATION

TO-71  
TO-78



## CHIP TOPOGRAPHY



## ORDERING INFORMATION\*

TO-78	TO-71	WAFER	DICE
IT120	IT120-T071	IT120/W	IT120/D
IT121	IT121-T071	IT121/W	IT121/D
IT122	IT122-T071	IT122/W	IT122/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS

( $25^\circ\text{C}$  unless otherwise noted)

PARAMETER	IT120A		IT120		IT121		IT122		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$h_{FE}$	DC Current Gain		200	200	80	80	80	80		$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
	225		225		100		100			$I_C = 1.0 \text{ mA}, V_{CE} = 5.0 \text{ V}$
$V_{BE(ON)}$	Emitter-Base On Voltage		0.7	0.7	0.7	0.7	0.7	0.7		$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
										$I_C = 0.5 \text{ mA}, I_B = 0.05 \text{ mA}$
$I_{CBO}$	Collector Cutoff Current		1.0	1.0	1.0	1.0	1.0	1.0		$I_E = 0, V_{CB} = 45 \text{ V}$
			$T_A = +150^\circ\text{C}$		10	10	10	10		$I_E = 0, V_{EB} = 5.0 \text{ V}$
$I_{EBO}$	Emitter Cutoff Current		1.0	1.0	1.0	1.0	1.0	1.0		$I_C = 0, V_{EB} = 5.0 \text{ V}$
$C_{obo}$	Output Capacitance		2.0	2.0	2.0	2.0	2.0	2.0		$I_E = 0, V_{CB} = 5.0 \text{ V}$
$C_{te}$	Emitter Transition Capacitance		2.5	2.5	2.5	2.5	2.5	2.5		$f = 1 \text{ MHz}$
$C_{C1-C2}$	Collector to Collector Capacitance		4.0	4.0	4.0	4.0	4.0	4.0		$V_{CC} = 0$
$I_{C1-C2}$	Collector to Collector Leakage Current		10	10	10	10	10	10		$V_{CC} = \pm 60 \text{ V}$
$V_{CEO(SUST)}$	Collector to Emitter Sustaining Voltage		45	45	45	45	45	45		$I_C = 1.0 \text{ mA}, I_B = 0$
$GBW$	Current Gain Bandwidth Product		10	10	7	7	7	7		$I_C = 10 \mu\text{A}, V_{CE} = 5 \text{ V}$
			220	220	180	180	180	180		$I_C = 1 \text{ mA}, V_{CE} = 5 \text{ V}$
$ IV_{BE1}-V_{BE2} $	Base-Emitter Voltage Differential		1	2	3	3	5	5		$\text{mV}$
$ I_{B1}-I_{B2} $	Base Current Differential		2.5	5	25	25	25	25		$\text{nA}$
$\Delta(V_{BE1} - V_{BE2})$	Base-Emitter Voltage Differential Change with Temperature		3	5	10	10	20	20		$\mu\text{V}/^\circ\text{C}$
										$T_A = -55^\circ\text{C} \text{ to } +125^\circ\text{C}$
										$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10  $\mu\text{A}$ .

# IT124

## Monolithic Dual Super-Beta NPN Transistor

**1**

### FEATURES

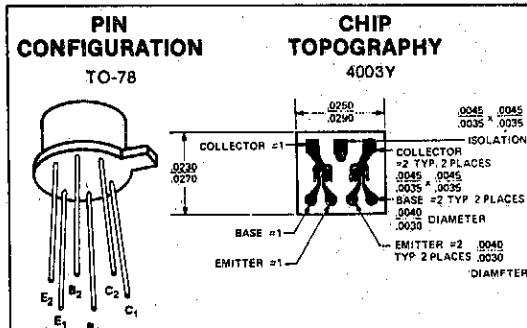
- Very High Gain
- Low Output Capacitance
- Tight V<sub>BE</sub> Matching
- High GBW

### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

	TO-78	
	ONE SIDE	BOTH SIDES
Collector-Base Voltage (Note 1)	2V	
Collector-Emitter Voltage (Note 1)	2V	
Emitter-Base Voltage (Notes 1 and 2)	7V	
Collector-Current (Note 1)	10 mA	
Collector-Collector Voltage	100V	
Storage Temperature Range	-65°C to +200°C	
Operating Temperature Range	-55°C to +150°C	
Lead Temperature (Soldering, 10 sec)	+300°C	

	TO-78			
	Power Dissipation	Dissipation above 25°C	ONE SIDE	BOTH SIDES
	300 mW	1.7 mW/°C	500 mW	4.3 mW/°C



### ORDERING INFORMATION\*

TO-78	WAFER	DICE
IT124	IT124/W	IT124/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
$\text{h}_{FE}$	DC Current Gain	1500			$I_C = 1\mu\text{A}, V_{CE} = 1\text{V}$
		1500			$I_C = 10\mu\text{A}, V_{CE} = 1\text{V}$
	TA = -55°C	600			
$V_{BE(ON)}$	Emitter-Base "ON" Voltage	0.7		V	
$V_{CE(SAT)}$	Collector Saturation Voltage	0.5			$I_C = 1\text{mA}, I_E = 0.1\text{mA}$
$I_{CBO}$	Collector Cutoff Current	100		pA	$I_E = 0, V_{CB} = 1\text{V}$
		100		nA	
$I_{EBO}$	Emitter Cutoff Current	100		pA	$I_C = 0, V_{EB} = 5\text{V}$
		100		pA	$I_E = 0, V_{CB} = 1\text{V}$
$C_{obo}$	Output Capacitance	0.8		pF	$f = 1\text{ MHz}$
$C_{te}$	Emitter Transition Capacitance	1.0		pF	
$C_{c1c2}$	Collector to Collector Capacitance	0.8			
$I_{c1c2}$	Collector to Collector Leakage Current	250		pA	$V_{CC} = \pm 50\text{V}$
$GBW$	Current Gain Bandwidth Product	10		MHz	$I_C = 10\mu\text{A}, V_{CE} = 1\text{V}$
		100		MHz	$I_C = 100\mu\text{A}, V_{CE} = 1\text{V}$
$NF$	Narrow Band Noise Figure		3	dB	$I_C = 10\mu\text{A}, V_{CE} = 3\text{V}, f = 1\text{ KHz}, R_G = 10\text{ Kohms}, BW = 200\text{ Hz}$
$BV_{CBO}$	Collector-Base Breakdown Voltage	2		V	$I_C = 10\mu\text{A}, I_E = 0$
$BV_{EBO}$ (Note 2)	Emitter-Base Breakdown Voltage	7		V	$I_E = 10\mu\text{A}, I_C = 0$
$V_{CEO(SUST)}$	Collector-Emitter Sustaining Voltage	2			$I_C = 1\text{mA}, I_B = 0$

### MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TYP	MAX	UNITS	CONDITIONS
$ V_{BE1}-V_{BE2} $	Base Emitter Voltage Differential	2	5	mV	$I_C = 10\mu\text{A}, V_{CE} = 1\text{V}$
$\Delta(V_{BE1}-V_{BE2})/\Delta T$	Base Emitter Voltage Differential Change with Temperature	5	15	$\mu\text{V}/^\circ\text{C}$	$I_C = 10\mu\text{A}, V_{CE} = 1\text{V}$ $T = -55^\circ\text{C} \text{ to } +125^\circ\text{C}$
$ I_{B1}-I_{B2} $	Base Current Differential		.6	nA	$I_C = 10\mu\text{A}, V_{CE} = 1\text{V}$

### NOTES:

1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 $\mu\text{A}$ .



## FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Tight  $I_B$  Match
- Tight  $V_{BE}$  Tracking
- Dielectric Isolated Matched Pairs for Differential Amplifiers

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ C$  unless otherwise specified)

### Collector-Base Voltage (Note 1)

IT126, IT127	.....	60V
IT128	.....	55V
IT129	.....	45V

### Collector-Emitter Voltage (Note 1)

IT126, IT127	.....	60V
IT128	.....	55V
IT129	.....	45V

### Emitter-Base Voltage (Notes 1 and 2)

7.0V

### Collector Current (Note 1)

100 mA

### Collector-Collector Voltage

70V

### Storage Temperature Range

-65°C to +200°C

### Operating Temperature Range

-55°C to +150°C

### Lead Temperature (Soldering, 10 sec.)

+300°C

### TO71 TO78

### One Side Both Sides One Side Both Sides

Total Dissipation at 25°C

0.3 Watt 0.5 Watt 0.4 Watt 0.75 Watt

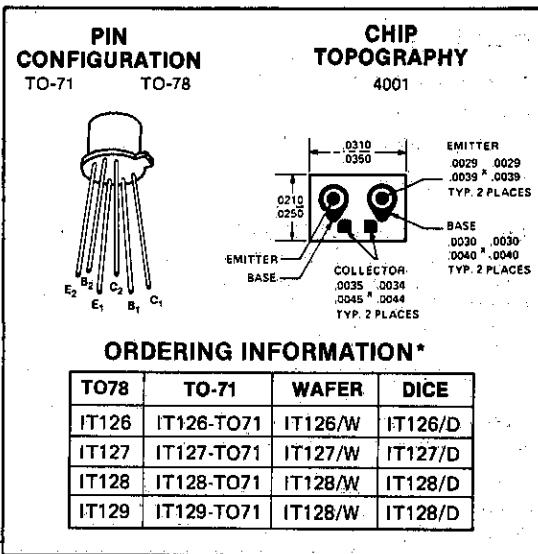
Cast Temperature

1.7 mW/°C 2.9 mW/°C 2.5 mW/°C 4.3 mW/°C

Derating Factor

# IT126-IT129

## Monolithic Dual NPN Transistor



1

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	IT126		IT127		IT128		IT129		UNITS	CONDITIONS		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
$hFE$	DC Current Gain		150		150		100		70*	$I_C = 10 \mu A, V_{CE} = 5V$		
			200	800	200	800	150	800	100			
			230		230		170		115			
			100		100		75		50			
$T_A = -55^\circ C$		75		75		60		40		$I_C = 1 mA, V_{CE} = 5V$		
$V_{BE(on)}$	Emitter-Base On Voltage		.9		.9		.9		.9	V		
			1.0		1.0		1.0		1.0			
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3	$I_C = 10 mA, I_B = 1 mA$		
			1.0		1.0		1.0		1.0			
$I_{CBO}$	Collector Cutoff Current		0.1		0.1		0.1		0.1*	$I_E = 0, V_{CB} = 45V, 30V^*$		
	$T_A = +150^\circ C$		0.1		0.1		0.1		0.1*			
$I_{EBO}$	Emitter Cutoff Current		0.1		0.1		0.1		0.1	$I_C = 0, V_{EB} = 5V$		
$C_{obo}$	Output Capacitance		3		3		3		3	pF $I_E = 0, V_{CB} = 20V$		
$BV_{C1C2}$	Collector-to Collector Breakdown Voltage		$\pm 100$		$\pm 100$		$\pm 100$		$\pm 100$	$I_C = \pm 1 \mu A$		
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage		60		60		55		45	V $I_C = 1 mA, I_B = 0$		
$BV_{CBO}$	Collector Base Breakdown Voltage		60		60		55		45			
$BV_{EBO}$	Emitter Base Breakdown Voltage		7		7		7		7	$I_C = 10 \mu A, I_E = 0$		
MATCHING CHARACTERISTICS												
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential		1		2		3		5	mV $I_C = 1 mA, V_{CE} = 5V$		
$\Delta  V_{BE1} - V_{BE2} /\Delta T$	Base Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu V/^\circ C$ $I_C = 1 mA, V_{CE} = 5V$		
$ I_{B1} - I_{B2} $	Base Current Differential		2.5		5		10		20	nA $I_C = 10 \mu A, V_{CE} = 5V$		
			.25		.5		1.0		2.0	$\mu A I_C = 1 mA, V_{CE} = 5V$		

### NOTES:

1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10  $\mu$  Amps.



# IT130-IT132

## Monolithic Dual PNP Transistor

### FEATURES

- High  $h_{FE}$  at Low Current
- Low Output Capacitance
- Tight  $I_B$  Match
- Tight  $V_{BE}$  Tracking

1

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Collector-Base Voltage (Note 1)	45V
Collector-Emitter Voltage (Note 1)	45V
Emitter Base Voltage (Notes 1 and 2)	7V
Collector Current (Note 1)	50 mA
Collector-Collector Voltage	60V
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

TO-71

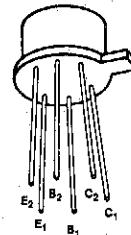
TO-78

	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation	400 mW	750 mW	300 mW	500 mW

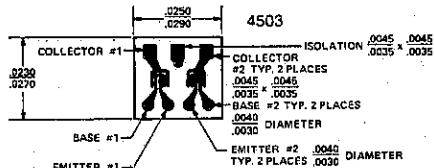
2.3 mW/ $^\circ\text{C}$  4.3 mW/ $^\circ\text{C}$  1.7 mW/ $^\circ\text{C}$  4.3 mW/ $^\circ\text{C}$

### PIN CONFIGURATIONS

TO-71  
TO-78



### CHIP TOPOGRAPHY



### ORDERING INFORMATION\*

TO-78	TO-71	WAFER	DICE
IT130A	IT130A-T071	IT130A/W	IT130A/D
IT130	IT130-T071	IT130/W	IT130/D
IT131	IT131-T071	IT131/W	IT131/D
IT132	IT132-T071	IT132/W	IT132/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

PARAMETER	IT130A		IT130		IT131		IT132		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$h_{FE}$	200	200	80	80						$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
	225	225	100	100						$I_C = 1.0 \text{ mA}, V_{CE} = 5.0 \text{ V}$
	$T_A = -55^\circ\text{C}$	75	75	30	30	30				$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$V_{BE(ON)}$	Emitter-Base On Voltage		0.7	0.7	0.7	0.7	0.7	0.7		$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$V_{CE(SAT)}$	Collector Saturation Voltage		0.5	0.5	0.5	0.5	0.5	0.5		$I_C = 0.5 \text{ mA}, I_B = 0.05 \text{ mA}$
$I_{CBO}$	Collector Cutoff Current		-1.0	-1.0	-1.0	-1.0	-1.0	-1.0	nA	$I_E = 0, V_{CB} = 45 \text{ V}$
$I_{EB0}$	Emitter Cutoff Current		-1.0	-1.0	-1.0	-1.0	-1.0	-1.0	nA	$I_C = 0, V_{EB} = 5.0 \text{ V}$
$C_{ob}$	Output Capacitance		2.0	2.0	2.0	2.0	2.0	2.0	pF	$I_E = 0, V_{CB} = 5.0 \text{ V}$
$C_{te}$	Emitter Transition Capacitance		2.5	2.5	2.5	2.5	2.5	2.5	pF	$I_C = 0, V_{EB} = 0.5 \text{ V}$
$C_{C1-C_2}$	Collector to Collector Capacitance		4.0	4.0	4.0	4.0	4.0	4.0		$V_{CC} = 0$
$I_{C1-C_2}$	Collector to Collector Leakage Current		10	10	10	10	10	10	nA	$V_{CC} = \pm 60 \text{ V}$
$V_{CEO(SUST)}$	Collector to Emitter Sustaining Voltage		-45	-45	-45	-45	-45	-45		$I_C = 1.0 \text{ mA}, I_B = 0$
$GBW$	Current Gain Bandwidth Product		5	5	4	4	4	4	MHz	$I_C = 10 \mu\text{A}, V_{CE} = 5 \text{ V}$
$ V_{BE1}-V_{BE2} $	Base Emitter Voltage Differential		1	2	3	5	5	5	mV	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$ I_{B1}-I_{B2} $	Base Current Differential		2.5	5	25	25	25	25	nA	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$\Delta(V_{BE1}-V_{BE2})/\Delta T$	Base-Emitter Voltage Differential Change with Temperature		3	5	10	20	20	20	$\mu\text{V}/^\circ\text{C}$	$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$

### NOTES:

1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0V, and the reverse base-to-emitter current must never exceed 10  $\mu\text{A}$ .

**FEATURES**

- High Gain at Low Current
- Low Output Capacitance
- Tight  $I_B$  Match
- Tight  $V_{BE}$  Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

**ABSOLUTE MAXIMUM RATINGS**

( $T_A = 25^\circ C$  unless otherwise noted)

## Collector-Base Voltage (Note 1)

IT136, IT137	.....	60V
IT138	.....	55V
IT139	.....	45V

## Collector-Emitter Voltage (Note 1)

IT136, IT137	.....	60V
IT138	.....	55V
IT139	.....	45V

## Emitter-Base Voltage (Notes 1 and 2)

IT136, IT137	.....	7V
--------------	-------	----

Collector Current (Note 1) ..... 100 mA

Collector-Collector Voltage ..... 70V

Storage Temperature Range .....  $-65^\circ C$  to  $+200^\circ C$

Operating Temperature Range .....  $-55^\circ C$  to  $+150^\circ C$

Lead Temperature (Soldering, 10 sec.) .....  $+300^\circ C$

**TO78**

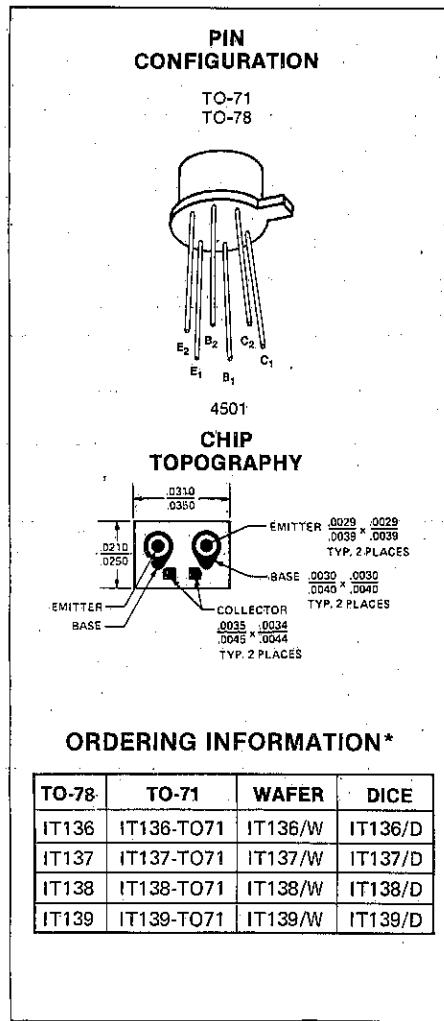
 ONE  
SIDE      BOTH  
SIDES

Power Dissipation ..... 0.4 Watt    0.75 Watt  
 Derate above  $25^\circ C$  .....  $2.3 \text{ mW}/^\circ C$   $4.3 \text{ mW}/^\circ C$

**TO71**

 ONE  
SIDE      BOTH  
SIDES

Power Dissipation ..... 0.3 Watt    0.5 Watt  
 Derate above  $25^\circ C$  .....  $1.7 \text{ mW}/^\circ C$   $2.9 \text{ mW}/^\circ C$


**ORDERING INFORMATION\***

TO-78	TO-71	WAFER	DICE
IT136	IT136-TO71	IT136/W	IT136/D
IT137	IT137-TO71	IT137/W	IT137/D
IT138	IT138-TO71	IT138/W	IT138/D
IT139	IT139-TO71	IT139/W	IT139/D

\*When ordering wafer/dice refer to Appendix B-23.

# IT136 - IT139

**INTERSIL**

## ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

1

PARAMETER	IT136		IT137		IT138		IT139		UNITS	CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$h_{FE}$	DC Current Gain	150	150	100		70				$I_C = 10 \mu A, V_{CE} = 5V$	
		150	800	150	800	100	800	70	800	$I_C = 1.0 mA, V_{CE} = 5V$	
		125		125		80		50		$I_C = 10 mA, V_{CE} = 5V$	
		65		60		40		25		$I_C = 50 mA, V_{CE} = 5V$	
	TA = 55°C	75		75		60		40		$I_C = 1 mA, V_{CE} = 5V$	
$V_{BE(on)}$	Emitter - Base On Voltage	,9		,9		,9		,9		$I_C = 10 mA, V_{CE} = 5V$	
		1.0		1.0		1.0		1.0		$I_C = 50 mA, V_{CE} = 5V$	
$V_{CE(sat)}$	Collector Saturation Voltage	.3		.3		.3		.3		$I_C = 1 mA, I_B = .1 mA$	
		.6		.6		.6		.6		$I_C = 10 mA, I_B = 1 mA$	
$I_{CBO}$	Collector Cutoff Current	0.1		0.1		0.1		0.1*	nA	$I_E = 0, V_{CB} = 45V, 30V^*$	
		TA = +150°C	0.1		0.1		0.1	0.1*	μA		
$I_{EBO}$	Emitter Cutoff Current	0.1		0.1		0.1		0.1	nA	$I_C = 0, V_{EB} = 5V$	
$C_{obo}$	Output Capacitance	3		3		3		3	pF	$I_E=0, V_{CB}=20V, f=1 MHz$	
PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{C1C2}$	Collector to Collector Breakdown Voltage	± 100		± 100		± 100		± 100			$I_C = \pm 1 \mu A$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		60		55		45			$I_C = 1 mA, I_B = 0$
$BV_{CBO}$	Collector Base Breakdown Voltage	60		60		55		45			$I_C = 10 \mu A, I_E = 0$
$BV_{EBO}$	Emitter Base Breakdown Voltage	7		7		7		7			$I_E = 10 \mu A, I_C = 0$
PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$ V_{BE_1} - V_{BE_2} $	Base Emitter Voltage Differential		1		2		3		5	mV	$I_C = 1 mA, V_{CE} = 5V$
$\Delta V_{BE_1} - V_{BE_2} /\Delta T$	Base Emitter Voltage Differential Change with Temperature		3		5		10		20	μV/°C	$I_C = 1 mA, V_{CE} = 5V$ $T_A = -55^\circ C$ to $+125^\circ C$
$ I_{B1} - I_{B2} $	Base Current Differential		2.5		5		10		20	nA	$I_C = 10 \mu A, V_{CE} = 5V$
			.25		.5		1.0		2.0	μA	$I_C = 1 mA, V_{CE} = 5V$

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA

# IT500-IT505 Monolithic Dual Cascoded N-Channel JFET

1

## FEATURES

- CMRR > 120 dB
- $I_G < 5\text{pA} @ 50\text{V}_DG$
- $C_{rss} < 0.5 \text{ pF}$
- $g_{os} > .025 \mu\text{mhos}$

## ABSOLUTE MAXIMUM RATINGS

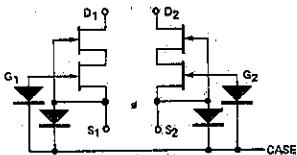
( $T_A = 25^\circ\text{C}$  unless otherwise specified)

### Drain-Source and Drain-Gate

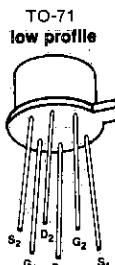
	ONE SIDE	BOTH SIDES
Power Dissipation .....	250 mW	500 mW
Derate above $25^\circ\text{C}$ .....	3.8 mW/ $^\circ\text{C}$	7.7 mW/ $^\circ\text{C}$
Drain Current (Note 1) .....	50 mA	
Gate-Gate Voltage .....	$\pm 60\text{V}$	
Storage Temperature .....	-65 $^\circ\text{C}$ to +200 $^\circ\text{C}$	
Operating Temperature .....	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$	
Lead Temperature (Soldering, 10 sec.) .....	+300 $^\circ\text{C}$	

## GENERAL DESCRIPTION

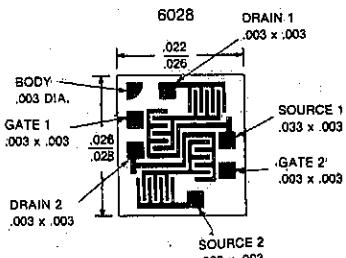
A low noise, low leakage FET that employs a cascode structure to accomplish very low  $I_G$  at high voltage levels, while giving high transconductance and very high common mode rejection ratio.



## PIN CONFIGURATION



## CHIP TOPOGRAPHY (Note 2)



## ORDERING INFORMATION\*

TO-78	WAFER	DICE
IT500	IT500/W	IT500/D
IT501	IT501/W	IT501/D
IT502	IT502/W	IT502/D
IT503	IT503/W	IT503/D
IT504	IT504/W	IT504/D
IT505	IT505/W	IT505/D

NOTE 1. Per transistor.

NOTE 2. Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.

\*When ordering wafer/dice refer to Appendix B-23.

# IT500-IT505

## ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

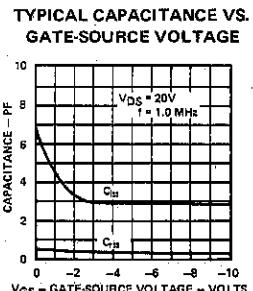
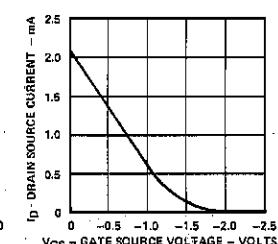
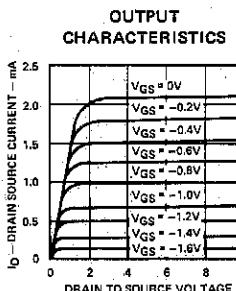
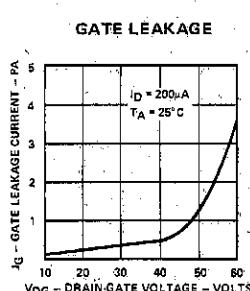
1

Symbol	Characteristics		Min	Max	Unit	Test Conditions						
I <sub>GSSR</sub>	Gate Reverse Current	T <sub>A</sub> = 125°C	-100	-5	pA	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0						
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage		-60		nA	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0						
V <sub>GS</sub> (off)	Gate-Source Cutoff Voltage		-0.7	-4	V	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1 nA						
V <sub>GS</sub>	Gate-Source Voltage		-0.2	-3.8								
I <sub>G</sub>	Gate Operating Current	T <sub>A</sub> = 125°C	-5	-5	pA	V <sub>DG</sub> = 50V, I <sub>D</sub> = 200 μA						
I <sub>DSS</sub>	Saturation Drain Current (Note 1)		0.7	7	mA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0						
g <sub>fs</sub>	Common-Source Forward Transconductance (Note 1)		1000	4000		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0						
g <sub>fs</sub>	Common-Source Forward Transconductance (Note 1)		700	1600	μmho	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200 μA	f = 1 kHz					
g <sub>os</sub>	Common-Source Output Conductance			1		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0						
g <sub>os</sub>	Common-Source Output Conductance			0.025		V <sub>DS</sub> = 20V, I <sub>D</sub> = 200 μA						
C <sub>g1g2</sub>	Gate to Gate Capacitance			3.5	pF	V <sub>G1</sub> = V <sub>G2</sub> = 10V						
C <sub>iss</sub>	Common-Source Input Capacitance			7	pF		f = 1 MHz					
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 3)			0.5		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0						
NF	Spot Noise Figure			0.5	dB		f = 100 Hz, R <sub>G</sub> = 10 MΩ					
$\bar{e}_n$		Equivalent Input Noise Voltage		0.035	$\frac{\mu V}{\sqrt{Hz}}$		f = 10 Hz					
				0.010			f = 1 kHz					
Symbol	Characteristics	IT500	IT501	IT502	IT503	IT504	IT505	Unit	Test Conditions			
I <sub>G1</sub> , I <sub>G2</sub>	Differential Gate Current			5	.5	5		10	15	nA	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200 μA + 125°C	
I <sub>DSS1</sub>	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.9	1	0.85	1	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V
I <sub>DSS2</sub>												f = 1 kHz
g <sub>fs1</sub> /g <sub>fs2</sub>	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.90	1	0.85	1	
V <sub>G1</sub> -V <sub>G2</sub>	Differential Gate-Source Voltage			5	5	10		15	25	50	mV	
ΔV <sub>G1</sub> -V <sub>G2</sub>	Gate-Source Differential Voltage			5	10	20		40	100	200	μV/°C	V <sub>DG</sub> = 20V T <sub>A</sub> = 25°C T <sub>B</sub> = 125°C I <sub>D</sub> = 200 μA
ΔT	Change with Temp. (Note 2)			5	10	20		40	100	200		T <sub>A</sub> = -55°C T <sub>B</sub> = 25°C
C <sub>MRR</sub> **	Common Mode Rejection Ratio	120	120	120	120	120	120	120	120	120	dB	ΔV <sub>DD</sub> = 10V, I <sub>D</sub> = 200 μA

\*\* C<sub>MRR</sub> = 20 log<sub>10</sub> ΔV<sub>DD</sub> / Δ(V<sub>gs1</sub> - V<sub>gs2</sub>) , ΔV<sub>DD</sub> = 10V - 20V

NOTES: 1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%. 2. Measured at end points, T<sub>A</sub> and T<sub>B</sub>.  
3. With case guarded C<sub>rss</sub> is typically < 0.15 pF.

## TYPICAL PERFORMANCE CURVES



# A050

## Using the IT500 Family to Improve the Input Bias Current of BIFET OPAMPS

1

### INTRODUCTION

The LF156 family of BIFET OPAMPS is very popular because of the combination of high slew rate (typically  $12V/\mu s$  @ unity gain) and moderate offset voltage (about 2mV). Input bias current, however, varies directly with input voltage, rising from 30pA @  $V_{IN} = -10V$ , to 50 pA @  $V_{IN} = 0V$ , and finally to 80pA @  $V_{IN} = +10V$ . This can be improved markedly by using one of the IT500 series to drive the inputs of the LF156.

The IT500, like the others in its family, is a dual cascoded n-channel JFET pair, featuring a typical input bias current of  $<1pA$  with inputs ranging from  $-15V$  to  $+15V$ ; actual  $I_G$  is guaranteed to be less than 5pA @  $V_{DG} = 50V$ .

Figure 1 shows an IT500 being used to drive the inputs of an LF156. This greatly reduces the input bias current, and in no way affects the already superior slew rate; the offset voltage is not significantly degraded because of the excellent matching of the IT500.

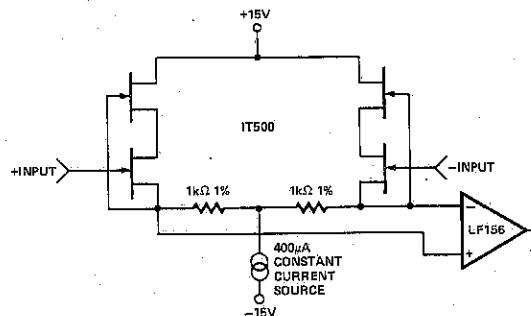


FIGURE 1. INPUT DRIVE CIRCUIT USING IT500

The constant current source can be designed with any transistor pair having a high beta @  $I_C = 400\mu A$ . See Figure 2.

An added bonus of the IT500 is its CMRR > 100dB, compared to the LF156 CMRR of 85dB.

This configuration is ideal for electrometer circuits, with good measurement accuracy down to 10pA of input current ( $< 10\%$  error with 10pA of input current). A  $10M\Omega$  glass feedback resistor connected between the -INPUT and OPAMP OUTPUT does the trick. Other possible applications include sample and hold amplifiers, instrumentation amplifiers, etc.

Although this application note has dealt solely with the LF156, all present day BIFET OPAMPS exhibit the same  $I_{BIAS}$  vs.  $V_{IN}$  dependency, and all will benefit from using the IT500 as a preamplifier.

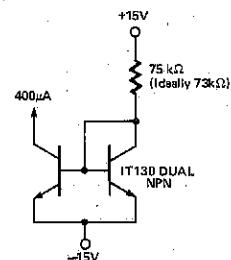


FIGURE 2. CONSTANT CURRENT SOURCE



# IT550

## Dual N-Channel JFET

1

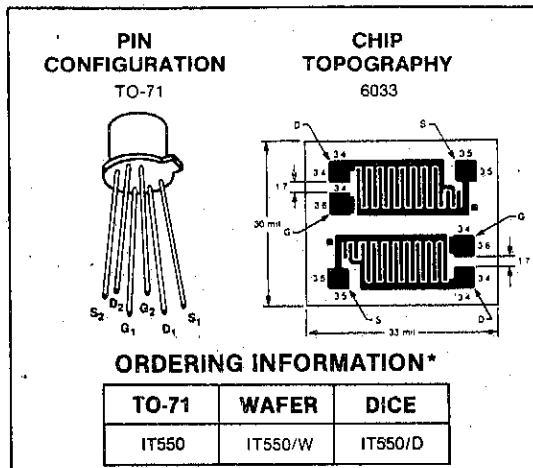
### FEATURES

- Specified Matching Characteristics
- High Gain
- Low "ON" Resistance

### ABSOLUTE MAXIMUM RATINGS

(25°C Unless otherwise noted)

Gate-Drain or Gate-Source Voltage	.....	-40V
Gate Current	.....	50 mA
Gate-Gate Voltage	.....	±60V
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	One Side	325mW
	Both Sides	650mW
Derate above 25°C	2.2mW/°C	3.3mW/°C



### ORDERING INFORMATION\*

TO-71	WAFER	DICE
IT550	IT550/W	IT550/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS

TEST CONDITIONS (25°C unless otherwise noted)

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
$I_{GSS}$	Gate-Reverse Current $T_A = 150^\circ C$	$V_{GS} = -20V, V_{DS} = 0$		-100	pA
				-200	mA
$BV_{GSS}$	Gate-Source Breakdown Voltage	$I_G = -1\mu A, V_{DS} = 0$	-40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V, I_D = 1nA$	-0.5	-3	
$V_{GS(f)}$	Gate-Source Voltage	$V_{DS} = 0V, I_G = 2mA$		1.0	
$I_{DSS}$	Saturation Drain Current (Note 1)	$V_{DS} = 15V, V_{GS} = 0$	5	30	mA
$r_{DS(on)}$	Static Drain Source ON Resistance	$I_D = 1mA, V_{GS} = 0$		100	$\Omega$
$g_{fs}$	Common-Source Forward Transconductance (Note 1)	$f = 1kHz$	7500	12,500	$\mu mho$
		$f = 100MHz$	7000		
$g_{os}$	Common-Source Output Conductance	$f = 1kHz$		45	
$C_{rss}$	Common-Source Reverse Transfer Capacitance	$V_{DG} = 15V, I_D = 2mA$ $f = 1MHz$		3	pF
$C_{iss}$	Common-Source Input Capacitance			12	
$NF$	Spot Noise Figure	$f = 10Hz, R_g = 1M$		1.0	dB
$e_n$	Equivalent Short Circuit Input Noise Voltage	$f = 10Hz$		50	$nV/\sqrt{Hz}$

SYMBOL	PARAMETERS	CONDITIONS	IT550		UNIT
			MIN.	MAX.	
$I_{DSS1}$ $I_{DSS2}$	Saturation Drain Current Ratio (Notes 1 and 2)	$V_{DS} = 15V, V_{GS} = 0$	0.95	1	—
$ V_{GS1}-V_{GS2} $	Differential Gate-Source Voltage	$V_{DS} = 15V, I_D = 2mA$ $(T_A = -55^\circ C \text{ to } +125^\circ C)$		50	mV
$\Delta  V_{GS1}-V_{GS2} $ $\Delta T$	Gate-Source Voltage Differential Drift (Note 3)			100	$\mu V/^\circ C$
$g_{fs1}$ $g_{fs2}$	Transconductance Ratio (Notes 1 and 2)	$V_{DS} = 15V, I_D = 2mA$ $f = 1kHz$	0.90	1	—

### NOTES:

1. Pulse test required; pulse width 300 $\mu s$ , duty cycle  $\leq 3\%$ .

2. Assumes smaller value in numerator

3. Measured at end points  $T_A$  and  $T_B$



# IT1700

## P-Channel Enhancement Mode MOSFET

1

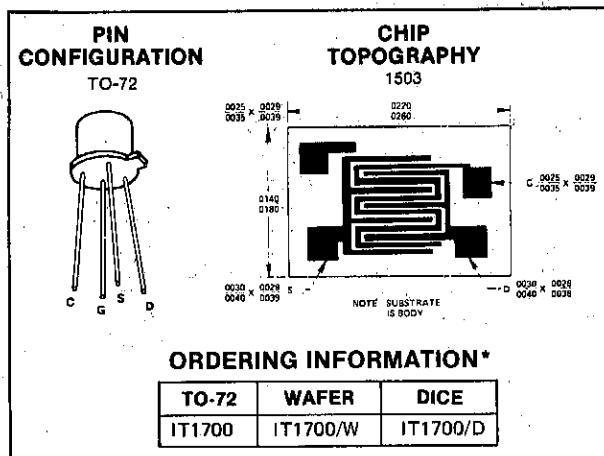
### FEATURES

- Low ON-Resistance
- High Gain
- Low Noise Voltage
- High Input Impedance
- Low Leakage

### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Drain-Source and Gate-Source Voltage .....	-40 V
Peak Gate-Source Voltage (Note 1).....	±125 V
Drain Current .....	50 mA
Storage Temperature .....	-65°C to +200°C
Operating Temperature Range ...	-55°C to +150°C
Lead Temperature (Soldering, 10 sec) .....	+300°C
Power Dissipation .....	375 mW
Derate above 25°C .....	3 mW/°C



### ORDERING INFORMATION\*

TO-72	WAFER	DICE
IT1700	IT1700/W	IT1700/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V<sub>BS</sub> = 0 unless otherwise noted.

PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS	
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	-40	V	V <sub>GS</sub> = 0, I <sub>D</sub> = -10 μA	
BV <sub>SDS</sub>	Source to Drain Breakdown Voltage	-40	V	V <sub>GS</sub> = 0, I <sub>D</sub> = -10 μA	
I <sub>GSS</sub>	Gate Leakage Current	(See note 2)			
I <sub>DSS</sub>	Drain to Source Leakage Current	200	pA	V <sub>GS</sub> = 0, V <sub>DS</sub> = -20 V	
I <sub>DSS</sub> (150°C)	Drain to Source Leakage Current	0.4	μA		
I <sub>SDS</sub>	Source to Drain Leakage Current	400	pA		
I <sub>SDS</sub> (150°C)	Source to Drain Leakage Current	0.8	μA		
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2	-5	V	
R <sub>DS(on)</sub>	Static Drain to Source "on" Resistance	400	ohms	V <sub>GS</sub> = -10 V, V <sub>DS</sub> = 0	
I <sub>DS(on)</sub>	Drain to Source "on" Current	2	mA	V <sub>GS</sub> = -10 V, V <sub>DS</sub> = -15 V	
g <sub>fs</sub>	Forward Transconductance Common Source	2000	4000	μmhos	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -10 mA f = 1 kHz
C <sub>iss</sub>	Small Signal, Short Circuit, Common Source, Input Capacitance		5	pF	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -10 mA f = 1 MHz
C <sub>rss</sub>	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance		1.2	pF	V <sub>DG</sub> = -15 V, I <sub>D</sub> = 0 f = 1 MHz
C <sub>oss</sub>	Small Signal, Short Circuit, Common Source, Output Capacitance		3.5	pF	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -10 mA f = 1 MHz

NOTES: 1. Device must not be tested at ±125V more than once nor longer than 300 ms.

2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10 pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.



IT1750

# N-Channel Enhancement Mode MOSFET

## FEATURES

- Low ON Resistance
- Low C<sub>dg</sub>
- High Gain
- Low Threshold Voltage

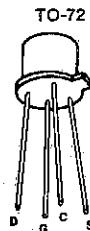
1

## ABSOLUTE MAXIMUM RATINGS

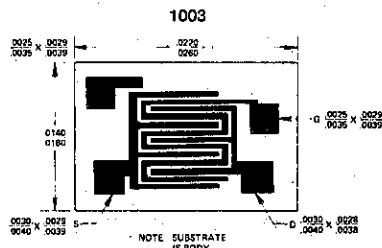
(T<sub>A</sub> = 25°C unless otherwise noted)

Drain-Source and Gate-Source Voltage	25V
Peak Gate-Source Voltage (Note 1)	±125V
Drain Current	100 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	375 mW
Derate above 25°C	3 mW/°C

## PIN CONFIGURATION



## CHIP TOPOGRAPHY



## ORDERING INFORMATION\*

TQ-72	WAFER	DICE
IT1750	IT1750/W	IT1750/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, Body connected to Source and V<sub>BS</sub> = 0 unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V <sub>G(S(th))</sub> Gate to Source Threshold Voltage	0.50	1.5	3.0	V	V <sub>DS</sub> = V <sub>G(S)</sub> , I <sub>D</sub> = 10 μA
I <sub>DSS</sub> Drain Leakage Current		0.1	10	nA	V <sub>DS</sub> = 10 V, V <sub>G(S)</sub> = 0
I <sub>IGSS</sub> Gate Leakage Current	See note 2.				
V <sub>BDSS</sub> Drain Breakdown Voltage	25			V	I <sub>D</sub> = 10 μA, V <sub>G(S)</sub> = 0
I <sub>DS(on)</sub> Drain To Source on Resistance		25	50	ohms	V <sub>G(S)</sub> = 20 V
I <sub>D(on)</sub> Drain Current	10	50		mA	V <sub>DS</sub> = V <sub>G(S)</sub> = 10 V
Y <sub>fs</sub> Forward Transadmittance	3,000			μmhos	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA, f = 1 KHz
C <sub>iss</sub> Total Gate Input Capacitance		5.0	6.0	pF	I <sub>D</sub> = 10 mA, V <sub>DS</sub> = 10 V, f = 1 MHz
C <sub>dg</sub> Gate to Drain Capacitance		1.3	1.6	pF	V <sub>DG</sub> = 10 V, f = 1 MHz

### NOTES:

1. Devices must not be tested at ±125V more than once nor longer than 300 ms.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.



# J105-J107

## N-Channel JFET

1

### FEATURES

- Low  $r_{DS(on)}$

### APPLICATIONS

- Analog Switches
- Choppers
- Commutators

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Drain or Gate-Source Voltage	.....	-25V
Gate Current	.....	50 mA
Storage Temperature Range	... -65° C to +200° C	
Operating Temperature Range	-55° C to +150° C	
Lead Temperature (Soldering, 10 sec.)	..... +300° C	
Power Dissipation	.....	360 mW
Derate above 25° C	.....	3.3 mW/°C

### PIN CONFIGURATION

TO-92



### ORDERING INFORMATION\*

J105	TO-92 only
J106	TO-92 only
J107	TO-92 only

### ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25 °C unless otherwise noted

\*When ordering wafer/dice refer to Appendix B-23.

PARAMETER	J105			J106			J107			UNIT TEST CONDITIONS
	MIN	Typ	MAX	MIN	Typ	MAX	MIN	Typ	MAX	
$I_{GSS}$	Gate-Reverse Current (Note 1)			-3			-3			-3 nA $V_{DS}=0V, V_{GS}=-15V$
$V_{GS(\text{off})}$	Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4.5 V $V_{DS}=5V, I_D=1 \mu\text{A}$
$BV_{GS}$	Gate-Source Breakdown Voltage	-25		-25			-25			-25 mA $V_{DS}=0V, I_G=-1 \mu\text{A}$
$I_{DSS}$	Drain Saturation Current (Note 2)	500		200			100			500 mA $V_{DS}=15V, V_{GS}=0V$
$I_{D(\text{off})}$	Drain Cutoff Current (Note 1)			3			3			3 nA $V_{DS}=5V, V_{GS}=-10V$
$r_{DS(\text{on})}$	Drain source ON Resistance			3			6			3 $\Omega V_{DS} \leq 0.1V, V_{GS}=0V$
$C_{gg(\text{off})}$	Drain Gate OFF Capacitance			35			35			35 pF $V_{DS}=0V, V_{GS}=-10V$
$C_{sg(\text{off})}$	Source Gate OFF Capacitance			35			35			35 pF $f=1 \text{ MHz}$
$C_{dg(\text{on})}$ + $C_{sg(\text{on})}$	Drain Gate plus Source Gate ON Capacitance			160			160			160 pF $V_{DS}=V_{GS}=0V$
$t_{d(\text{on})}$	Turn On Delay Time		15			15			15	Switching Time Test Conditions J105 J106 J107 ns ns ns
$t_r$	Rise Time		20			20			20	
$t_{d(\text{off})}$	Turn Off Delay Time		15			15			15	
$t_f$	Fall Time		20			20			20	
$V_{DD}$										1.5V 1.5V 1.5V
$V_{GS(\text{off})}$										-12V -7V -5V
$R_L$										50Ω 50Ω 50Ω

NOTES: 1. Approximately doubles for every 10 °C increase in  $T_A$ .

2. Pulse test duration = 300  $\mu\text{s}$ ; duty cycle  $\leq 3\%$ .



# INTERSIL

## J111-J113 N-Channel JFET

1

### FEATURES

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
- No Offset or Error Voltage Generated by Closed Switch
- Purely Resistive
- High Isolation Resistance from Driver
- Fast Switching
- Short Sample and Hold Aperture Time

### APPLICATIONS

- Analog Switches
- Choppers
- Commutators

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Drain or Gate-Source Voltage	.....	-35V
Gate Current	.....	50 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	310 mW
Derate Above 25°C	.....	2.8 mW/°C

PIN CONFIGURATION		CHIP TOPOGRAPHY
TO-92		5001
D	S G	<p>Pinout details: Pin 1 (D) is the Drain, Pin 2 (S) is the Source, and Pin 3 (G) is the Gate. The chip topography shows a vertical drain electrode at the top, a gate electrode with a contact area of 0123/0127, and a source electrode at the bottom with a contact area of 014/018. The drain electrode has a contact area of 019/023. The source electrode has a contact area of 0045 ± 0035 / 0035 ± 0026. The gate electrode has a contact area of 00135 FULL RADIUS / 00175. (DRAIN). A note states 'SUBSTRATE IS GATE'.</p>

### ORDERING INFORMATION\*

TO-92	WAFER	DICE
J111	J111/W	J111/D
J112	J112/W	J112/D
J113	J113/W	J113/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS

TEST CONDITIONS:  $25^\circ\text{C}$  unless otherwise noted

PARAMETERS	J111			J112			J113			TEST CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
$I_{GSS}$					-1				-1	nA
$V_{GS(off)}$	Gate Source Cutoff Voltage	-3	-10	-1	-5	-0.5	-3			V
$BV_{GSS}$	Gate Source Breakdown Voltage	-35		-35		-35				
$I_{DS(on)}$	Drain Saturation Current (Note 2)	20		5		2				mA
$I_D(0ff)$	Drain Cutoff Current (Note 1)		1		1			1		nA
$R_{DS(on)}$	Drain Source ON Resistance		30		50		100			$\Omega$
$C_{dg(off)}$	Drain Gate OFF Capacitance		5		5		5			f = 1 MHz
$C_{sg(off)}$	Source Gate OFF Capacitance		5		5		5			
$C_{dg(on)}$	Drain Gate Plus Source Gate ON Capacitance		28		28		28			
$t_{d(on)}$	Turn On Delay Time	7		7		7				
$t_r$	Rise Time	6		6		6				
$t_{d(off)}$	Turn Off Delay Time	20		20		20				
$t_f$	Fall Time	15		15		15				
Switching Time Test Conditions										
	J111	J112	J113							
$V_{DD}$	10V	10V	10V							
$V_{GS(off)}$	-12V	-7V	-5V							
$R_L$	0.8k $\Omega$	1.6k $\Omega$	3.2k $\Omega$							

### NOTES:

1. Approximately doubles for every  $10^\circ\text{C}$  increase in  $T_A$ .
2. Pulse Test duration 300 $\mu\text{s}$ ; duty cycle  $\leq 3\%$ .



# J174-J177 P-Channel JFET

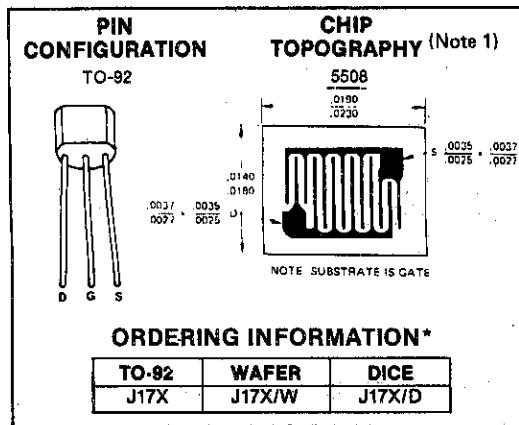
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## FEATURES

- Low Insertion Loss
- No Offset or Error Generated by Closed Switch
- Purely Resistive
- High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
- Fast Switching

## APPLICATIONS

- Analog Switches
- Choppers
- Commutators



\*When ordering wafer/dice refer to Appendix B-23.

## ABSOLUTE MAXIMUM RATINGS (TA = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1)	30V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	350 mW
Derate above 25°C	3.5 mW/°C

## ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETERS	J174		J175		J176		J177		UNIT	TEST CONDITIONS	
	MIN	Typ	MAX	MIN	Typ	MAX	MIN	Typ	MAX	Vds = 0, Vgs = 20V	
I <sub>GSSR</sub> (Note 2)			1			1			1	nA	Vds = 0, Vgs = 20V
V <sub>GSS(off)</sub> (Note 1)	5		10	3		8	1		4	0.8	50 mA
BV <sub>GSS</sub> (Note 1)	30			30			30				-65°C to +200°C
I <sub>DS</sub>	-20		-100	-7		-60	-2		-25	1.5	-55°C to +150°C
I <sub>D(off)</sub> (Note 2)			-1			-1			-1	nA	300°C
R <sub>DS(on)</sub> (Note 1)			85			125			250		350 mW
C <sub>Dg(off)</sub> (Note 1)	5.5			5.5			5.5			pF	Vds = 0, Vgs = 10V
C <sub>Sg(off)</sub> (Note 1)	5.5			5.5			5.5				Vds = 0, Ig = 1 μA
C <sub>Dg(on) + C<sub>Sg(on)</sub></sub>	40			40			40				f = 1 MHz
t <sub>d(on)</sub>	2			5			15		20	ns	Switching Time Test Conditions
t <sub>r</sub>	5			10			20		25		J174 J175 J176 J177
t <sub>d(off)</sub>	5			10			15		20		V <sub>DD</sub> -10V -6V -6V -6V
t <sub>f</sub>	10			20			20		25		V <sub>GSS(off)</sub> 12V 8V 6V 3V
										R <sub>L</sub> 560Ω 12kΩ 5.6kΩ 10kΩ	
										V <sub>GSS(on)</sub> 0V 0V 0V 0V	

## NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in TA.
3. Pulse test duration ~300μs; duty cycle ≤ 3%.



# J201-J204 N-Channel JFET

1

## FEATURES

- High Input Impedance
- Low  $I_{GSS}$

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)	
Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	360 mW
Derate above 25°C	3.3mW/°C

## ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETERS	J201			J202			J203			J204			UNIT	TEST CONDITIONS	
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
$I_{GSS}$			-100			-100			-100			-100	pA	$V_{DS} = 0, V_{GS} = -20V$	
$V_{GS(off)}$	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	-0.5		-2.0	V	$V_{DS} = 20V, I_D = 10\text{ }\mu\text{A}$	
$BV_{GSS}$	-40			-40			-40			-25				$V_{DS} = 0, I_G = -1\mu\text{A}$	
$I_{DSS}$	0.2		1.0	0.9		4.5	4.0		20		1.2		mA	$V_{DS} = 20V, V_{GS} = 0$	
$I_G$		Gate Current (Note 1)	-3.5			-3.5			-3.5		-3.5		pA	$V_{DG} = 20V, I_D = 200\mu\text{A}$	
$G_f$	500			1,000			1,500			1500					
$G_{os}$		Common-Source Forward Transconductance (Note 2)	1			3.5			10		2.5		$\mu\text{mho}$	$V_{DS} \approx 20V, V_{GS} = 0$	
$C_{iss}$		Common-Source Input Capacitance	4			4			4		4		pF	$f = 1\text{ kHz}$	
$C_{rss}$		Common-Source Reverse Transfer Capacitance	1			1			1		1			$f = 1\text{ MHz}$	
$\bar{e}_n$		Equivalent Short-Circuit Input Noise Voltage	5			5			5		10		$\frac{nV}{\sqrt{\text{Hz}}}$	$V_{DS} = 10V, V_{GS} = 0$	

NOTES: 1. Approximately doubles for every 10°C increase in TA.  
2. Pulse test duration = 2ms.

PIN CONFIGURATION	CHIP TOPOGRAPHY	
TO-92	5010*	
NOTE: SUBSTRATE IS GATE		
ORDERING INFORMATION*		
TO-92	WAFER	DICE
J201	J201/W	J201/D
J202	J202/W	J202/D
J203	J203/W	J203/D
J204	J204/W	J204/D

\*When ordering wafer/dice refer to Appendix B-23.  
\*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

PARAMETERS		J204			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
S T A T I C	$I_{GSS}$			-100	pA	$V_{DS} = 0, V_{GS} = -20V$
	$V_{GS(\text{off})}$	-0.5		-2.0	V	$V_{DS} = 20V, I_D = 10\text{nA}$
	$BV_{GSS}$	-25				$V_{DS} = 0, I_G = -\mu\text{A}$
	$I_{DSS}$		1.2		mA	$V_{DS} = 20V, V_{GS} = 0$
	$I_G$		-3.5		pA	$V_{DG} = 20V, I_D = 200\mu\text{A}$
D Y N A M I C	$g_{fs}$		1500		$\mu\text{mho}$	$V_{DS} = 20V, V_{GS} = 0$
	$g_{os}$		2.5			
	$C_{iss}$		4		pF	$f = 1\text{MHz}$
	$C_{rss}$		1			
	$e_n$		10		$\frac{\text{nV}}{\text{Hz}}$	$V_{DS} = 10V, V_{GS} = 0$



# J308-J310

## N-Channel JFET

### FEATURES

- Industry Standard Part in Low Cost Plastic Package
- High Power Gain
- Low Noise
- Dynamic Range Greater than 100 dB
- Easily Matched to  $75\Omega$  Input

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### APPLICATIONS

- VHF/UHF Amplifiers
- Oscillators
- Mixers

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ C$  unless otherwise noted)

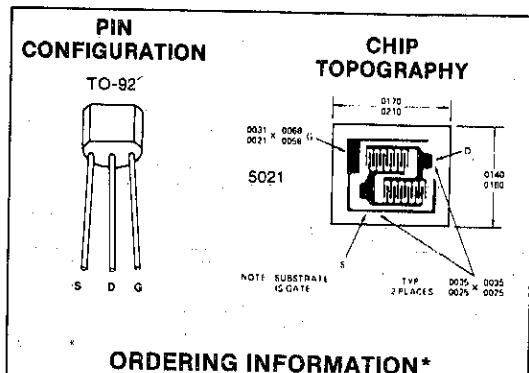
Drain-Gate Voltage	.....	-25V
Drain-Source Voltage	.....	-25V
Continuous Forward Gate Current	.....	-10 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	300 mW
Derate above 25°C	.....	1.7 mW/°C

### ELECTRICAL CHARACTERISTICS

TEST CONDITIONS:  $25^\circ C$  unless otherwise noted

PARAMETER	J308			J309			J310			UNIT	TEST CONDITIONS
	MIN	Typ	MAX	MIN	Typ	MAX	MIN	Typ	MAX		
$BV_{GSS}$ Gate-Source Breakdown Voltage	-25			-25			-25			V	$I_G = -1\mu A, V_{DS} = 0$
$IG_{SSR}$ Gate Reverse Current				-1.0			-1.0			nA	$V_{GS} = -15V, V_{DS} = 0$
$V_{GS(off)}$ Gate-Source Cutoff Voltage	$T_A = 125^\circ C$			-1.0	-6.5	-1.0	-4.0	-2.0		$\mu A$	$V_{DS} = 10V, I_D = 1nA$
$I_{DSS}$ Saturation Drain Current (Note 1)	12		60	12			30	24		mA	$V_{DS} = 10V, V_{GS} = 0$
$V_{GS(f)}$ Gate-Source Forward Voltage				1.0			1.0			V	$V_{DS} = 0, I_G = 1\text{ mA}$
$g_{fs}$ Common-Source Forward Transconductance	8,000		20,000	10,000			20,000	8,000		18,000	
$g_{os}$ Common-Source Output Conductance			200				200			200	
$g_{fg}$ Common-Gate Forward Transconductance		13,000			13,000			12,000		$\mu\text{hos}$	$V_{DS} = 10V, I_D = 10\text{ mA}$
$g_{og}$ Common Gate Output Conductance		150			150			150			f = 1 kHz
$C_{gd}$ Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5		
$C_{gs}$ Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0	pF	$V_{DS} = 0, V_{GS} = -10V$
$e_n$ Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{\text{Hz}}}$	$f = 1\text{ MHz}$
$R_{e(vfs)}$ Common-Source Forward Transconductance		12			12			12			$f = 100\text{ Hz}$
$R_{e(vfg)}$ Common-Gate Input Conductance		14			14			14			
$R_{e(vsi)}$ Common-Source Input Conductance		0.4			0.4			0.4		mmho	
$R_{e(vos)}$ Common-Source Output Conductance		0.15			0.15			0.15			$f = 105\text{ MHz}$
$G_{pg}$ Common-Gate Power Gain at Noise Match		16			16			16			
$INF$ Noise Figure		1.5			1.5			1.5			
$G_{pg}$ Common-Gate Power Gain at Noise Match		11			11			11			
$NF$ Noise Figure		2.7			2.7			2.7			$f = 450\text{ MHz}$

NOTE: 1. Pulse test PW 300  $\mu\text{s}$ , duty cycle  $\leq 3\%$ .



### ORDERING INFORMATION\*

TO-92	WAFER	DICE
J30X	J30X/W	J30X/D

\*When ordering wafer/dice refer to Appendix B-23.



# LM114/H, LM114A/AH Monolithic Dual NPN Transistor

1

## GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability.

Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 300MHz with 1mA collector current and 5V collector-base voltage and 22MHz with 10μA collector current. Typical collector-base capacitance is only 1.6 pF at 5V.

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Collector-Base Voltage (1)	45V
Collector-Emitter Voltage (1)	45V
Collector-Collector Voltage	45V
Emitter-Base Voltage (1)	6V
Collector Current (1)	20mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	800mW
Derate above 25°C	14mW/W

## ELECTRICAL CHARACTERISTICS (Note 2)

## FEATURES

- Low offset voltage
- Low drift
- High current gain
- Tight beta match
- High breakdown voltage
- Matching guaranteed over a 0V to 45V collector-base voltage range
- CMRR > 100 dB

PIN CONFIGURATION		CHIP TOPOGRAPHY	
TO-71 TO-78		4003	
TO-71	TO-78	COLLECTOR #1 TYP. 2 PLACES. 0.045" .0045" 0.035" .0035"	ISOLATION 0.025" .0025"
		BASE #2 TYP. 2 PLACES. 0.040" .0040" 0.030" .0030" DIAMETER.	
		EMITTER #1 TYP. 2 PLACES .0030	DIAMETER
ORDERING INFORMATION*			
TO-71	TO-78	WAFER	DICE
LM114	LM114H	LM114/W	LM114/D
LM114A	LM114AH		

\*When ordering wafer/dice refer to Appendix B-23.

PARAMETER	MAXIMUM LIMITS		UNITS	CONDITIONS
	LM114A, AH	LM114, H		
Offset Voltage	0.5	2.0	mV	1μA ≤ IC ≤ 100μA
Offset Current	2.0	10	nA	IC = 10μA
Bias Current	0.5			IC = 1μA
	20	40	nA	IC = 10μA
	3.0			IC = 1μA
Offset Voltage Change	0.2	1.5	mV	0V ≤ VCB ≤ VMAX, IC = 10μA
Offset Current Change	1.0	4.0	nA	
Offset Voltage Drift	2.0	10	μV/°C	
Offset Current	12	50		-55°C ≤ TA ≤ +125°, IC = 10μA
Bias Current	60	150	nA	
Collector-Base Leakage Current	10	50	pA	VCB = VMAX
TA = 125°C	10	50	nA	
Collector-Emitter Leakage Current	50	200	pA	VCE = VMAX, VEB = 0V
TA = 125°C	50	200	nA	
Collector-Collector Leakage Current	100	300	pA	VCC = VMAX
TA = 125°C	100	300	nA	

Note 1: Per transistor.

Note 2: These specifications apply for TA = +25°C and 0V ≤ VCB ≤ VMAX, unless otherwise specified. For the LM114 and LM114A, VMAX = 30V.



M116

# Diode Protected N-Channel Enhancement Mode MOSFET

## FEATURES

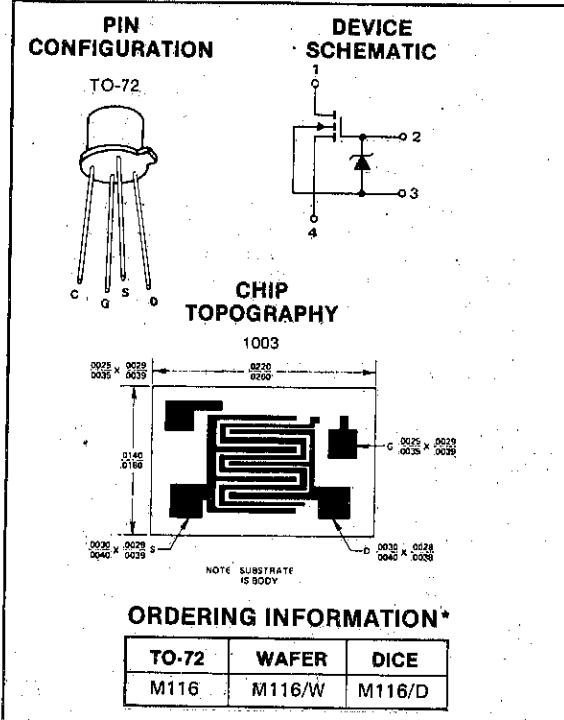
- Low  $I_{GSS}$
- Integrated Zener Clamp for Gate Protection

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## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Drain to Source Voltage	30V
Gate to Drain Voltage	30V
Drain Current	50 mA
Gate Zener Current	$\pm 0.1$ mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	2.2 mW/°C



## ORDERING INFORMATION\*

TO-72	WAFER	DICE
M116	M116/W	M116/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		M116		UNITS	TEST CONDITIONS
		MIN	MAX		
r <sub>DS(on)</sub>	Drain Source ON Resistance	100	200	Ω	V <sub>GS</sub> = 20 V, I <sub>D</sub> = 100 μA, V <sub>BS</sub> = 0 V <sub>GS</sub> = 10 V, I <sub>D</sub> = 100 μA, V <sub>BS</sub> = 0
V <sub>GS(th)</sub>	Gate Threshold Voltage	1	5		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 10 μA, V <sub>BS</sub> = 0
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	30		V	I <sub>D</sub> = 1 μA, V <sub>GS</sub> = V <sub>BS</sub> = 0
BV <sub>SDS</sub>	Source-Drain Breakdown Voltage	30			I <sub>S</sub> = 1 μA, V <sub>GD</sub> = V <sub>BD</sub> = 0
BV <sub>GDS</sub>	Gate-Body Breakdown Voltage	30	60		I <sub>G</sub> = 10 μA, V <sub>SB</sub> = V <sub>DB</sub> = 0
I <sub>D(OFF)</sub>	Drain Cutoff Current		10	nA	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = V <sub>BS</sub> = 0
I <sub>S(OFF)</sub>	Source Cutoff Current		10		V <sub>SD</sub> = 20 V, V <sub>GD</sub> = V <sub>BD</sub> = 0
I <sub>GSS</sub>	Gate-Body Leakage		100	pA	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = V <sub>BS</sub> = 0
C <sub>gs</sub>	Gate-Source		2.5		V <sub>GB</sub> = V <sub>DB</sub> = V <sub>SB</sub> = 0, f = 1 MHz Body Guarded
C <sub>gd</sub>	Gate-Drain Capacitance		2.5		V <sub>GB</sub> = 0, V <sub>DB</sub> = 10 V, f = 1 MHz
C <sub>db</sub>	Drain-Body Capacitance		7	pF	V <sub>GB</sub> = 0, V <sub>DB</sub> = 10 V, f = 1 MHz
C <sub>iss</sub>	Input Capacitance		10		V <sub>GB</sub> = 0, V <sub>DB</sub> = 10 V, V <sub>BS</sub> = 0 f = 1 MHz



# U200-U202

## N-Channel JFET

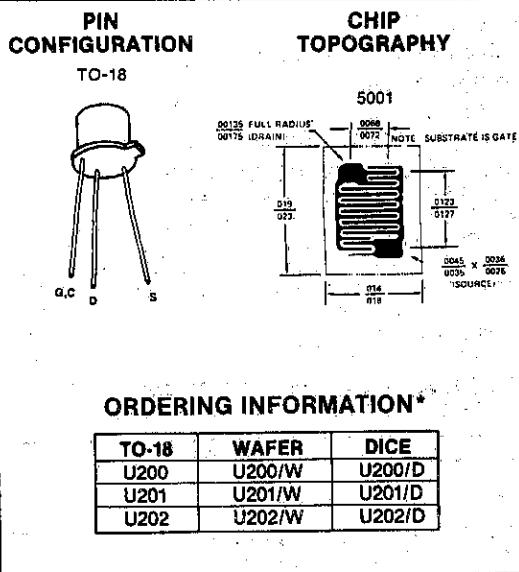
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### FEATURES

- Low Insertion Loss
- Good OFF Isolation

### APPLICATIONS

- Analog Switches
- Commutators
- Choppers



### ORDERING INFORMATION\*

TO-18	WAFER	DICE
U200	U200/W	U200/D
U201	U201/W	U201/D
U202	U202/W	U202/D

\*When ordering wafer/dice refer to Appendix B-23.

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	.....	-30V
Gate Current	.....	50 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	.....	+300°C
Total Device Dissipation	.....	1.8W
Derate above 25°C	.....	10 mW/°C

### ELECTRICAL CHARACTERISTICS ( $25^\circ C$ unless otherwise noted)

Parameter		U200		U201		U202		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
I <sub>GSS</sub>	Gate Reverse Current $T_A = 150^\circ C$	-1	-1	-1	-1	-1	-1	nA	V <sub>GSS</sub> = 20 V, V <sub>DS</sub> = 0
		-1	-1	-1	-1	-1	-1	μA	
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-30	-30	-30	-30	-30	-30	V	I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0
		-30	-30	-30	-30	-30	-30	V	
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	-0.5	-3	-1.5	-5	-3.5	-10	V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 10 nA
		-0.5	-3	-1.5	-5	-3.5	-10	V	
I <sub>D(off)</sub>	Drain Cutoff Current $T_A = 150^\circ C$	1	1	1	1	1	1	nA	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = -12 V
		1	1	1	1	1	1	μA	
I <sub>DSS</sub>	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0
R <sub>ds(on)</sub>	Drain-Source ON Resistance		150		75		50	ohm	V <sub>GS</sub> = 0, I <sub>D</sub> = 0
C <sub>iss</sub>	Common-Source Input Capacitance (Note 1)		30		30		30	pF	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0
C <sub>rss</sub>	Common Source Reverse Transfer Capacitance		8		8		8	pF	V <sub>DS</sub> = 0, V <sub>GS</sub> = -12 V

NOTE 1: Pulse test required, pulselwidth = 300 μsec, duty cycle ≤ 3%.



INTERSIL

U231-U235

Monolithic Dual N-Channel JFET

**FEATURES**

- Good Matching Characteristics

**APPLICATIONS**

- Differential Amplifiers
- Low and Maximum Frequency Amplifiers

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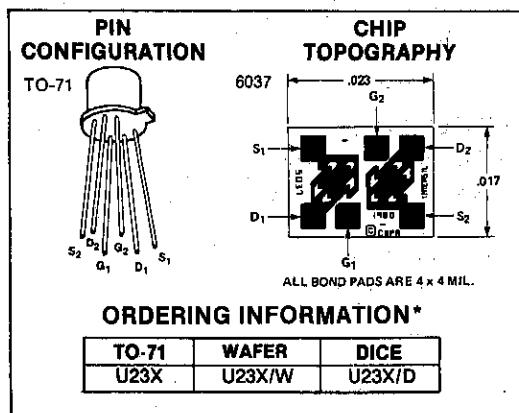
**ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	.....	-50V
Gate Current (Note 1)	.....	50 mA
Storage Temperature Range	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Load Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	300 mW
Derate above 25°C	.....	1.7 mW/°C

**ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted.

**ORDERING INFORMATION\***

TO-71	WAFER	DICE
U23X	U23X/W	U23X/D

\*When ordering wafer/dice refer to Appendix B-23.

Parameter		Min	Max	Unit	Test Conditions	
IGSSR	Gate-Reverse Current		-100	pA	VGS = -30V, VDS = 0	TA = 150°C
			-500	nA		
BVGSS	Gate-Source Breakdown Voltage	-50			IG = 1μA, VDS = 0	f = 1 kHz
	Gate-Source Cutoff Voltage	-0.5	-4.5	V		
VGS	Gate-Source Voltage	-0.3	-4.0		VDS = 20V, ID = 1 nA	f = 100 MHz
			-50	pA		
IG	Gate Operating Current		-250	nA	VDG = 20V, ID = 200μA	TA = 125°C
			0.5	5.0		
IDSS	Saturation Drain Current (Note 2)	1000	3000		VDS = 20V, VGS = 0	f = 1 kHz
		1000		μmho		
gfs	Common-Source Forward Transconductance (Note 1)	600	1600		VDS = 20V, VGS = 0	f = 100 MHz
	Common-Source Forward Transconductance (Note 1)	35		μmho		
gos	Common-Source Output Capacitance		10		VDG = 20V, ID = 200μA	f = 1 kHz
	Common-Source Output Conductance		6	pF		
Crss	Common-Source Reverse Transfer Capacitance		2		VDS = 20V, VGS = 0	f = 1 MHz
			80	nV/√Hz		
En	Equivalent Short Circuit Input Noise Voltage				f = 100 Hz	

Matching Characteristics		U231	U232	U233	U234	U235	Unit	Test Conditions	
(Ig1-Ig2)	Differential Gate Current	10	10	10	10	10	nA	VDG = 20V, ID = 200μA	125°C
(Idss1-Idss2)	Saturation Drain Current Match (Note 2)	5	5	5	10	15	%	VDS = 20V, VGS = 0	
Vgs1-Vgs2	Differential Gate-Source Voltage	5	10	15	20	25	mV		
Δ Vgs1-Vgs2	Gate-Source Voltage Differential Drift (Note 3)	10	25	50	75	100	μV/°C	TA = 25°C	TB = 125°C
		10	25	50	75	100			
(gfs1-gfs2)	Transconductance Match (Note 2)	3	5	5	10	15	%	TA = -55°C	TB = 25°C
gfs1	Differential Output Conductance	5	5	5	5	5	μmho		
gos1-gos2								f = 1 kHz	

**NOTES:**

1. Per transistor.
2. Pulse test required, pulse width = .300 μs, duty cycle ≤ 3%.
3. Measured at end points, TA and TB.



# U257

## Monolithic Dual N-Channel JFET

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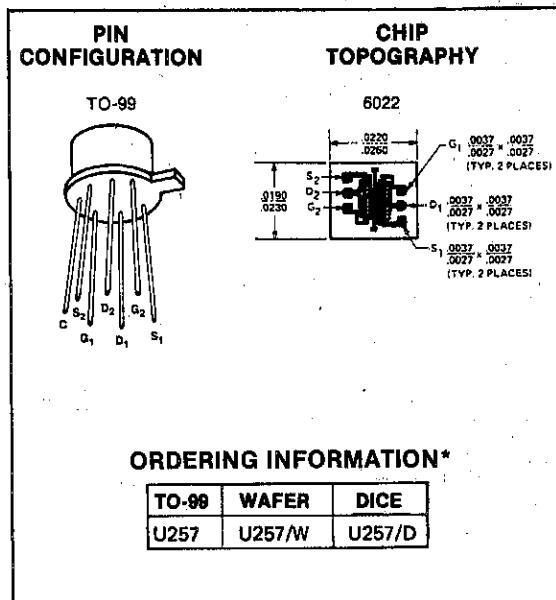
### FEATURES

- $g_{fs} > 5000 \mu\text{mho}$  from DC to 100 MHz
- Matched  $V_{GS}$ ,  $g_{fs}$  and  $g_{os}$

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above $25^\circ\text{C}$	3.8 mW/ $^\circ\text{C}$	7.7 mW/ $^\circ\text{C}$



### ORDERING INFORMATION\*

TO-99	WAFER	DICE
U257	U257/W	U257/D

\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ\text{C}$ unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
I <sub>GSSR</sub>	Gate Reverse Current	-100	pA		$V_{GS} = 15 \text{ V}$ , $V_{DS} = 0$
		-TA = 150°C	-250	nA	
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-25		V	$I_G = -1 \mu\text{A}$ , $V_{DS} = 0$
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	-1	-5		$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
I <sub>DSS</sub>	Saturation Drain Current (Note 2)	5	40	mA	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$
g <sub>fs</sub>	Common-Source Forward Transconductance	5000	10,000	$\mu\text{mho}$	$V_{DS} = 10 \text{ V}$ , $I_D = 5 \text{ mA}$ f = 1 kHz
g <sub>fs</sub>	Common-Source Forward Transconductance	5000	10,000		$V_{DG} = 10 \text{ V}$ , $I_D = 5 \text{ mA}$ f = 100 MHz
g <sub>os</sub>	Common-Source Output Conductance		150		$V_{DS} = 10 \text{ V}$ , $I_D = 5 \text{ mA}$ f = 1 kHz
g <sub>oss</sub>	Common-Source Output Conductance		150		f = 100 MHz
C <sub>iss</sub>	Common-Source Input Capacitance		5	pF	$V_{DG} = 10 \text{ V}$ , $I_D = 5 \text{ mA}$ f = 1 MHz
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance		1.2	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	f = 10 kHz
E <sub>n</sub>	Equivalent Input Noise Voltage		30		
I <sub>DSS1</sub>	Drain Current Ratio at Zero Gate Voltage (Note 2)	0.85	1		$V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$
I <sub>DSS2</sub>					
V <sub>GS1</sub> -V <sub>GS2</sub>	Differential Gate-Source Voltage		100	mV	
g <sub>f1</sub>	Transconductance Ratio	0.85	1		
g <sub>f2</sub>					
g <sub>os1</sub> -g <sub>os2</sub>	Differential Output Conductance		20	$\mu\text{mho}$	

#### NOTES:

1. Per transistor.
2. Pulse test required, pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 3\%$ .

### FEATURES

- Low ON Resistance
- $I_D(\text{off}) < 500 \mu\text{A}$
- Switches directly from T<sup>2</sup>L Logic (U306)

# 1

### APPLICATIONS

- Analog Switches
- Commutators
- Choppers

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

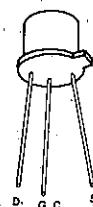
Gate-Drain or Gate-Source Voltage (Note 1)	30V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	350 mW
Derate above 25°C	2.8 mW/°C

### ELECTRICAL CHARACTERISTICS

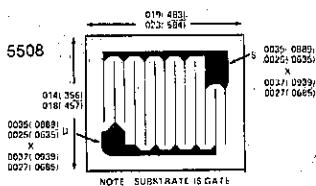
TEST CONDITIONS:  $25^\circ\text{C}$  unless otherwise noted.

### PIN CONFIGURATION

TO-18



### CHIP TOPOGRAPHY (Note 1)



NOTE: SUBSTRATE IS GATE

### ORDERING INFORMATION\*

TO-18	WAFER	DICE
U304	U304/W	U304/D
U305	U305/W	U305/D
U306	U306/W	U306/D

\*When ordering wafer/dice refer to Appendix B-23.

Parameter		U304		U305		U306		Unit	Test Conditions		
I <sub>GSSR</sub>	Gate Reverse Current		500		500		500	pA	$V_{GS} = 20\text{V}, V_{DS} = 0$		
	TA = 150°C		1.0		1.0		1.0	μA	$I_G = 1 \mu\text{A}, V_{DS} = 0$		
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	30		30		30			$V_{DS} = -15\text{V}, I_D = -1 \mu\text{A}$		
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	5	10	3	6	1	4		$V_{GS} = 0, I_D = -15\text{mA} (\text{U304}),$ $I_D = -7\text{mA} (\text{U305}),$ $I_D = -3\text{mA} (\text{U306})$		
V <sub>DS(on)</sub>	Drain-Source ON Voltage			-1.3		-0.8		-0.6	$V_{DS} = -15\text{V}, V_{GS} = 0$		
I <sub>DSS</sub>	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	$V_{DS} = -15\text{V}, V_{GS} = 12\text{V} (\text{U304})$ $V_{GS} = 7\text{V} (\text{U305})$ $V_{GS} = 5\text{V} (\text{U306})$		
I <sub>D(off)</sub>	Drain Cutoff Current			-500		-500		-500	pA	$V_{GS} = 0\text{V}, I_D = -1\text{mA}$	
f <sub>D(on)</sub>	Static Drain-Source ON Resistance			85		110		175	Ω	$V_{GS} = 0\text{V}, I_D = 0$	
f <sub>D(on)</sub>	Drain-Source ON Resistance			85		110		175	Ω	$f = 1\text{ kHz}$	
C <sub>iss</sub>	Common-Source Input Capacitance			27		27		27	pF	$V_{DS} = -15\text{V}, V_{GS} = 0$	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance			7		7		7		$V_{DS} = 0, V_{GS} = 12\text{V} (\text{U304})$ $V_{GS} = 7\text{V} (\text{U305})$ $V_{GS} = 5\text{V} (\text{U306})$	
t <sub>d(on)</sub>	Turn-ON Delay Time			20		25		25		$f = 1\text{ MHz}$	
t <sub>r</sub>	Rise Time			15		25		35	ns	$V_{DD} = -10\text{V}, -6\text{V}, -6\text{V}$	
t <sub>d(off)</sub>	Turn-OFF Delay Time			10		15		20		$V_{GS(off)} = 12\text{V}, 7\text{V}, 5\text{V}$	
t <sub>f</sub>	Fall Time			25		40		60		$R_L = 580\Omega, 743\Omega, 1800\Omega$	
										$V_{GS(on)} = 0, 0, 0$	
										$I_D(on) = -15\text{mA}, -7\text{mA}, -3\text{mA}$	

### NOTES:

1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsedwidth = 300μs, duty cycle ≤ 3%.



# U308-U310

## N-Channel JFET

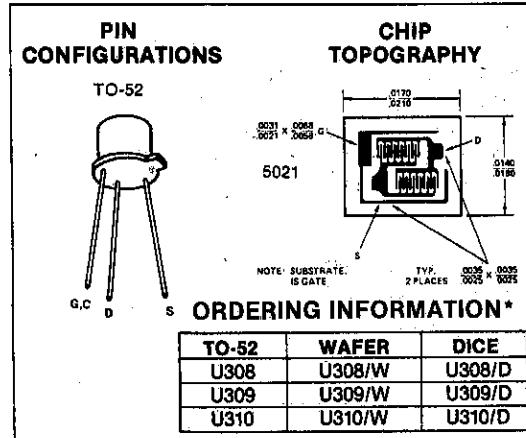
### FEATURES

- Industry Standard Part in Low Cost Plastic Package
- High Power Gain
- Low Noise
- Dynamic Range Greater than 100 dB
- Easily Matched to  $75\Omega$  Input

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ C$  unless otherwise noted)

Gate-Drain or Gate-Source Voltage	.....	-25V
Gate Current	.....	20 mA
Storage Temperature	.....	-65°C to +200°C
Operating Temperature Range	.....	-55°C to +150°C
Led Temperature (Soldering, 10 sec.)	.....	+300°C
Power Dissipation	.....	500 mW
Derate above 25°C	.....	4mW/ $^{\circ}C$



\*When ordering wafer/dice refer to Appendix B-23.

### ELECTRICAL CHARACTERISTICS ( $25^\circ C$ unless otherwise noted)

SYMBOL	PARAMETER	U308			U309			U310			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$I_{GSSR}$	Gate Reverse Current $T_A = 125^\circ C$			-150			-150			-150	pA	$V_{GS} = -15 V$
				-150			-150			-150	nA	$V_{GS} = 0$
$BV_{GSS}$	Gate-Source Breakdown Voltage	-25			-25			-25			V	$I_G = -1 \mu A, V_{DS} = 0$
												$V_{DS} = 10 V, I_D = 1 nA$
$I_{DSS}$	Saturation Drain-Current (Note 1)	12		60	12		30	24		60	mA	$V_{DS} = 10 V, V_{GS} = 0$
$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	$I_G = 10 mA, V_{DS} = 0$
$g_{fg}$	Common-Gate Forward Transconductance (Note 1)	10		20	10		20	10		18	mmho	$V_{DS} = 10 V, I_D = 10 mA$
												$f = 1 kHz$
$g_{ogs}$	Common-Gate Output Conductance			150			150			150	$\mu mho$	
$C_{gd}$	Drain-Gate Capacitance			2.5			2.5			2.5	pF	$V_{GS} = -10 V, V_{DS} = 10 V$
												$f = 1 MHz$
$C_{gs}$	Gate-Source Capacitance			5.0			5.0			5.0		
$e_n$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10 V, I_D = 10 mA$
												$f = 100 Hz$
$g_{fg}$	Common-Gate Forward Transconductance		15			15			15			$f = 100 MHz$
				14			14			14		$f = 450 MHz$
$g_{ogs}$	Common-Gate Output Conductance		0.18			0.18			0.18			$f = 100 MHz$
				0.32			0.32			0.32		$f = 450 MHz$
$G_{pg}$	Common-Gate Power Gain		16			16			16			$f = 100 MHz$
				11			11			11		$f = 450 MHz$
$NF$	Noise Figure		1.5			1.5			1.5			$f = 100 MHz$
				2.7			2.7			2.7		$f = 450 MHz$

NOTE: Pulse test duration = 2 ms.

# U401-U406

## Monolithic Dual N-Channel JFET

### FEATURES

- Minimum System Error and Calibration
- Low Drift with Temperature
- Operates from Low Power Supply Voltages
- High Output Impedance

1

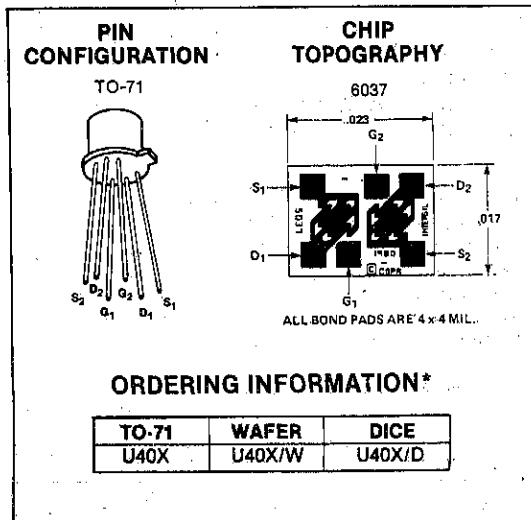
### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)	
Gate-Drain or Gate-Source Voltage (Note 1)	50V
Gate Current (Note 1)	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	300 mW	500 mW
Derate above 25°C	2.6 mW/°C	5 mW/°C

### ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25° unless otherwise noted.



\*When ordering wafer/dice refer to Appendix B-23.

Parameters		U401	U402	U403	U404	U405	U406	Unit	Test Conditions	
		Min	Max	Min	Max	Min	Max	Min	Max	
BVGSS	Gate-Source Breakdown Voltage	-50	-50	-60	-50	-50	-50	-50	V	
IGSS	Gate Reverse Current (Note 2)	-25	-25	-25	-25	-25	-25	-25	pA	
VGS(off)	Gate-Source Cutoff Voltage	-5	-2.5	-5	-2.5	-5	-2.5	-5	V	
VGS(on)	Gate-Source Voltage (on)	-2.3	-2.3	-2.3	-2.3	-2.3	-2.3	-2.3	V	
IDSS	Saturation Drain Current (Note 3)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA
IG	Operating Gate Current (Note 2) TA = 125°C	-15	-15	-15	-15	-15	-15	-15	pA	
BVG1-G2	Gate-Gate Breakdown Voltage	±50	±50	±50	±50	±50	±50	±50	V	
gfs	Common-Source Forward Transconductance (Note 3)	2000	7000	2000	7000	2000	7000	2000	7000	
gos	Common-Source Output Conductance	20	20	20	20	20	20	20	μmho	
gfs	Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	
gos	Common-Source Output Conductance	2.0	2.0	2.0	2.0	2.0	2.0	2.0	μmho	
Ciss	Common-Source Input Capacitance	8.0	8.0	8.0	8.0	8.0	8.0	8.0	pF	
Crss	Common-Source Reverse Transfer Capacitance	3.0	3.0	3.0	3.0	3.0	3.0	3.0	pF	
en	Equivalent Short-Circuit Input Noise Voltage	20	20	20	20	20	20	20	nV/√Hz	
CMRR	Common-Mode Rejection Ratio (Note 4)	95	95	95	95	90			dB	
Vgs1-Vgs2	Differential Gate-Source Voltage	5	10	10	15	20	40	40	mV	
Δ(Vgs1-Vgs2)	Gate-Source Voltage Differential Drift (Note 5)	10	10	25	25	40	80	80	μV/°C	
ΔT									T <sub>A</sub> = -55°C, T <sub>B</sub> = +25°C, I <sub>D</sub> = 200μA, T <sub>C</sub> = +125°C	

### NOTES:

1. Per transistor.
2. Approximately doubles for every 10°C increase in T<sub>A</sub>.
3. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
4. Measured at end points, T<sub>A</sub> and T<sub>B</sub>.

$$5. \text{ CMRR} = 20 \log_{10} \left[ \frac{\Delta VDD}{\Delta |Vgs_1 - Vgs_2|} \right], \Delta VDD = 10 \text{ V.}$$

**FEATURES**

- Low Insertion Loss
- No Error or Offset Voltage Generated by Closed Switch

**APPLICATIONS**

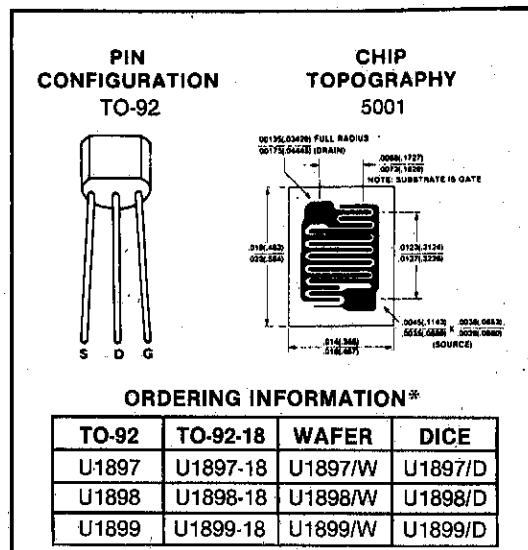
Analog Switches, Choppers

**ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)	
Gate-Drain or Gate-Source Voltage	-40V
Forward Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	350 mW
Derate above 25°C	3.5 mW/°C

**ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted



\*When ordering wafer/dice refer to Appendix B-23.

PARAMETERS	U1897		U1898		U1899		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX		IG = -1μA, VDS = 0	VGS = -20V, VDS = 0
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-40	-40	-40	-40	-40	V	VGS = -20V, VDS = 0	VGS = -20V, VDS = 0
I <sub>GSSR</sub>	Gate Reverse Current	-400	-400	-400	-400	-400	pA	V <sub>DG</sub> = 20V, I <sub>S</sub> = 0	V <sub>DG</sub> = 20V, I <sub>D</sub> = 0
I <sub>DGO</sub>	Drain-Gate Leakage Current	200	200	200	200	200		V <sub>SG</sub> = 20V, I <sub>D</sub> = 0	V <sub>DS</sub> = 20V, V <sub>GS</sub> = -12V (U1897)
I <sub>SGO</sub>	Source-Gate Leakage Current	200	200	200	200	200		V <sub>DS</sub> = 20V, V <sub>GS</sub> = -8V (U1898) V <sub>GS</sub> = -6V (U1899)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = -8V (U1898) V <sub>GS</sub> = -6V (U1899)
I <sub>D(off)</sub>	Drain Cutoff Current	200	200	200	200	200	nA	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1 nA	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1 nA
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	-5.0	-10	-2.0	-7.0	-1.0	-6.0	V	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1 nA
I <sub>DSS</sub>	Saturation Drain Current (Note 1)	30		15		8.0	mA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0
V <sub>DS(on)</sub>	Drain-Source ON Voltage		0.2		0.2		V	V <sub>GS</sub> = 0, I <sub>D</sub> = 6.6mA (U1897)	I <sub>D</sub> = 4.0mA (U1898) I <sub>D</sub> = 2.5mA (U1899)
I <sub>DS(on)</sub>	Static Drain-Source ON Resistance		30		50		Ω	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0
C <sub>DG</sub>	Drain-Gate Capacitance		5		5		pF	V <sub>DG</sub> = 20V, I <sub>S</sub> = 0	
C <sub>SG</sub>	Source-Gate Capacitance		5		5			V <sub>SG</sub> = 20V, I <sub>D</sub> = 0	
C <sub>iss</sub>	Common-Source Input Capacitance		16		16			V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	f = 1 MHz
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance		3.5		3.5				
t <sub>d(on)</sub>	Turn ON Delay Time		15		15		ns	Switching Time Test Conditions	
t <sub>r</sub>	Rise Time		10		20			U1897	U1898
t <sub>off</sub>	Turn OFF Time		40		60			V <sub>DD</sub>	V <sub>DD</sub>
								0	0
								-12V	-8V
								425Ω	770Ω
								6.6mA	4mA
									2.5mA

NOTE: 1. Pulse test pulselwidth = 300 μs; duty cycle &lt; 3%



# VCR2N/3P/4N/7N Voltage Controlled Resistors

## APPLICATIONS

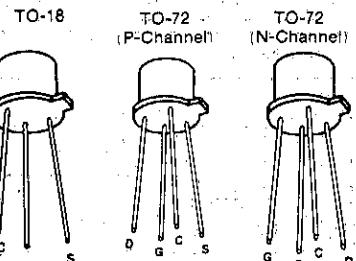
- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

1

## ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)	
Gate-Drain or Gate-Source Voltage	15V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	2 mW/°C

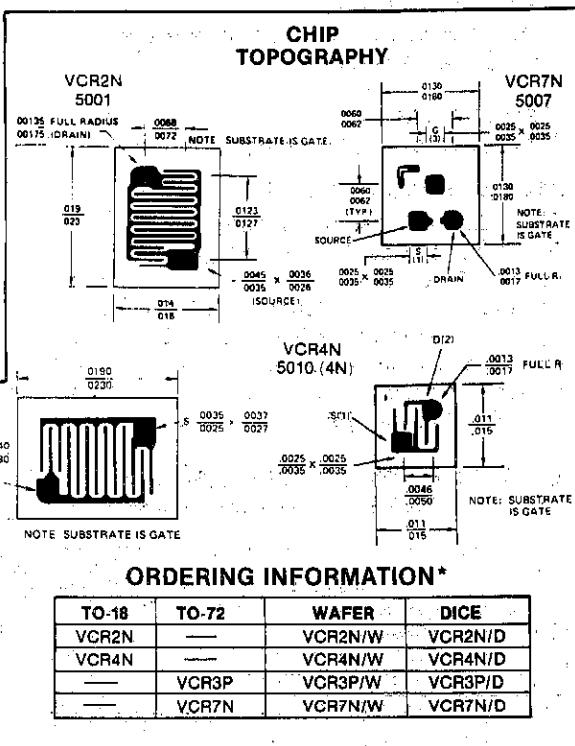
## PIN CONFIGURATIONS



VCR3P  
5508

VCR4N  
5010.(4N)

VCR7N  
5007



## ORDERING INFORMATION\*

TO-18	TO-72	WAFER	DICE
VCR2N	—	VCR2N/W	VCR2N/D
VCR4N	—	VCR4N/W	VCR4N/D
—	VCR3P	VCR3P/W	VCR3P/D
—	VCR7N	VCR7N/W	VCR7N/D

\*When ordering wafer/dice refer to Appendix B-23.

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

### N-Channel VCR FETs

Parameter	VCR2N		VCR4N		VCR7N		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max			
I <sub>GSS</sub>	Gate Reverse Current	-5	-	-0.2	-	-0.1	nA	V <sub>GS</sub> = -15V, V <sub>DS</sub> = 0	
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-15	-	-15	-	-15	-	I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0	
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	-3.5	-7	-3.5	-7	-2.5	-5	I <sub>D</sub> = 1 μA, V <sub>DS</sub> = 10V	
R <sub>dson</sub>	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V <sub>GS</sub> = 0, I <sub>D</sub> = 0
C <sub>dg0</sub>	Drain-Gate Capacitance	—	7.5	—	3	—	1.5	pF	V <sub>GD</sub> = -10V, I <sub>S</sub> = 0
C <sub>sg0</sub>	Source-Gate Capacitance	—	7.5	—	3	—	1.5	pF	V <sub>GS</sub> = -10V, I <sub>D</sub> = 0

### P-Channel VCR FETs

Parameter	VCR3P		Unit		Test Conditions
	Min	Max	V	Ω	
I <sub>GSS</sub>	Gate Reverse Current	—	20	nA	V <sub>GS</sub> = 15V, V <sub>DS</sub> = 0
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	15	—	—	I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	3.5	7	—	I <sub>D</sub> = -1 μA, V <sub>DS</sub> = -10V
R <sub>dson</sub>	Drain-Source ON Resistance	70	200	Ω	V <sub>GS</sub> = 0, I <sub>D</sub> = 0
C <sub>dg0</sub>	Drain-Gate Capacitance	—	6	pF	V <sub>GD</sub> = 10V, I <sub>S</sub> = 0
C <sub>sg0</sub>	Source-Gate Capacitance	—	6	pF	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0

## JFETS AS VOLTAGE CONTROLLED RESISTORS

The voltage controlled resistor is a junction field effect transistor whose drain to source ON resistance is controlled by gate to source voltage.

The gate control terminal is high impedance thereby allowing negligible control current. The gate voltage is zero for minimum resistance, and increases as the gate voltage approaches the pinch-off voltage.

This VCR is intended for use on applications using low level AC signals. Figure 1 shows the output characteristics, with an enlarged graph of  $V_{DS} = 0$  for AC signals with no DC component. Operation is in the first and third quadrants; the device will operate in the first quadrant only if a constant current is applied to the drain and the input signal level is kept low.

Figure 1 also shows that certain combinations of gate control voltage and signal levels will cause resistance modulation. This distortion may be improved by introducing local feedback as shown in figure 2 for best frequency response and impedance levels; eliminating the feedback capacitor will require the gate control voltage to be double for the same ON resistance. The resistor values should be equal, and about  $100\text{k}\Omega$ .

Best gate control voltage for best linearity is up to about  $0.8\text{V}_{\text{PK}}$ ; ON resistance increases rapidly beyond this point.

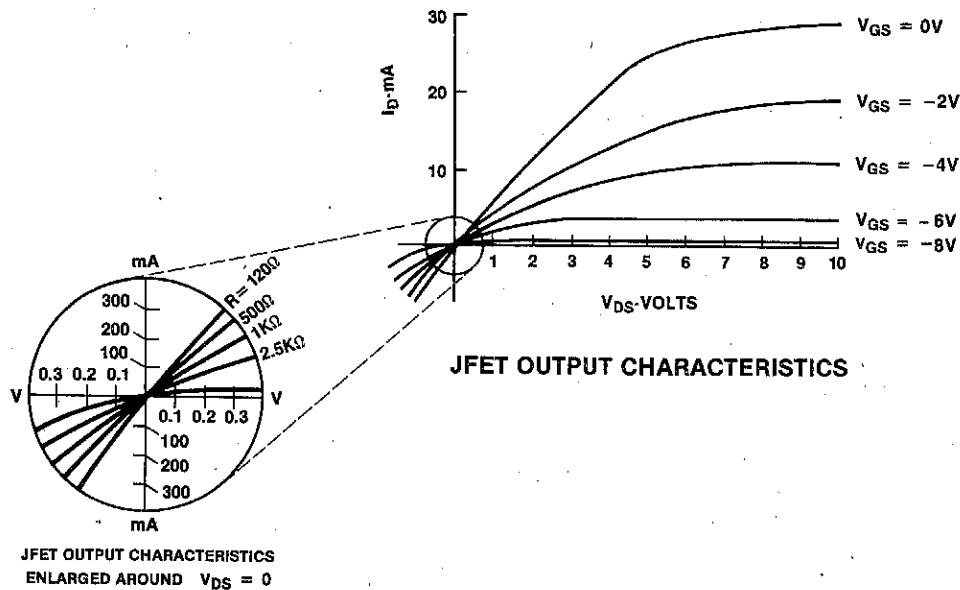


FIGURE 1

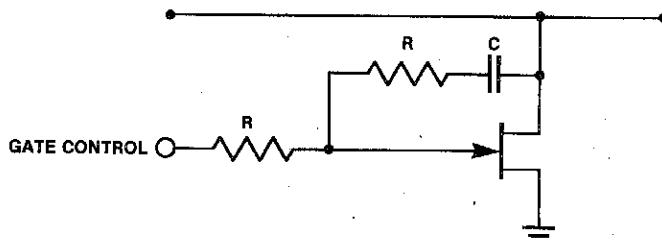


FIGURE 2

