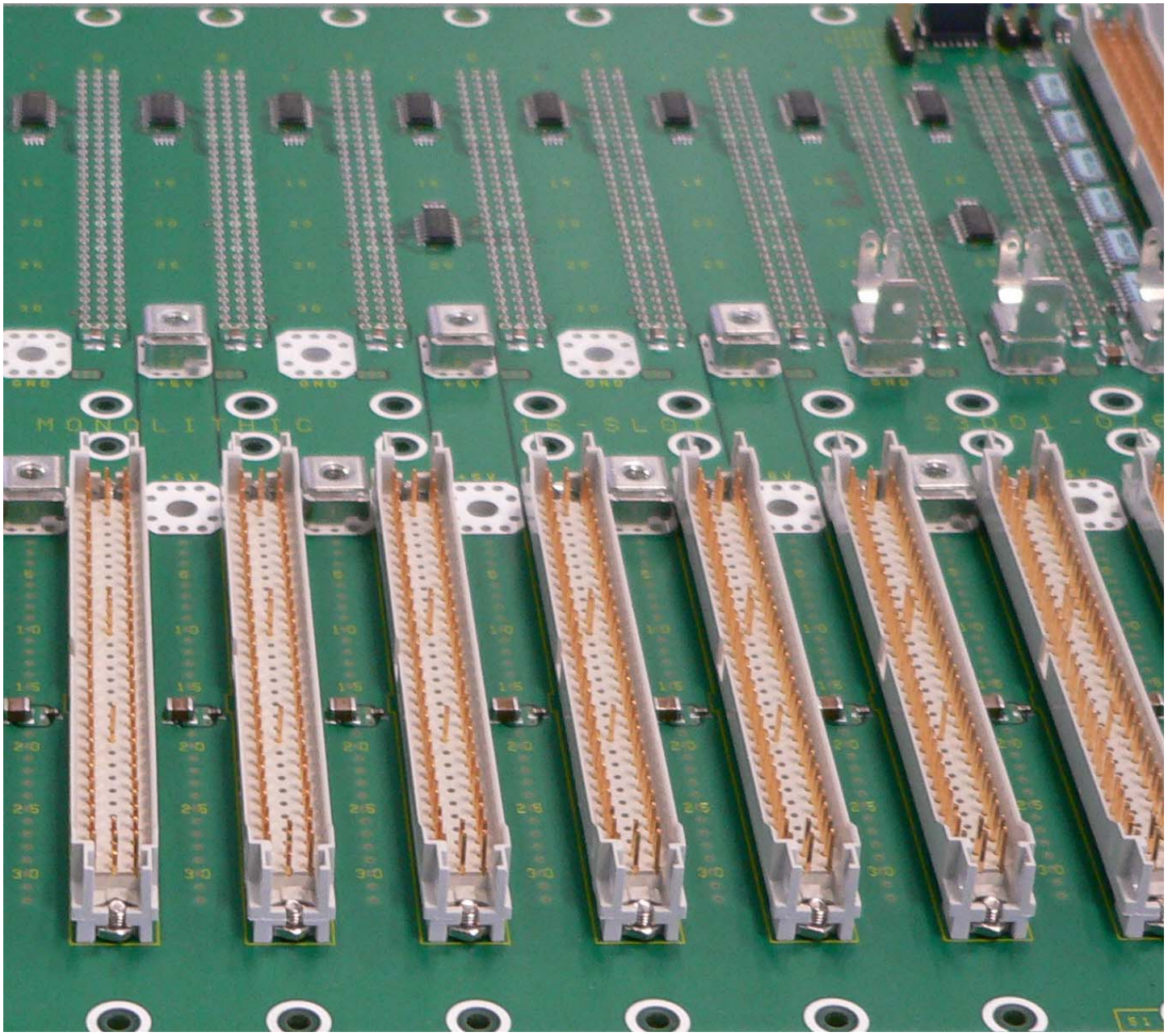
Schroff®

# User Manual
# VME / VME64x Backplanes



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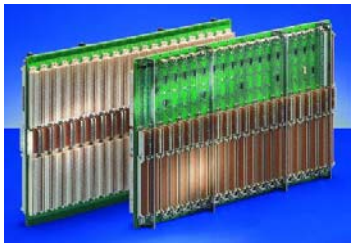
Pentair Enclosures



## What is VMEbus

The VMEbus started with the ANSI/VITA 1 specification in 1982. The original specification was sponsored by VITA and eventually standardized as IEEE 1014. It established a framework for 8-, 16- and 32-bit parallel-bus computer architectures that can implement single and multiprocessor systems. This bus includes the initial four basic subbuses: data transfer bus, priority interrupt bus, arbitration bus, and utility bus. Other architectures with other subbuses are possible within this VME framework.

In 1994, VME64 was formally approved by ANSI as ANSI/VITA 1-1994, incorporating all the features of VME32 and adding support for 64-bit transfers.

In 1998, the VME64 Extensions were officially approved as ANSI/VITA 1.1-1997. This standard is an extension of the ANSI/VITA 1-1994, VME64 Standard. It defines a set of features that can be added to VME and VME64 boards, backplanes and subracks. These features include a 160 pin connector (the 5-row DIN instead of the previous 3-row DIN), a P0 connector, geographical addressing, voltage pins for 3.3V, a test and maintenance bus, EMI, ESD, front panel handles and keying per IEEE 1101.10.

ANSI/VITA 1.5 is an extension of the ANSI/VITA 1-1994, VME64 and ANSI/VITA1.1-1997, VME64x standards. It extends performance by adding dual edge, source synchronous data transfer (2eSST) capability that allows sustained data transfers in excess of 300MB/sec.

ANSI/VITA 1.7 defines higher currents (2A) for the voltage pins on VME / VME64x equipment, ANSI/VITA 3 implements life insertion at VME64x boards and ANSI/VITA 38 finally adds system management features to the VME64x environment.

## What is VITA

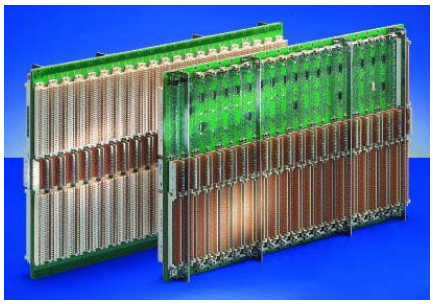
VITA, the **V**MEbus **I**nternational **T**rade **A**ssociation, is an incorporated, non-profit organization of vendors and users having a common market interest in real-time, modular embedded computing systems. Accredited as an American National Standards Institute (ANSI) developer and a submitter of Industry Trade Agreements to the IEC, the VITA Standards Organization provides its members with the ability to develop and to promote open technology standards.

### VME / VME64x Backplanes

**J1 Backplane**
The basic configuration is the 3U high (Single Eurocard) J1 plane. This plane provides all the address, data and control lines, and is fully capable of operating as a standalone bus.

**J2 Backplane**
For larger computer structures, the basic configuration can be extended with a second plane, the J2 plane, also 3U high. It´s located directly below the J1 plane in the 19-inch rack and extends the data and address space of the computer system. In addition, the user is provided with 64 freely-definable inputs/outputs per slot, which can be connected using interconnection points on the rear of the backplane. The J2 plane is only used as an extension of the VMEbus from the J1-plane and cannot be operated as a standalone bus.

**J1/J2 Monolithic Backplane**
Monolithic backplanes combine the J1 and J2 planes on a single printed circuit board. Because of its continuous power supply layer, the monolithic backplane is superior to two separate J1 and J2 planes, particularily with respect to dynamic current distribution.



# Schroff VME / VME64x Backplanes

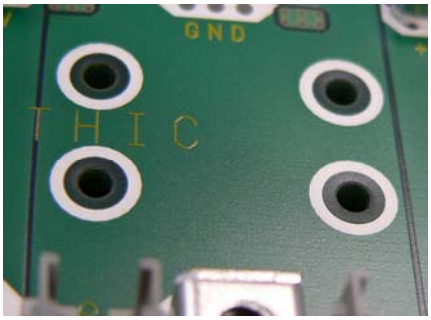
Schroff VME / VME64x backplanes are fully compliant to the latest VITA specifications.

| | |
|---|---|
| ANSI / VITA 1-1994 | VME64 Specification |
| ANSI / VITA 1.1-1997 | VME64x Specification |
| ANSI / VITA 1.5-2003 | VME2eSST Specification, VME64 and VME64x |
| ANSI / VITA 1.7-2003 | Increased Current Level |
| ANSI / VITA 3-1995 | Live Insertion System Requirements |
| ANSI / VITA 38-2003 | System Management Specification |

Schroff VME / VME64x backplanes are specially designed to achieve exellent power distribution, best signal integrity and virtually zero cross talk, The SMD components used on Schroff VME / VME64x backplanes lead to a much lower failure rate than conventional components.

Schroff uses ceramic capacitors on the VME / VME64x backplanes to gain a better noise reduction at frequencies above 10MHz. This feature reduces the radiated and conducted noise caused by the processor clock signals. In addition, ceramic capacitors have no limitation in useful lifetime, as compared to aluminium capacitors that dry out after 5 to 10 years, and are unaware of the hazardous fire risks known from tantalum electrolytics.

# Schroff VME / VME64x Backplane Features

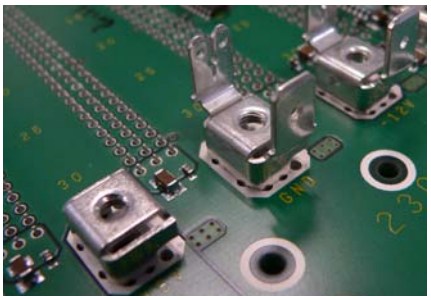



## Isolated Assembling / Connection to ChassisGND

Schroff VME / VME64x backplanes have a specially designed pattern of mounting holes to assemble the backplane isolated or connected to ChassisGND.

For isolation between BackplaneGND and ChassisGND M2.5 screws and isolating washers should be used in at least every second connector position.

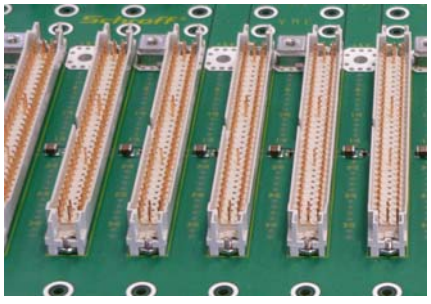
If noise reduction shall be achieved by connecting BackplaneGND to ChassisGND conductive spring washers are recommended instead of isolating ones.



## Power Input

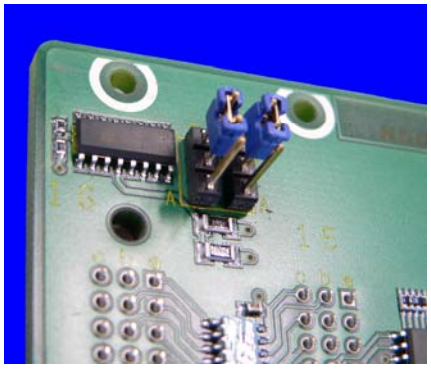
Schroff VME / VME64x backplanes are populated with specially designed power bugs. The power cables can be connected to the power bugs with cable lugs fastened with M4 screws. Each power bug can handle 30 Amps.

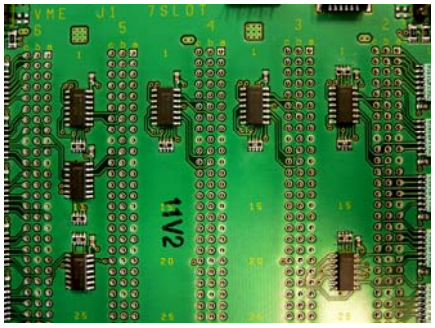
+5V Stdby input is realized with a faston terminal.



## Shrouds

Schroff VME / VME64x backplanes have long pins on the I/O positions and shrouds on all J2 positions and on 1J1. All other J1 postions have short pins. The long tails are gold plated.





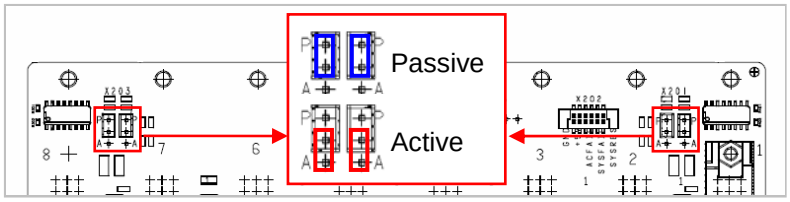
# Special Features of Schroff VME Backplanes

Schroff is offering VME J1, J2 and J1/J2 monolithic backplanes.

## Termination

Schroff VMEbus backplanes come with a passive inboard termination in the J2 area and with both, active and passive inboard termination, at J1. Active or passive termination can be selected with a jumper field at each upper end of the backplane.

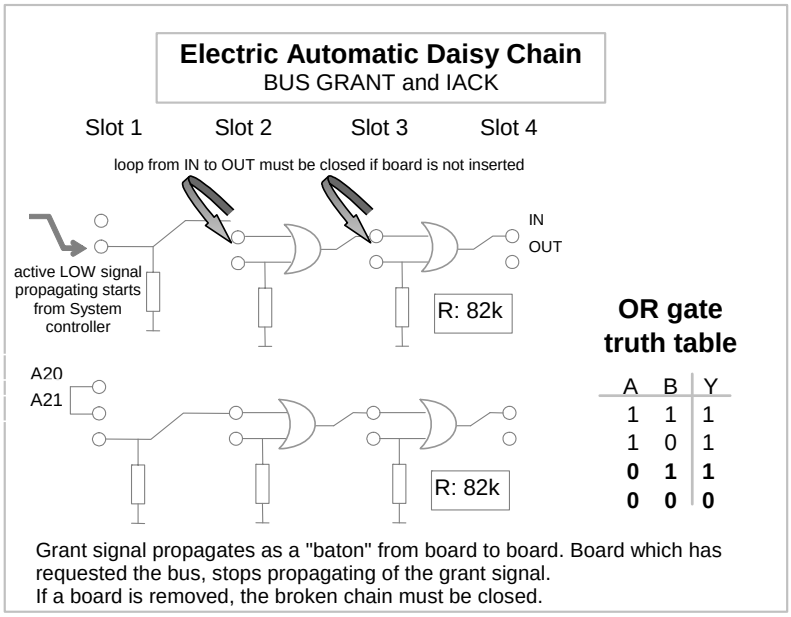
While the current consumption in non-operating mode is around 1,5A on a passive J1 backplane, the active termination reduces the current consumption of the backplane to 20mA.




## Daisy Chain

By default, Schroff VMEbus backplanes with more than 2 Slots are equipped with Electric Automatic Daisy Chain.

**E**lectric Automatic **D**aisy **C**hain (EDC**)** is achieved by integrated circuits with „or“ logic. When the daughter card is removed, the logic closes the chain.




**A**utomatic **D**aisy **C**hain (ADC), realized by a special connector with mechanical switches inside. This option is available on request.

**M**anual **D**aisy **C**hain (MDC), closes the connections by jumper pins. This option is available on request. Realized with a special C-96 J1 connector with long tails on the daisy chain pins, where the required connections can be made with jumpers.

## Latchable Shrouds

The shroud used on Schroff VME backplanes is prepared to accept optional latches. Two different latches are available, please refer to chapter „article numbers“, table accessories.

## Special Features of Schroff VME64x backplanes

Schroff is offering VME64x J1/J2 monolithic backplanes.

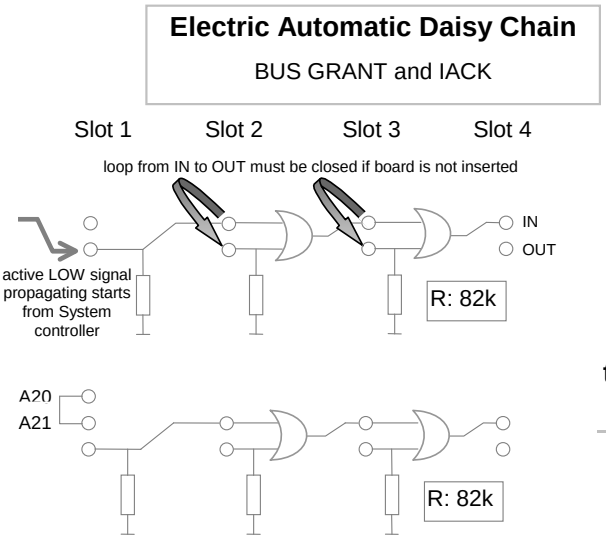
### Termination

Schroff VME64x backplanes come with a passive inboard termination.

### Daisy Chain

Schroff VME64x backplanes with more than 2 Slots are equipped with **E**lectric Automatic **D**aisy **C**hain.

**E**lectric Automatic **D**aisy **C**hain (EDC**)** is achieved by integrated circuits with „or“ logic. When the daughter card is extracted, the logic closes the chain.




**OR gate truth table**

| A | B | Y |
|---|---|---|
| 1 | 1 | 1 |
| 1 | 0 | 1 |
| **0** | **1** | **1** |
| **0** | **0** | **0** |

Grant signal propagates as a "baton" from board to board. Board which has requested the bus, stops propagating of the grant signal.
If a board is removed, the broken chain must be closed.

### Mechanical Stability

As the VME64x specification has implemented the P0 connector between the J1 and J2 area, there is no possibility of mounting the backplane to a horizontal centre profile. To prevent the bending of the 6U VME64x backplane during insertion and extraction of the daughter boards, the Schroff VME64x backplanes are equipped with Stiffeners.

### Live Insertion

Schroff VME64x backplanes fulfil the requirements of the VME Live Insertion standard VITA 3. The LI/I* (Live Insertion IN) is an active low input signal to a VME64x LI board that acts to enable/disable the on-board power control logic. A set of two pins per slot for LI/I* and GND spaced by 100mil is optional available to connect the signal to a radial power control module.

## Connectors on Schroff VME / VME64x Backplanes

### Pin Assignment VME / VME64x Connectors

### Table 1: VME64 J1/P1 Connector Pin Assignment

| Pin | Z | A | B | C | D |
|---|---|---|---|---|---|
| 1 | Reserved | D00 | BBSY* | D08 | Reserved |
| 2 | GND | D01 | BCLR* | D09 | Reserved |
| 3 | Reserved | D02 | ACFAIL* | D10 | Reserved |
| 4 | GND | D03 | BG0IN* | D11 | Reserved |
| 5 | Reserved | D04 | BG0OUT* | D12 | Reserved |
| 6 | GND | D05 | BG1IN* | D13 | Reserved |
| 7 | Reserved | D06 | BG1OUT* | D14 | Reserved |
| 8 | GND | D07 | BG2IN* | D15 | Reserved |
| 9 | Reserved | GND | BG2OUT* | GND | Reserved |
| 10 | GND | SYSCLK | BG3IN* | SYSFAIL* | Reserved |
| 11 | Reserved | GND | BG3OUT* | BERR* | Reserved |
| 12 | GND | DS1* | BR0* | SYSRESET* | Reserved |
| 13 | Reserved | DS0* | BR1* | LWORD* | Reserved |
| 14 | GND | WRITE* | BR2* | AM5 | Reserved |
| 15 | Reserved | GND | BR3* | A23 | Reserved |
| 16 | GND | DTACK* | AM0 | A22 | Reserved |
| 17 | Reserved | GND | AM1 | A21 | Reserved |
| 18 | GND | AS* | AM2 | A20 | Reserved |
| 19 | Reserved | GND | AM3 | A19 | Reserved |
| 20 | GND | IACK* | GND | A18 | Reserved |
| 21 | Reserved | IACKIN* | SERA | A17 | Reserved |
| 22 | GND | IACKOUT* | SERB | A16 | Reserved |
| 23 | Reserved | AM4 | GND | A15 | Reserved |
| 24 | GND | A07 | IRQ7* | A14 | Reserved |
| 25 | Reserved | A06 | IRQ6* | A13 | Reserved |
| 26 | GND | A05 | IRQ5* | A12 | Reserved |
| 27 | Reserved | A04 | IRQ4* | A11 | Reserved |
| 28 | GND | A03 | IRQ3* | A10 | Reserved |
| 29 | Reserved | A02 | IRQ2* | A09 | Reserved |
| 30 | GND | A01 | IRQ1* | A08 | Reserved |
| 31 | Reserved | -12V | +5VSTDBY | +12V | Reserved |
| 32 | GND | +5V | +5V | +5V | Reserved |
| Pin | Z | A | B | C | D |

**Note:** (*) These signals are active LOW
(1) Rows z and d are optional, not present on Schroff VME backplanes

**Table 2: VME64 J2/P2 Connector Pin Assignment**

| Pin | Z | A | B | C | D |
|---|---|---|---|---|---|
| 1 | Reserved | User Defined | +5V | User Defined | Reserved |
| 2 | GND | User Defined | GND | User Defined | Reserved |
| 3 | Reserved | User Defined | RETRY* | User Defined | Reserved |
| 4 | GND | User Defined | A24 | User Defined | Reserved |
| 5 | Reserved | User Defined | A25 | User Defined | Reserved |
| 6 | GND | User Defined | A26 | User Defined | Reserved |
| 7 | Reserved | User Defined | A27 | User Defined | Reserved |
| 8 | GND | User Defined | A28 | User Defined | Reserved |
| 9 | Reserved | User Defined | A29 | User Defined | Reserved |
| 10 | GND | User Defined | A30 | User Defined | Reserved |
| 11 | Reserved | User Defined | A31 | User Defined | Reserved |
| 12 | GND | User Defined | GND | User Defined | Reserved |
| 13 | Reserved | User Defined | +5V | User Defined | Reserved |
| 14 | GND | User Defined | D16 | User Defined | Reserved |
| 15 | Reserved | User Defined | D17 | User Defined | Reserved |
| 16 | GND | User Defined | D18 | User Defined | Reserved |
| 17 | Reserved | User Defined | D19 | User Defined | Reserved |
| 18 | GND | User Defined | D20 | User Defined | Reserved |
| 19 | Reserved | User Defined | D21 | User Defined | Reserved |
| 20 | GND | User Defined | D22 | User Defined | Reserved |
| 21 | Reserved | User Defined | D23 | User Defined | Reserved |
| 22 | GND | User Defined | GND | User Defined | Reserved |
| 23 | Reserved | User Defined | D24 | User Defined | Reserved |
| 24 | GND | User Defined | D25 | User Defined | Reserved |
| 25 | Reserved | User Defined | D26 | User Defined | Reserved |
| 26 | GND | User Defined | D27 | User Defined | Reserved |
| 27 | Reserved | User Defined | D28 | User Defined | Reserved |
| 28 | GND | User Defined | D29 | User Defined | Reserved |
| 29 | Reserved | User Defined | D30 | User Defined | Reserved |
| 30 | GND | User Defined | D31 | User Defined | Reserved |
| 31 | Reserved | User Defined | GND | User Defined | Reserved |
| 32 | GND | User Defined | +5V | User Defined | Reserved |
| Pin | Z | A | B | C | D |

(1) Rows z and d are optional, not present on Schroff VME backplanes

**Table 3: VME64x J1/P1 Connector Pin Assignment**

| Pin | Z | A | B | C | D |
|---|---|---|---|---|---|
| 1 | MPR | D00 | BBSY* | D08 | VPC (1) |
| 2 | GND | D01 | BCLR* | D09 | GND (1) |
| 3 | MCLK | D02 | ACFAIL* | D10 | +V1 |
| 4 | GND | D03 | BG0IN* | D11 | +V2 |
| 5 | MSD | D04 | BG0OUT* | D12 | RsvU |
| 6 | GND | D05 | BG1IN* | D13 | -V1 |
| 7 | MMD | D06 | BG1OUT* | D14 | -V2 |
| 8 | GND | D07 | BG2IN* | D15 | RsvU |
| 9 | MCTL | GND | BG2OUT* | GND | GAP* |
| 10 | GND | SYSCLK | BG3IN* | SYSFAIL* | GA0* |
| 11 | RESP* | GND | BG3OUT* | BERR* | GA1* |
| 12 | GND | DS1* | BR0* | SYSRESET* | +3.3V |
| 13 | RsvBus | DS0* | BR1* | LWORD* | GA2* |
| 14 | GND | WRITE* | BR2* | AM5 | +3.3V |
| 15 | RsvBus | GND | BR3* | A23 | GA3* |
| 16 | GND | DTACK* | AM0 | A22 | +3.3V |
| 17 | RsvBus | GND | AM1 | A21 | GA4* |
| 18 | GND | AS* | AM2 | A20 | +3.3V |
| 19 | RsvBus | GND | AM3 | A19 | SMB_SCL(2) |
| 20 | GND | IACK* | GND | A18 | +3.3V |
| 21 | RsvBus | IACKIN* | IPMB_SCL(2) | A17 | SMB_SDA(2) |
| 22 | GND | IACKOUT* | IPMB_SDA(2) | A16 | +3.3V |
| 23 | RsvBus | AM4 | GND | A15 | SMB_ALERT#(2) |
| 24 | GND | A07 | IRQ7* | A14 | +3.3V |
| 25 | RsvBus | A06 | IRQ6* | A13 | RsvBus |
| 26 | GND | A05 | IRQ5* | A12 | +3.3V |
| 27 | RsvBus | A04 | IRQ4* | A11 | LI/I* |
| 28 | GND | A03 | IRQ3* | A10 | +3.3V |
| 29 | RsvBus | A02 | IRQ2* | A09 | LI/O* |
| 30 | GND | A01 | IRQ1* | A08 | +3.3V |
| 31 | RsvBus | -12V | +5VSTBY | +12V | GND(1) |
| 32 | GND | +5V | +5V | +5V | VPC(1) |
| **Pin** | **Z** | **A** | **B** | **C** | **D** |

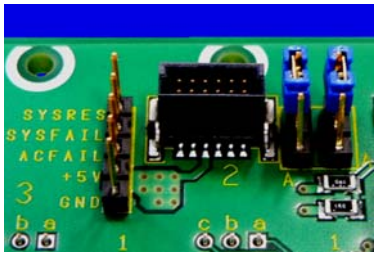
**Note:** (1) These pins are MFBL (mate-first-break-last) pins
(2) System management signals (IPMB..., SMB_...) introduced with VITA 38
(*) These signals are active LOW

**Table 4: VME64x J2/P2 Connector Pin Assignment**

| Pin | Z | A | B | C | D |
|---|---|---|---|---|---|
| 1 | User Defined | User Defined | +5V | User Defined | User Defined(1) |
| 2 | GND | User Defined | GND | User Defined | User Defined(1) |
| 3 | User Defined | User Defined | RETRY* | User Defined | User Defined |
| 4 | GND | User Defined | A24 | User Defined | User Defined |
| 5 | User Defined | User Defined | A25 | User Defined | User Defined |
| 6 | GND | User Defined | A26 | User Defined | User Defined |
| 7 | User Defined | User Defined | A27 | User Defined | User Defined |
| 8 | GND | User Defined | A28 | User Defined | User Defined |
| 9 | User Defined | User Defined | A29 | User Defined | User Defined |
| 10 | GND | User Defined | A30 | User Defined | User Defined |
| 11 | User Defined | User Defined | A31 | User Defined | User Defined |
| 12 | GND | User Defined | GND | User Defined | User Defined |
| 13 | User Defined | User Defined | +5V | User Defined | User Defined |
| 14 | GND | User Defined | D16 | User Defined | User Defined |
| 15 | User Defined | User Defined | D17 | User Defined | User Defined |
| 16 | GND | User Defined | D18 | User Defined | User Defined |
| 17 | User Defined | User Defined | D19 | User Defined | User Defined |
| 18 | GND | User Defined | D20 | User Defined | User Defined |
| 19 | User Defined | User Defined | D21 | User Defined | User Defined |
| 20 | GND | User Defined | D22 | User Defined | User Defined |
| 21 | User Defined | User Defined | D23 | User Defined | User Defined |
| 22 | GND | User Defined | GND | User Defined | User Defined |
| 23 | User Defined | User Defined | D24 | User Defined | User Defined |
| 24 | GND | User Defined | D25 | User Defined | User Defined |
| 25 | User Defined | User Defined | D26 | User Defined | User Defined |
| 26 | GND | User Defined | D27 | User Defined | User Defined |
| 27 | User Defined | User Defined | D28 | User Defined | User Defined |
| 28 | GND | User Defined | D29 | User Defined | User Defined |
| 29 | User Defined | User Defined | D30 | User Defined | User Defined |
| 30 | GND | User Defined | D31 | User Defined | User Defined |
| 31 | User Defined | User Defined | GND | User Defined | GND(1) |
| 32 | GND | User Defined | +5V | User Defined | VPC(1) |
| **Pin** | **Z** | **A** | **B** | **C** | **D** |

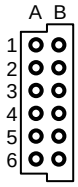
**Note:** (1) These pins are MFBL (mate-first-break-last) pins

## Additional Connectors on Schroff VME / VME64x Backplanes



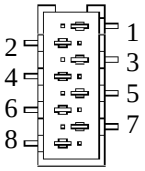

### Utility Connectors

12-pin fine-pitch connector, assembled on all Schroff VME64x and below mentioned VME backplanes
**23001-007, 23001-012, 23001-076, 23001-080**




| | |
|---|---|
| A1: nc | B1: nc |
| A2: nc | B2: -12V |
| A3: +12V | B3: +3.3V |
| A4: GND | B4: +5V |
| A5: nc | B5: ACFAIL |
| A6: SYSFAIL | B6: SYSRESET |

8-pin connector, pitch 2.54mm, assembled on all J1 and monolithic VME backplanes other than described above




1: GND
2: +5V
3: +12V
4: ACFAIL
5: -12V
6: SYSFAIL
7: nc
8: SYSRESET

5-pin connector, pitch 2.54mm, assembled on the Schroff VME J1 and monolithic backplanes

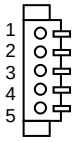
| Pin | Signal |
|---|---|
| 1 | Sysreset |
| 2 | Sysfail |
| 3 | ACFAIL |
| 4 | + 5V |
| 5 | GND |

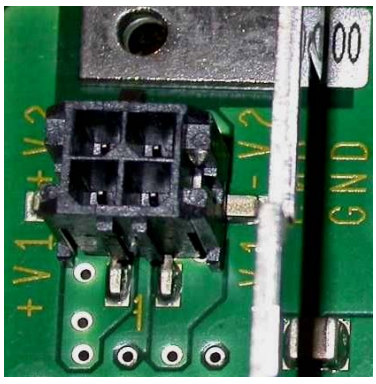

### IPMB Connector, VME64x Backplanes only

According to ANSI / VITA 38-2003, System Management Specification.

Vsm is connected to +5V Standby

1 SMB_SCL
2 GND
3 SMB_SDA
4 +5V Stdby
5 SMB_Alert

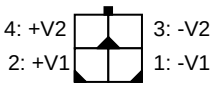


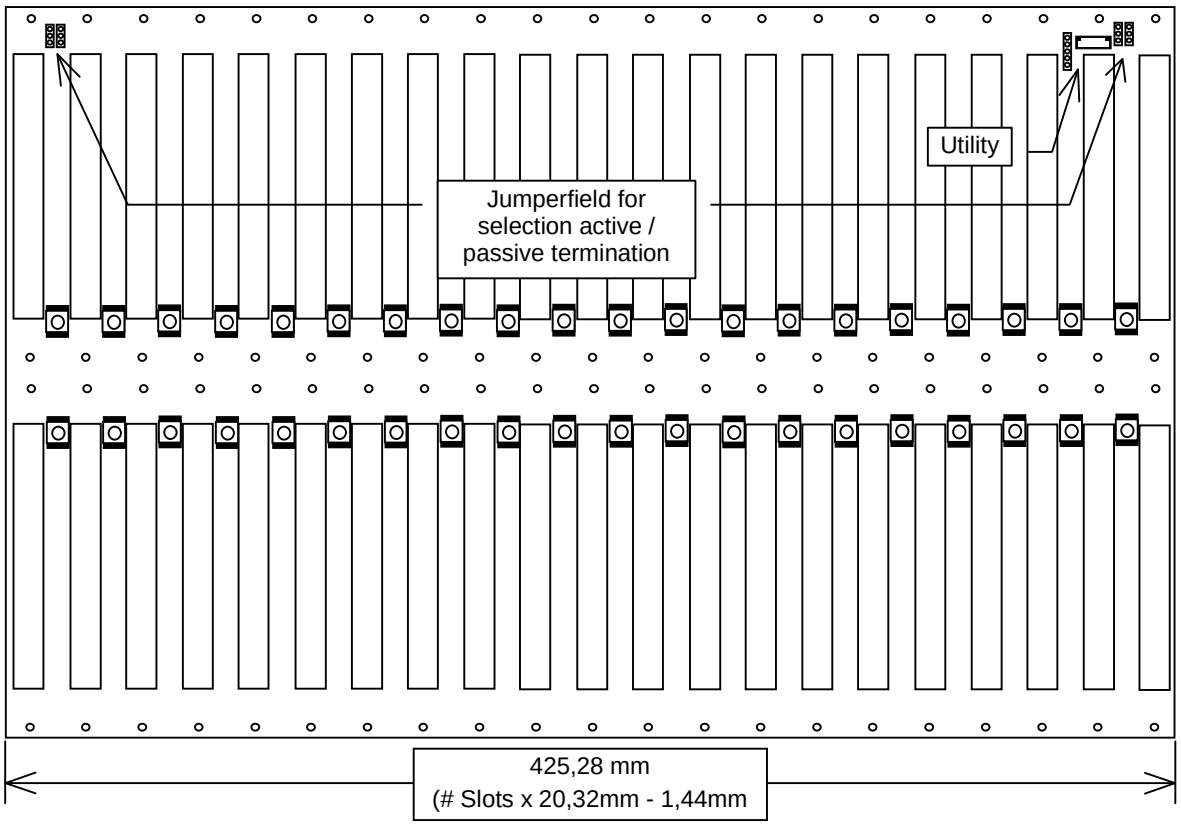

### V1 / V2 Connector, VME64x Backplanes only

V1/V2 auxiliary power supplied to the VME64x backplanes shall remain within the limits of 38V to 75V, including regulation variation, noise and ripple frequencies to 20 MHz.

If the +V1 and +V2 voltage rails are tied to ground and the +12V power is used, the nominal voltage between the +12V and the -V1 and -V2 power rails is 60 volts. With voltage tolerances, the 60 volt maximum is exceeded. Additional protection might be needed to comply with local and national regulatory agencies.



## Layout for 6U Monolithic VME Backplanes (rear view)




### Power Entry Table J1 Backplanes

| Powerbug between Slots | Slot x (Faston) | Slot 21-20 | Slot 20-19 | Slot 19-18 | Slot 18-17 | Slot 17-16 | Slot 16-15 | Slot 15-14 | Slot 14-13 | Slot 13-12 | Slot 12-11 | Slot 11-10 | Slot 10-9 | Slot 9-8 | Slot 8-7 | Slot 7-6 | Slot 6-5 | Slot 5-4 | Slot 4-3 | Slot 3-2 | Slot 2-1 | Slot 1 (Faston) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | | | | | +5V | GND | +-12V |
| 4 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | | | | +/-12 | +5V | GND | |
| 5 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | | | +/-12 | GND | +5V | GND | |
| 6 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | | +/-12 | +5V | GND | +5V | GND | |
| 7 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | +5V | GND | -12V | +12V | +5V | GND | |
| 8 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | +12V | +5V | GND | -12V | +12V | +5V | GND | |
| 9 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | -12V | +12V | +5V | GND | -12V | +12V | +5V | GND | |
| 10 Slot | $5V_{Stdby}$ | | | | | | | | | | | | -12V | +12V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 11 Slot | $5V_{Stdby}$ | | | | | | | | | | | -12V | +12V | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 12 Slot | $5V_{Stdby}$ | | | | | | | | | | -12V | +12V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 13 Slot | $5V_{Stdby}$ | | | | | | | | | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 14 Slot | $5V_{Stdby}$ | | | | | | | | -12V | +12V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 15 Slot | $5V_{Stdby}$ | | | | | | | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 16 Slot | $5V_{Stdby}$ | | | | | | -12V | +12V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 17 Slot | $5V_{Stdby}$ | | | | | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 18 Slot | $5V_{Stdby}$ | | | | -12V | +12V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 19 Slot | $5V_{Stdby}$ | | | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 20 Slot | $5V_{Stdby}$ | | -12V | +12V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |
| 21 Slot | $5V_{Stdby}$ | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | +5V | GND | |

NOTE: Not all powerbug positions might be assembled.

## Power Entry Table J2 Backplanes

| Powerbug between Slots | Slot x (Faston) | Slot 21-20 | Slot 20-19 | Slot 19-18 | Slot 18-17 | Slot 17-16 | Slot 16-15 | Slot 15-14 | Slot 14-13 | Slot 13-12 | Slot 12-11 | Slot 11-10 | Slot 10-9 | Slot 9-8 | Slot 8-7 | Slot 7-6 | Slot 6-5 | Slot 5-4 | Slot 4-3 | Slot 3-2 | Slot 2-1 | Slot 1 (Faston |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | | | | | +5V | GND | |
| 4 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | | | | GND | +5V | GND | |
| 5 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | | | +5V | GND | +5V | GND | |
| 6 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | | GND | +5V | GND | +5V | GND | |
| 7 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | | +5V | GND | +5V | GND | +5V | GND | |
| 8 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | |
| 9 Slot | $5V_{Stdby}$ | | | | | | | | | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 10 Slot | $5V_{Stdby}$ | | | | | | | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 11 Slot | $5V_{Stdby}$ | | | | | | | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 12 Slot | $5V_{Stdby}$ | | | | | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 13 Slot | $5V_{Stdby}$ | | | | | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 14 Slot | $5V_{Stdby}$ | | | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 15 Slot | $5V_{Stdby}$ | | | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 16 Slot | $5V_{Stdby}$ | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 17 Slot | $5V_{Stdby}$ | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 18 Slot | $5V_{Stdby}$ | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 19 Slot | $5V_{Stdby}$ | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 20 Slot | $5V_{Stdby}$ | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 21 Slot | $5V_{Stdby}$ | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |

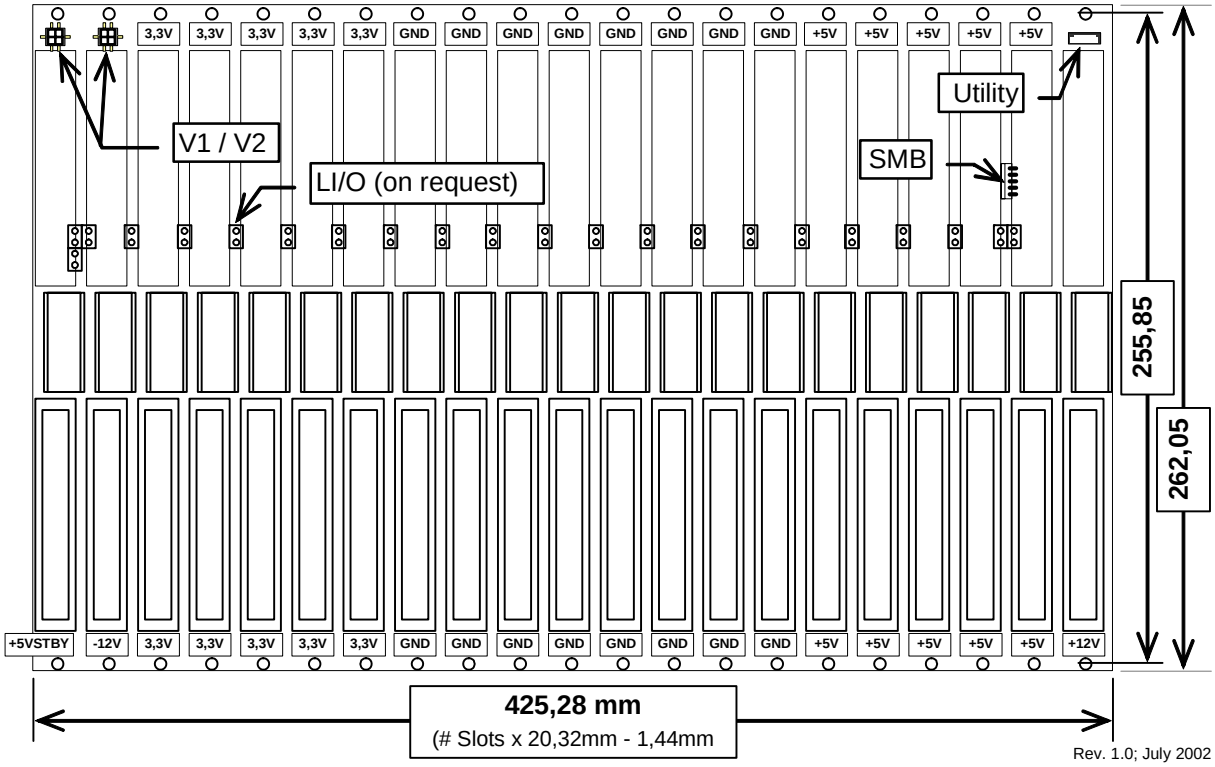
NOTE: Not all powerbug positions might be assembled.

## Power Entry Table Monolithic Backplanes

| Powerbug between Sl. | Slot x (Fast.) | Slot 21-20 | Slot 20-19 | Slot 19-18 | Slot 18-17 | Slot 17-16 | Slot 16-15 | Slot 15-14 | Slot 14-13 | Slot 13-12 | Slot 12-11 | Slot 11-10 | Slot 10-9 | Slot 9-8 | Slot 8-7 | Slot 7-6 | Slot 6-5 | Slot 5-4 | Slot 4-3 | Slot 3-2 | Slot 2-1 | Slot 1 (Fast.) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | | | | | | | | | | +5V | GND | +12V |
| 3 Sl J2 | GND | | | | | | | | | | | | | | | | | | | +5V | GND | -12V |
| 4 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | | | | | | | | | +/-12 | +5V | GND | |
| 4 Sl J2 | | | | | | | | | | | | | | | | | | | GND | +5V | GND | |
| 5 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | | | | | | | | +/-12 | GND | +5V | GND | |
| 5 Sl J2 | | | | | | | | | | | | | | | | | | +5V | GND | +5V | GND | |
| 6 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | | | | | | | +/-12 | +5V | GND | +5V | GND | |
| 6 Sl J2 | | | | | | | | | | | | | | | | | GND | +5V | GND | +5V | GND | |
| 7 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | | | | | | -12V | +12V | +5V | GND | +5V | GND | |
| 7 Sl J2 | | | | | | | | | | | | | | | | +5V | GND | +5V | GND | +5V | GND | |
| 8 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | | | | | -12V | +12V | GND | +5V | GND | +5V | GND | |
| 8 Sl J2 | | | | | | | | | | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | |
| 9 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | | | | -12V | +12V | +5V | GND | +5V | GND | -12V | +12V | |
| 9 Sl J2 | | | | | | | | | | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 10 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | | | -12V | +12V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 10 Sl J2 | | | | | | | | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 11 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 11 Sl J2 | | | | | | | | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 12 Sl J1 | $5V_{Stdby}$ | | | | | | | | | | -12V | +12V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 12 Sl J2 | | | | | | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 13 Sl J1 | $5V_{Stdby}$ | | | | | | | | | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 13 Sl J2 | | | | | | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 14 Sl J1 | $5V_{Stdby}$ | | | | | | | | -12V | +12V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 14 Sl J2 | | | | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 15 Sl J1 | $5V_{Stdby}$ | | | | | | | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 15 Sl J2 | | | | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 16 Sl J1 | $5V_{Stdby}$ | | | | | | -12V | +12V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 16 Sl J2 | | | | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 17 Sl J1 | $5V_{Stdby}$ | | | | | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 17 Sl J2 | | | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 18 Sl J1 | $5V_{Stdby}$ | | | | -12V | +12V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 18 Sl J2 | | | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 19 Sl J1 | $5V_{Stdby}$ | | | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 19 Sl J2 | | | | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 20 Sl J1 | $5V_{Stdby}$ | | -12V | +12V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 20 Sl J2 | | | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |
| 21 Sl J1 | $5V_{Stdby}$ | -12V | +12V | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | -12V | +12V | |
| 21 Sl J2 | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | +5V | GND | |

NOTE: Not all powerbug positions might be assembled.

## Layout for 6U Monolithic VME64x Backplanes (rear view)

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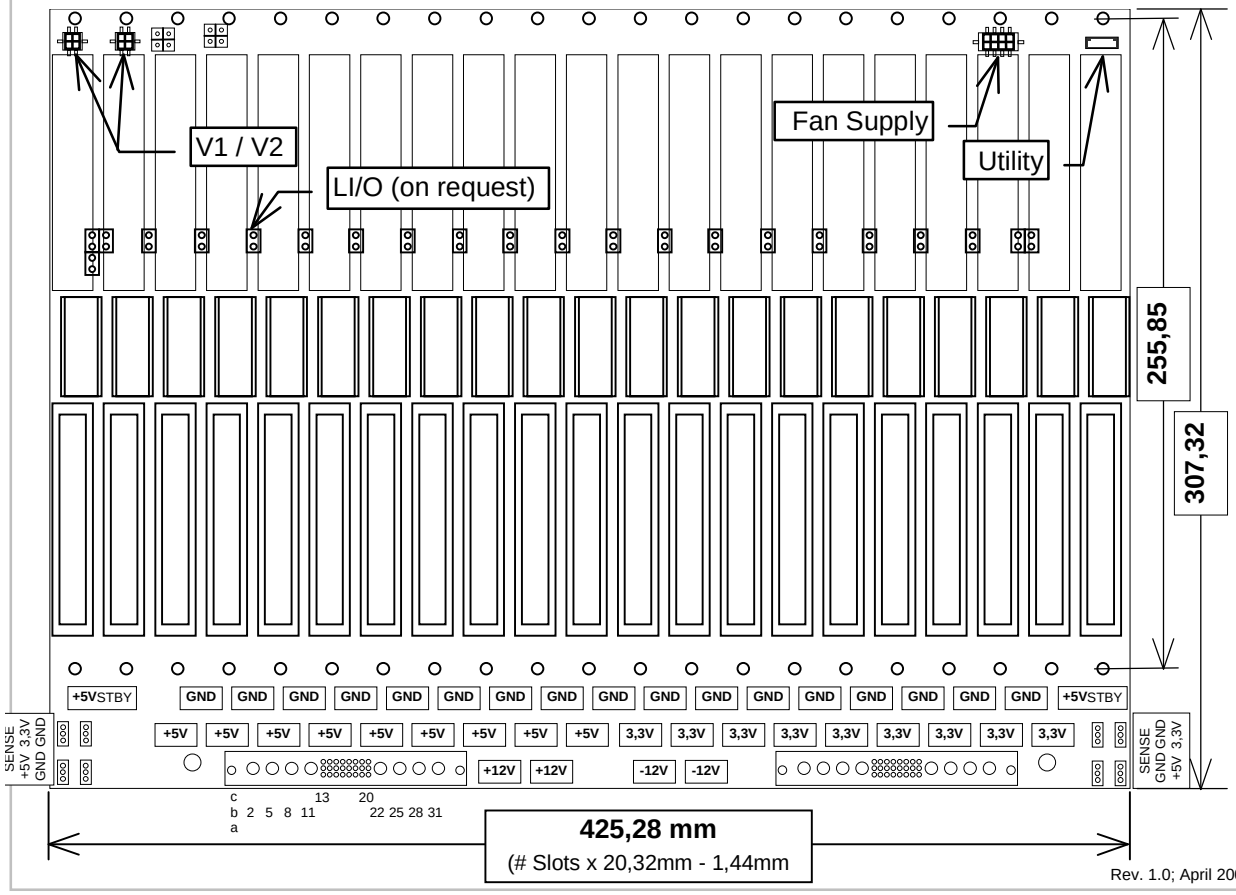
## Layout for 7U Monolithic VME64x Backplanes (rear view)




Rev. 1.0; April 2002

## Accessories

| Article Number | Description |
|---|---|
| 23204-113 | Cable IPMB, 750mm length (VME64x Backplanes) |
| 23204-115 | Cable Utility-Sense, 12-Way, 350mm length |
| 23204-116 | Cable Utility-Sense, 12-Way, 600mm length |
| 20800-304 | Cable Utility, 5-Way, 450mm length (VME Backplanes) |
| 60800-330 | Jumper Daisy Chain, 10 pieces (VME Backplanes) |
| 69001-995 | Locking lever, grey, long, for R96 mating connector (VME Backplanes) |
| 69001-106 | Locking lever, black, short, for C96 mating connector (VME Backplanes) |

## Mechanical and Climatic Parameters

| | VME Backplanes | VME64x Backplanes |
|---|---|---|
| **Operating Temperature** | -25°C - +85°C (active termination)<br>-40°C - +85°C (passive termination)<br>-40°C - +105°C (on request) | |
| **Storage Temperature** | -40°C - +105°C<br>-55°C - +105°C (on request) | |
| **Humidity** | 95%, non condensing<br>Conformal Coating (on request) | |
| **Climatic Test Group** (IEC68/1) | 25/085/21 | |
| **Flammability** (PCB, Connectors) | UL 94 V-0 | |
| **Connectors** (VME J1, J2) | DIN 41612 | IEC 61076-4-113<br>160 way extended DIN |
| Performance level per IEC 60603-2 | Level 2 | Level 2 |
| Mechanical Durability (Mating Cycles) | > 400 cycles | > 400 cycles |
| Total Insertion and Extraction Force | < 100 N | < 160 N |
| | DIN 41612 Level 1<br>(on request) | IEC 61076-4-113 Level 1<br>(on request) |
| **Connectors** (VME P0) | | IEC 61076-4-101<br>HM Modul B19, AB<br>compatible with AB Shroud |
| Performance level per IEC 60603-2 | | Level 2 |
| Mechanical Durability (Mating Cycles) | | > 250 cycles |
| Total Insertion and Extraction Force | | < 0,7 N / Pin |
| **Vibration** acc. DIN 41640 Part 15 | 10 Hz - 500 Hz, 5 g rms | |
| **Shock** (10 pulses each direction x, y, z) | 50 g, 6 ms | |
| **Low Pressure / Altitude**<br>(max voltage between two pins <=12V) | 250 mbar / 20.000 m | |
| **Dimensions** (mm) | | |
| Width | 20,32 mm x Slots - 1,4 mm | 20,32mm x Slots - 1,5 mm |
| Height (3U / 6U) | 128,70 / 262,05 mm | 262,05 mm |
| Thickness | 3,2 mm +/- 0,3 mm | 4,7 mm +/- 0,5 mm |

## Electrical Parameters

| | VME Backplanes | VME64x Backplanes |
|---|---|---|
| **Specifications** | ANSI/VITA 1-1994<br>VME64 Specification<br>ANSI/VITA 1.7 - 2003<br>Increased Current Level for 96 Pin & 160 Pin DIN/IEC Connector Standard | ANSI/VITA 1-1994<br>VME64 Specification<br>ANSI/VITA 1.1-1997<br>VME64x Specification<br>ANSI/VITA 1.5-2003<br>2eSST Transfer Protocol<br>ANSI/VITA 1.7 - 2003<br>Increased Current Level for 96 Pin & 160 Pin DIN/IEC Connector Standard<br>ANSI/VITA 3-1995<br>VME64x Live Insertion System Requirements<br>ANSI/VITA 38 – 2003<br>SMB Specification, Draft |
| **Service Life**<br>MTBF, acc. to MIL HDBK 217F, 25°C, ground, benign; 21-Slot Monolithic | more than 235.000 h | |
| **Characteristic Impedance** | 55 Ω ± 10 % | |
| **Ohmic Resistance** | < 60 mΩ / Slot | |
| **Hot Swap** | not supported | supported |
| **Termination** | active / passive, field changeable<br>330 / 470 Ohm Networks | passive<br>330 / 470 Ohm Networks |
| **Power input**<br>4 to 21 Slots<br>2 Slots | Power bugs for wiring, comprising M4 Screws<br>Fastons | |
| **Max. Current Carrying Capacity** | per ANSI/VITA 1.7-2003<br>3U BP:<br>+5V, 6 A / Slot @ 95°C<br>6U BP:<br>+5V, 12 A / Slot @ 95°C | per ANSI/VITA 1.7-2003<br>+5V: 12A / Slot @ 95°C<br>+3,3V: 18 A / Slot @ 95°C<br>+/-12V;+/-V1;+/-V2:<br>2 A / Slot @ 95°C each<br>VPC: 6 A / Slot @ 95°C |
| **Max. Voltage Drop** on +5V | < 50 mV | |
| **Data Transfer Rate** (peak)<br>MBLT protocol<br>2eVME<br>2eSST | 80 Mbyte/s<br>160 Mbyte/s | 80 Mbyte/s<br>160 Mbyte/s<br>320 Mbyte/s |