CY28353-2

Differential Clock Buffer/Driver

Features

- **Phase-locked loop (PLL) clock distribution for double data rate synchronous DRAM applications**
- **Distributes one differential clock input to six differential outputs**
- **External feedback pins (FBINT, FBINC) are used to synchronize the outputs to the clock input**
- **Conforms to the DDRI specification**
- **Spread Aware for electromagnetic interference (EMI) reduction**
- **28-pin SSOP package**

Description

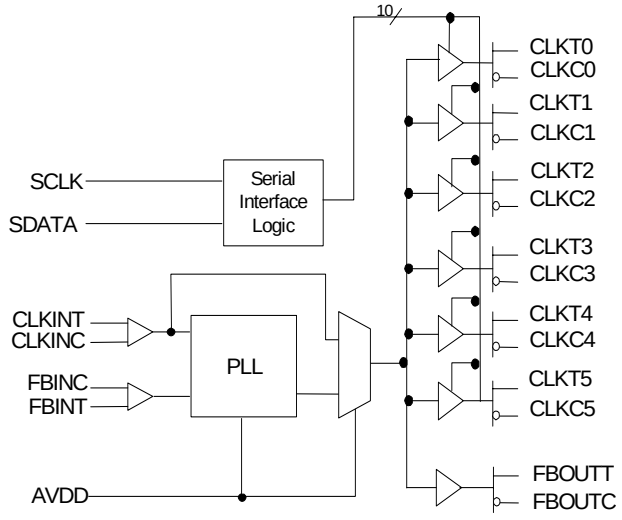
This PLL clock buffer is designed for 2.5 V_{DD} and 2.5 AV_{DD} operation and differential data input and output levels.

This device is a zero delay buffer that distributes a differential clock input pair (CLKINT, CLKINC) to six differential pairs of clock outputs (CLKT[0:5], CLKC[0:5]) and one differential pair feedback clock outputs (FBOUTT, FBOUTC). The clock outputs are controlled by the input clocks (CLKINT, CLKINC) and the feedback clocks (FBINT, FBINC).

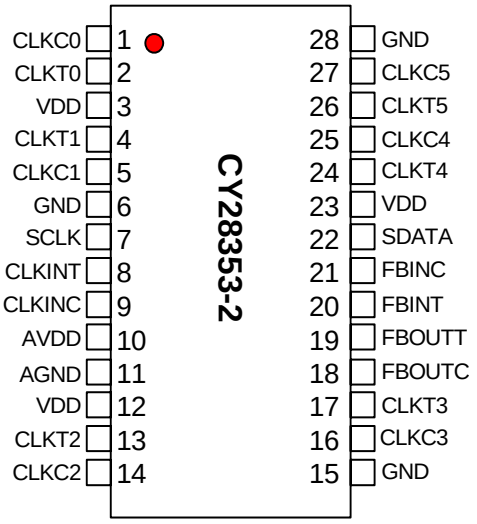
The two-line serial bus can set each output clock pair (CLKT[0:5], CLKC[0:5]) to the Hi-Z state. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

The PLL in this device uses the input clocks (CLKINT, CLKINC) and the feedback clocks (FBINT, FBINC) to provide high-performance, low-skew, low–jitter output differential clocks.

Block Diagram



Pin Configuration



28 pin SSOP

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Pin Description [1]

Pin Number	Pin Name	I/O	Pin Description	Electrical Characteristics
8	CLKINT	I	**Complementary Clock Input**.	LV Differential Input
9	CLKINC	I	**Complementary Clock Input**.	
21	FBINC	I	**Feedback Clock Input**. Connect to FBOUTC for accessing the PLL.	Differential Input
20	FBINT	I	**Feedback Clock Input**. Connect to FBOUTT for accessing the PLL.	
2,4,13,17,24,26	CLKT(0:5)	O	**Clock Outputs**.	Differential Outputs
1,5,14,16,25,27	CLKC(0:5)	O	**Clock Outputs**.	
19	FBOUTT	O	**Feedback Clock Output**. Connect to FBINT for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.	Differential Output
18	FBOUTC	O	**Feedback Clock Output**. Connect to FBINC for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.	
7	SCLK	I, PU	**Serial Clock Input**. Clocks data at SDATA into the internal register.	Data Input for the two-line serial bus
22	SDATA	I/O, PU	**Serial Data Input**. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.	Data Input and Output for the two-line serial bus
3,12,23	VDD		**2.5V Power Supply for Logic**.	2.5V Nominal
10	AVDD		**2.5V Power Supply for PLL**.	2.5V Nominal
6,15,28	GND		**Ground**.	
11	AGND		**Analog Ground for PLL**.	

Function Table

Inputs			Outputs				
VDDA	**CLKINT**	**CLKINC**	**CLKT(0:5)**[2]	**CLKC(0:5)**[2]	**FBOUTT**	**FBOUTC**	**PLL**
GND	L	H	L	H	L	H	BYPASSED/OFF
GND	H	L	H	L	H	L	BYPASSED/OFF
2.5V	L	H	L	H	L	H	On
2.5V	H	L	H	L	H	L	On
2.5V	< 20 MHz	< 20 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Off

Notes:
1. A bypass capacitor (0.1 µF) should be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins their high-frequency filtering characteristic will be cancelled by the lead inductance of the traces.
2. Each output pair can be three-stated via the two-line serial interface.

Zero Delay Buffer

When used as a zero delay buffer the CY28353-2 will likely be in a nested clock tree application. For these applications the CY28353-2 offers a differential clock input pair as a PLL reference. The CY28353-2 then can lock onto the reference and translate with near zero delay to low skew outputs. For normal operation, the external feedback input, FBINT, is connected to the feedback output, FBOUTT. By connecting the feedback output to the feedback input the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

When VDDA is strapped low, the PLL is turned off and bypassed for test purposes.

Power Management

The individual output enable/disable control of the CY28353-2 allows the user to implement unique power management schemes into the design. Outputs are tri-stated when disabled through the two-line interface as individual bits are set low in Byte0 and Byte1 registers. The feedback output pair (FBOUTT, FBOUTC) cannot be disabled via two line serial bus. The enabling and disabling of individual outputs is done in such a manner as to eliminate the possibility of partial “runt” clocks.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block r\ead operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 Bits	18:11	Command Code – 8 Bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits (Skip this step if I^2C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N –8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge

Table 2. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge
		...	Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

Byte0: Output Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	1	2, 1	CLKT0, CLKC0
6	1	4, 5	CLKT1, CLKC1
5	1	–	Reserved
4	1	–	Reserved
3	1	13, 14	CLKT2, CLKC2
2	1	26, 27	CLKT5, CLKC5
1	1	–	Reserved
0	1	24, 25	CLKT4, CLKC4

Byte1: Output Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	1	–	Reserved
6	1	17, 16	CLKT3, CLKC3
5	0	–	Reserved
4	0	–	Reserved
3	0	–	Reserved
2	0	–	Reserved
1	0	–	Reserved
0	0	–	Reserved

Byte2: Test Register 3

Bit	@Pup	Pin#	Description
7	1	–	0 = PLL leakage test, 1 = disable test
6	1	–	Reserved
5	1	–	Reserved
4	1	–	Reserved
3	1	–	Reserved
2	1	–	Reserved
1	1	–	Reserved
0	1	–	Reserved

Maximum Ratings[3]

Input Voltage Relative to V_{SS}:.....V_{SS} – 0.3V

Input Voltage Relative to V_{DDQ} or AV_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: ..... –65°C to +150°C

Operating Temperature:..... 0°C to +85°C

Maximum Power Supply:.....3.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range:

$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters $V_{DDA} = V_{DDQ} = 2.5V + 5\%$, $T_A = 0°C$ to $+70°C$[4]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VIL	Input Low Voltage	SDATA, SCLK			1.0	V
VIH	Input High Voltage		2.2			V
VID	Differential Input Voltage[5]	CLKINT, FBINT	0.35		V_{DDQ} + 0.6	V
VIX	Differential Input Crossing Voltage[6]	CLKINT, FBINT	$(V_{DDQ}/2) – 0.2$	$V_{DDQ}/2$	$(V_{DDQ}/2) + 0.2$	V
IIN	Input Current	V_{IN} = 0V or $V_{IN} = V_{DDQ}$, CLKINT, FBINT	–10		10	µA
IOL	Output Low Current	V_{DDQ} = 2.375V, V_{OUT} = 1.2V	26	35		mA
IOH	Output High Current	V_{DDQ} = 2.375V, V_{OUT}=1V	–18	–32		mA
VOL	Output Low Voltage	V_{DDQ} = 2.375V, I_{OL} = 12 mA			0.6	V
VOH	Output High Voltage	V_{DDQ} = 2.375V, I_{OH} = –12 mA	1.7			V
VOUT	Output Voltage Swing[7]		1.1		V_{DDQ} – 0.4	V
VOC	Output Crossing Voltage[8]		$(V_{DDQ}/2) – 0.2$	$V_{DDQ}/2$	$(V_{DDQ}/2) + 0.2$	V
IOZ	High-impedance Output Current	V_O = GND or $V_O = V_{DDQ}$	–10		10	µA
IDDQ	Dynamic Supply Current[9]	All V_{DDQ} and V_{DDI}, F_O = 170 MHz		235	300	mA
IDSTAT	Static Supply Current				1	mA
IDD	PLL Supply Current	V_{DDA} only		9	12	mA
Cin	Input Pin Capacitance			4	6	pF

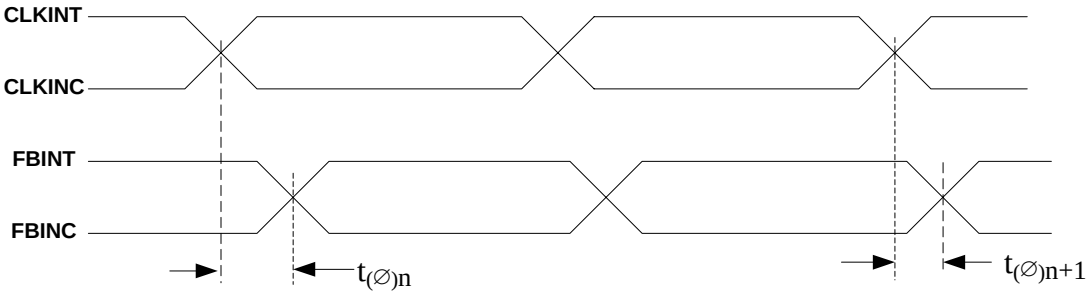
AC Parameters $V_{DD} = V_{DDQ} = 2.5V \pm 5\%$, $T_A = 0°C$ to $+70°C$ [10,11]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
fCLK	Operating Clock Frequency	AV_{DD}, $V_{DD} = 2.5V \pm 0.2V$	60		170	MHz
tDC	Input Clock Duty Cycle		40		60	%
tlock	Maximum PLL lock Time				100	µs
Tr / Tf	Output Clocks Slew Rate	20% to 80% of V_{OD}	1		2.5	V/ns
tpZL, tpZH	Output Enable Time[12](all outputs)			3		ns
tpLZ, tpHZ	Output Disable Time[12] (all outputs)			3		ns
tCCJ	Cycle to Cycle Jitter	f > 66 MHz	–100		100	ps
tjit(h-per)	Half-period jitter[14]	f > 66 MHz	–100		100	ps
tPLH	Low-to-High Propagation Delay, CLKINT to CLKT[0:5]		1.5	3.5	6	ns
tPHL	High-to-Low Propagation Delay, CLKINT to CLKT[0:5]		1.5	3.5	6	ns
tSKEW	Any Output to Any Output Skew[13]				100	ps
tPHASE	Phase Error[13]		–150		150	ps
tPHASEJ	Phase Error Jitter	f > 66MHz	–50		50	ps

Notes:

3. **Multiple Supplies**: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply srquencing is NOT required.
4. Unused inputs must be held HIGH or LOW to prevent them from floating.
5. Differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
6. Differential cross-point input voltage is expected to track VDDQ and is the voltage at which the differential signals must be crossing.
7. For load conditions see *Figure 7*.
8. The value of VOC is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120Ω resistor. See *Figure 7*.
9. All outputs switching loaded with 16 pF in 60Ω environment. See *Figure 7*.
10. Parameters are guaranteed by design and characterization. Not 100% tested in production.
11. PLL is capable of meeting the specified parameters while supporting SSC synthesizers with modulation frequency between 30 kHz and 33.3 kHz with a down spread of –0.5%.
12. Refers to transition of non-inverting output.

Differential Parameter Measurement Information



$$t_{(\varnothing)n} = \frac{\sum_{1}^{n=N} t_{(\varnothing)n}}{} \quad \text{(N is large number of samples)}$$

Figure 1. Static Phase Offset

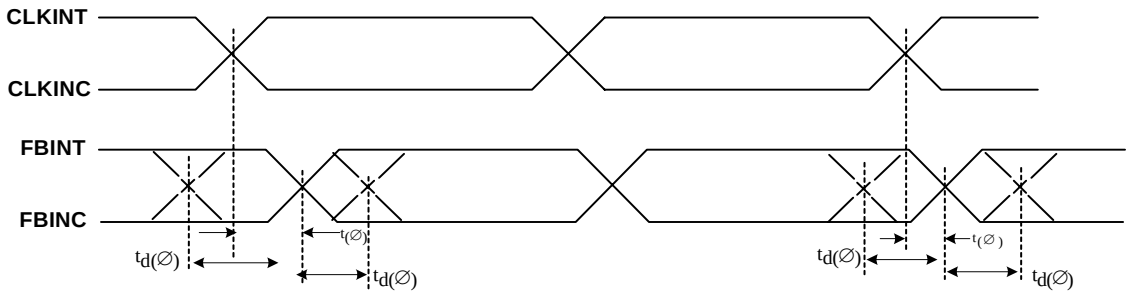


Figure 2. Dynamic Phase Offset

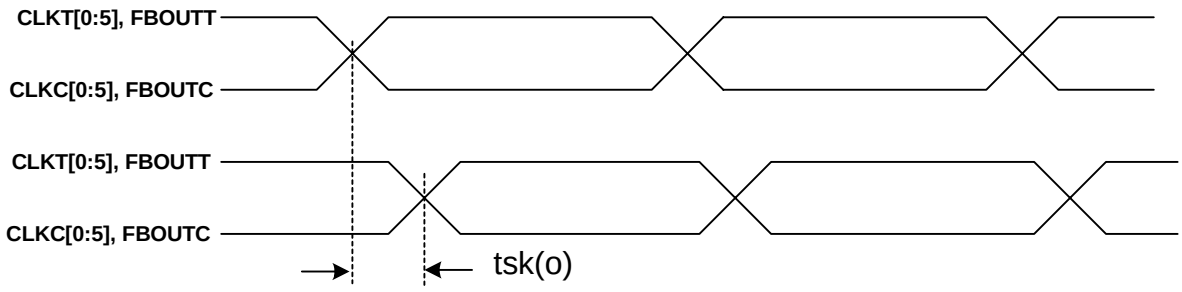
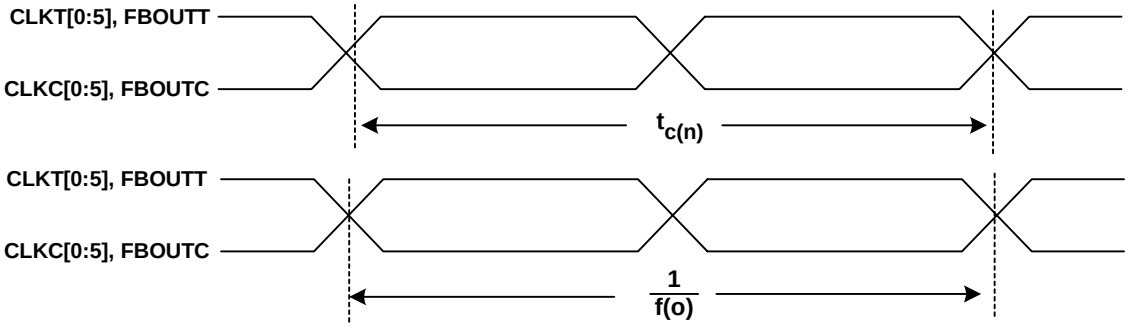


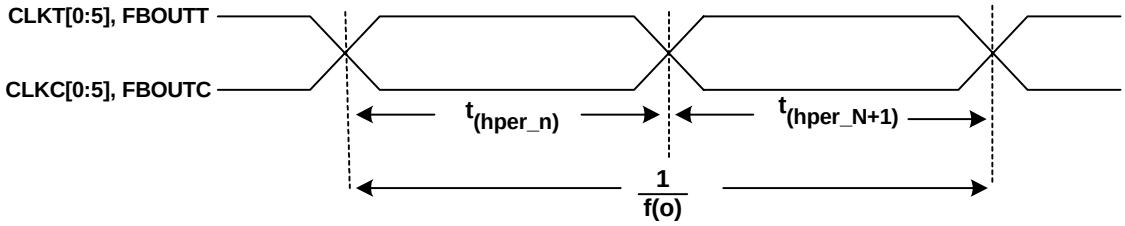
Figure 3. Output Skew

Notes:
13. All differential input and output terminals are terminated with 120Ω/16 pF, as shown in *Figure 7*.
14. Period Jitter and Half-period Jitter specifications are separate specifications that must be met independently of each other.



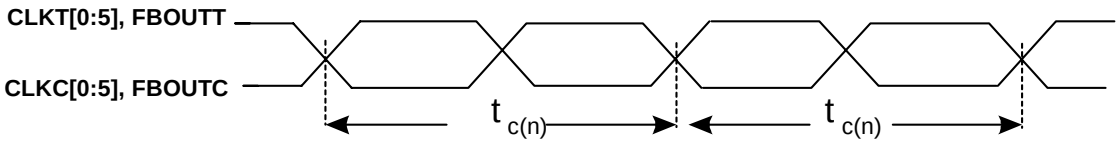
$$t_{jit(hper)} = t_{c(n)} - \frac{1}{fo}$$

Figure 4. Period Jitter



$$t_{jit(hper)} = t_{hper(n)} - \frac{1}{2x\ fo}$$

Figure 5. Half-Period Jitter



$$t_{jit(cc)} = t_{c(n)} - t_{c(n+1)}$$

Figure 6. Cycle-to-Cycle Jitter

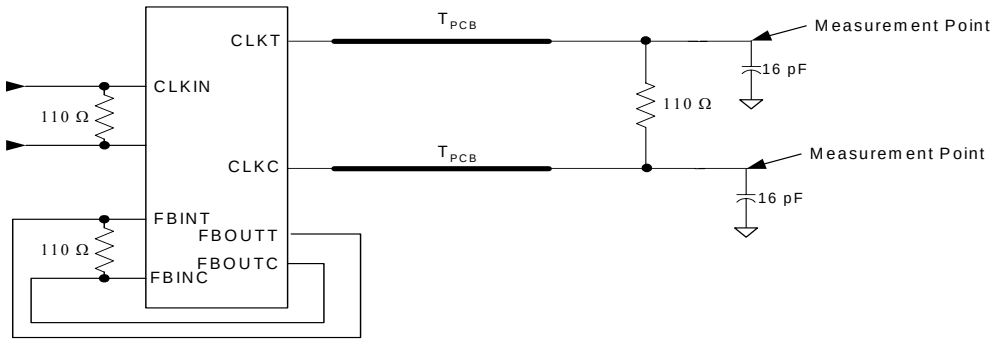


Figure 7. Differential Signal Using Direct Termination Resistor

Ordering Information

Part Number	Package Type	Product Flow
CY28353OC-2	28-pin SSOP	Commercial, 0° to 70°C
CY28353OC-2T	28-pin SSOP–Tape and Reel	Commercial, 0° to 70°C
Lead Free		
CY28353OXC-2	28-pin SSOP	Commercial, 0° to 70°C
CY28353OXC-2T	28-pin SSOP–Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

28-Lead (5.3 mm) Shrunk Small Outline Package O28