

CoreU1PHY – UTOPIA Level 1 PHY Interface

Product Summary

Intended Use

- Standard UTOPIA Level 1 PHY Interface to any ATM Link-Layer Device

Key Features

- Standard 8-Bit, 25 MHz UTOPIA Level 1 PHY Interface Complies with the ATM Forum UTOPIA Specification, Level 1 Version 2.01 (af-phy-0017.000)
- Separate TX and RX Clocks and Interface Pins
- Supports Cell-Level Handshake for 53- or 54-byte ATM Cells with Automatic Add/Drop of UDF2 Field in the ATM Header in 53-byte Mode
- 16-Bit (54-byte) User Interfaces Can be Used Directly or Bolt-Up to One of Actel's ATM Cell Buffer Blocks: ATMBUFx

Supported Families

- Fusion
- ProASIC3/E
- ProASIC^{PLUS}[®]
- Accelerator[®]

Core Deliverables

- Netlist Version
 - Compiled RTL Simulation Model Fully Supported in Actel Libero[®] Integrated Design Environment (IDE)
 - Structural VHDL and Verilog Netlists (with and without I/O Pads) Compatible with Actel's

Libero IDE and Industry Standard Synthesis and Simulation Tools

- RTL Version
 - VHDL Source Code
 - Core Synthesis and Simulation Scripts
- Actel-Developed Testbench (VHDL) Fully Supported by Industry-Standard Simulation Tools

Design Tools Support

- Simulation: VITAL Compliant VHDL and OVI Compliant Verilog Simulators
- Synthesis: LeonardoSpectrum[®], Synplify[®], Design Compiler[®], FPGA Compiler[™], and FPGA Express[™]

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General Description

CoreU1PHY is a UTOPIA Level 1 PHY interface core that connects directly to any ATM link-layer (master) device and user logic (or optional ATM cell buffer blocks) to provide an interface between the link-layer device and a non-standard physical layer device (Figure 1).

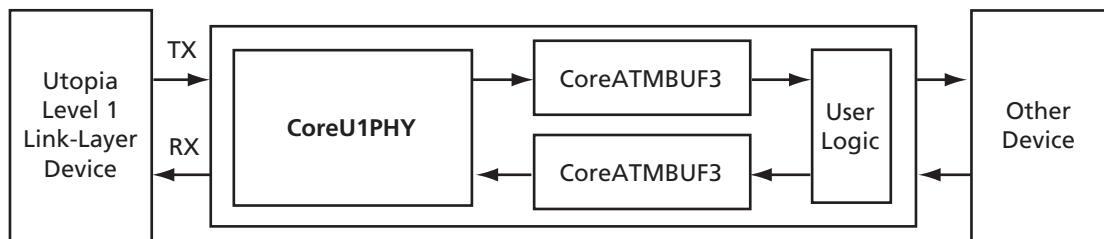


Figure 1 • Block Diagram

Device Requirements

CoreU1PHY can be implemented in either the ProASIC^{PLUS} or Axcelerator device families. Table 1 indicates the number of core logic cells required in each technology.

Table 1 • Device Utilization and Performance

| Family | Cells or Tiles | | Total Utilization | | Performance |
|-------------------------|----------------|---------------|-------------------|------------|-------------|
| | Sequential | Combinatorial | Device | Percentage | |
| Fusion | 59 | 61 | AFS060 | 8.0% | 25 MHz |
| ProASIC3/E | 59 | 61 | A3P060 | 8.0% | 25 MHz |
| ProASIC ^{PLUS} | 79 | 58 | APA075 | 4.5% | >25 MHz |
| Axcelerator | 60 | 60 | AX125 | 6.0% | >25 MHz |

UTOPIA Interface

CoreU1PHY implements a standard 8-bit point-to-point physical-layer interface that supports cell lengths of either 53 or 54 bytes. If the cell_size bit is low, a 53-byte cell is transferred and the UDF2 byte is inserted on ingress to and dropped on egress from the user interface; otherwise, 54 bytes are transferred. The UTOPIA interface signals are summarized in Table 2.

Table 2 • UTOPIA Interface Signals

| Signal | Type | Description |
|------------|------|---|
| u1_tx_clk | In | TX interface clock |
| u1_tx_clav | Out | Active high cell buffer space available |
| u1_tx_en | In | Active low data transfer enable |
| u1_tx_soc | In | Active high start-of-cell indication |
| u1_tx_data | In | 8-bit ingress data |
| u1_rx_clk | In | RX interface clock |
| u1_rx_clav | Out | Active high cell buffer space available |
| u1_rx_en | In | Active low data transfer enable |
| u1_rx_soc | Out | Active high start-of-cell indication |
| u1_rx_data | Out | 8-bit ingress data |

TX Interface (Ingress)

The process of transferring a cell on the UTOPIA level 1 TX interface begins with u1_tx_clav. The core asserts u1_tx_clav high whenever w_avail is asserted at the user interface. If u1_tx_clav is low, the link-layer device must wait until CoreU1PHY indicates that it is ready to receive another cell.

To begin sending cells on the TX interface, the link-layer simply asserts u1_tx_en low (Figure 2).

CoreU1PHY will then look for u1_tx_soc to become active (high), indicating that the first word of the cell transfer is active on the bus. As shown in Figure 2, u1_tx_soc may be asserted during the same cycle that u1_tx_en is driven low. Once u1_tx_soc is recognized, the core accepts 53 bytes (or 54) and forwards them to the user interface.

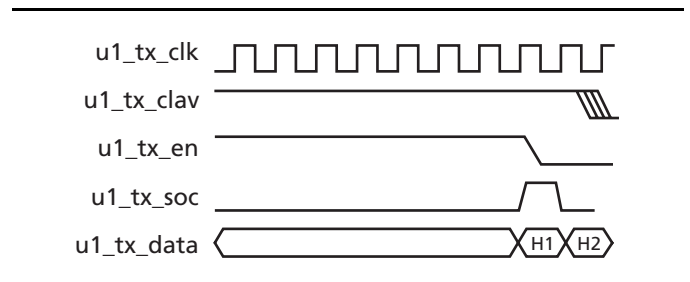


Figure 2 • TX Start of Cell

If the link-layer device does not have another cell to send, or if polling during the current cell transfer indicates that the CoreU1PHY is not ready to accept another cell, the U1 link-layer may deselect the physical interface by de-asserting u1_tx_en after the last word of the transfer (Figure 3).

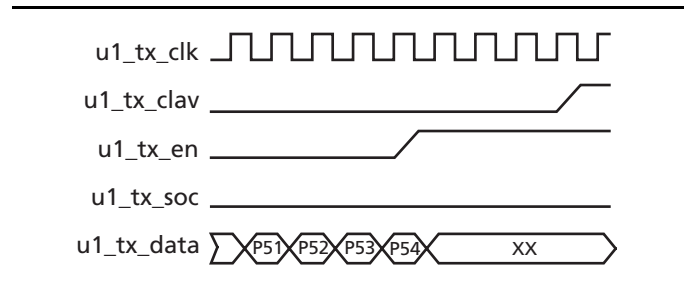


Figure 3 • TX Transfer Complete

Alternatively, the link-layer device may choose to stall in-between cells without deselecting the physical interface, as illustrated in [Figure 4](#).

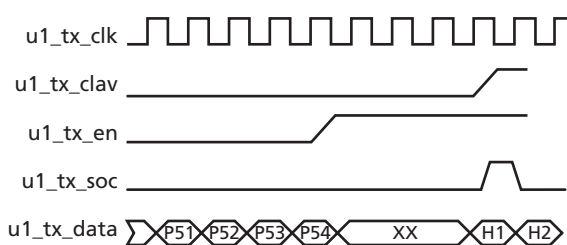


Figure 4 • TX Stalled by u1_tx_clav

If the link-layer has another cell to send to the physical interface and if polling during the current cell indicates that the CoreU1PHY is able to accept another cell, the link-layer may send cells back-to-back, as illustrated in [Figure 5](#).

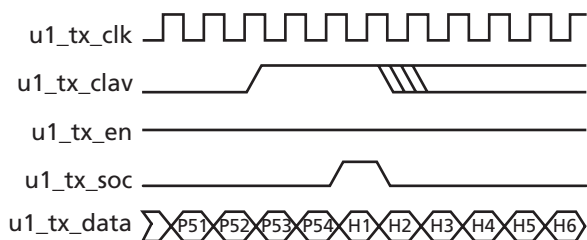


Figure 5 • TX Back-to-Back Transfer

RX Interface (Egress)

The RX interface operates in a similar manner. The process begins with u1_rx_clav. If the user interface indicates there is at least one complete cell available for transfer by asserting r_avail high, the core responds with u1_rx_clav high; otherwise, u1_rx_clav is asserted low and the link-layer device must wait until the user logic indicates that a cell is available for transfer.

To begin receiving cells on the RX interface, the link-layer must select the CoreU1PHY by asserting u1_rx_en low ([Figure 6](#)).

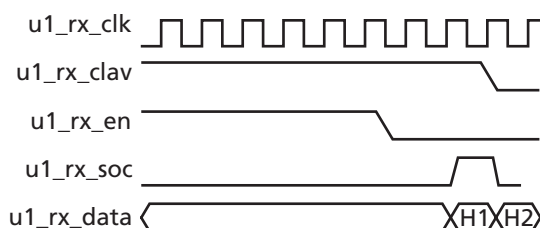


Figure 6 • RX Start of Cell Transfer

The CoreU1PHY will then assert u1_rx_soc high, indicating that the first word of the cell transfer is active on the bus. Once a transfer has begun, all 53 or 54 bytes of the cell are transferred without interruption.

If polling during the current transfer indicates that there are no more cells available, or if the link-layer is unable to receive another cell from the CoreU1PHY, the link-layer may deselect the physical interface by de-asserting u1_rx_en after receiving the last byte of the current cell, as illustrated in [Figure 7](#).

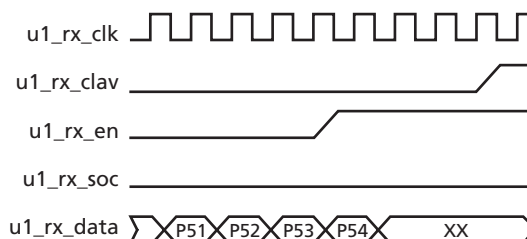


Figure 7 • RX End of Transfer

If the link-layer continues to enable the CoreU1PHY during the last two bytes of the current cell transfer, and one or more complete ATM cells are ready to be transferred (u1_rx_avail is high), the CoreU1PHY will send back-to-back cells, as shown in [Figure 8](#). If the user interface indicates r_avail low (no data to send), but the link-layer continues to assert U1_rx_en low, the CoreU1PHY interface will remain idle until r_avail is asserted high on the user interface and another cell transfer begins.

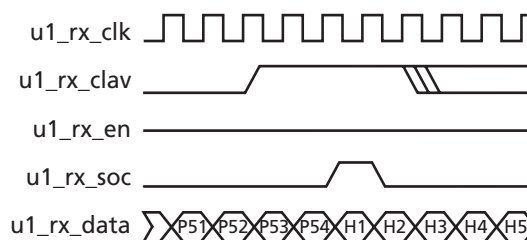


Figure 8 • RX Back-to-Back Transfer

User Interface

The user interface can connect directly to Actel's CoreATMBUF3 cell buffer, an intellectual property core that provides buffering for up to three 54-byte ATM cells in each direction (Figure 1 on page 1). Alternatively, the designer may choose to connect his/her own cell buffer or user logic function directly to the user interface. The signals associated with the user interface are summarized in Table 3.

Table 3 • User Interface Signals

| Signal | Type | Description |
|-----------|------|-------------------------------------|
| reset | In | Active high – resets all registers |
| xlate | In | 53 / 54-byte cell size control |
| w_avail | In | Active high – user ready to receive |
| w_phy_act | Out | Active high physical selected |
| w_enable | Out | Active high data enable |
| w_adr | Out | 5-bit word count |
| w_data | Out | 16-bit data bus |
| r_avail | In | Active high – user ready to send |
| r_buf_en | Out | Active high read enable |
| r_adr | Out | 5-bit word count |
| r_data | In | 16-bit data bus |

When reset is asserted high, all registers in the CoreU1PHY are cleared. They will remain in this state as long as reset is asserted.

If the xlate input is low, the CoreU1PHY will transfer data to/from the link-layer device as 53-byte ATM cells. On ingress (TX), the CoreU1PHY will duplicate the fifth byte of the ATM header and insert it as the sixth byte (UDF2) in order to create a standard 54-byte ATM cell on the user "write" interface. Conversely, the CoreU1PHY will accept a standard 54-byte cell at the user "read" interface and drop the sixth byte during transfer to the egress (RX) interface. If xlate is high, no translation is performed; 54-byte cells are transferred on all interfaces.

The user interface is divided into write (TX) and read (RX) interfaces. The control signals and data for the write interface are associated with the u1_tx_clk, while control

signals and data for the read interface are associated with the u1_rx_clk.

Each interface is controlled from the user logic by the w_avail and r_avail signals, respectively.

When the cell buffer or user logic is ready to receive or send a cell on either interface, the user must assert x_avail high. In turn, this will cause the CoreU1PHY to assert u1_x_clav to the link-layer device.

Write Interface (ingress)

Whenever the link-layer asserts u1_tx_en low, the w_phy_act signal is asserted high to indicate that the ingress user interface is active. The w_enable signal will remain low until the link-layer begins to transfer a cell. Since the CoreU1PHY translates from 8-bit data at the UTOPIA interface to 16-bit data at the user interface, w_enable is asserted for one clock cycle while a data word is valid. W_adr is incremented on the next rising-edge of u1_tx_clk, and then w_enable is de-asserted for one clock cycle (except during insertion of the UDF2 byte, as shown in Figure 9). W_adr increments from 00 to 1B hex (27 words).

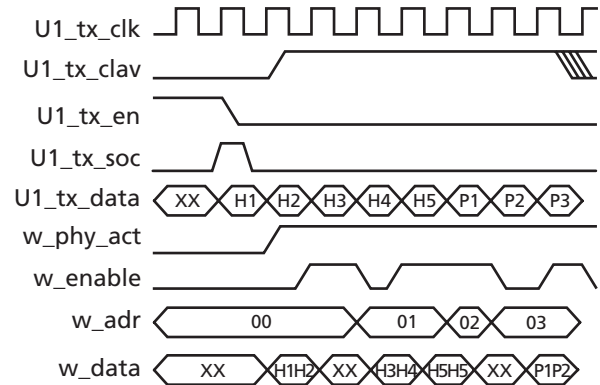


Figure 9 • Write Interface Cell Transfer

If the address resets to 00 hex before reaching 1B hex, the cell transfer was interrupted by the link-layer and the previous bytes of the cell should be dropped. When w_adr reaches 1B hex, a complete 54-byte cell has been received. The w_adr will reset to 00 hex and w_enable is de-asserted until another cell transfer begins. The w_phy_act signal is not de-asserted unless the link-layer deselects the CoreU1PHY by asserting u1_tx_en high.

Read Interface (egress)

When `r_avail` is asserted high at the user interface and the `u1_rx_en` signal is asserted low by the link-layer, the CoreU1PHY will begin accepting data on the user interface. Once a cell transfer has begun, the CoreU1PHY will transfer 27 words of data regardless of the state of `r_avail`. The CoreU1PHY asserts `r_buf_en` high, expecting to accept data at the `r_data` inputs on the next rising-edge of `u1_rx_clk` as illustrated in Figure 10.

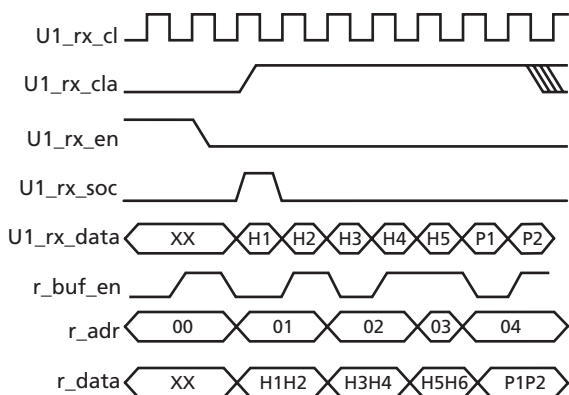


Figure 10 • Read Interface Cell Transfer

The CoreU1PHY provides `r_adr` as a word count (00 to 1B hex) and increments whenever the core accepts data at the `r_data` pins. Since the CoreU1PHY translates from 16-bit data at the user interface to 8-bit data at the UTOPIA interface, `r_buf_en` is asserted for one clock cycle, data is

accepted on the following rising edge of `u1_rx_clk`, and the `r_adr` is incremented.

Then `r_buf_en` is de-asserted for one clock cycle except after the third data word when `xlate` is low (53-byte mode), or when a back-to-back read operation is needed in order to get the first payload byte in time.

The cycle is repeated until `r_adr` reaches 1B hex and the last two bytes of the ATM cell are sent. At this point, `r_adr` is reset to 00 hex, and if `r_avail` indicates that another cell is immediately available, and `u1_rx_en` remains low, the CoreU1PHY will immediately begin sending the next cell as shown in Figure 11. Otherwise, `r_buf_en` remains low until the CoreU1PHY begins to transmit another cell.

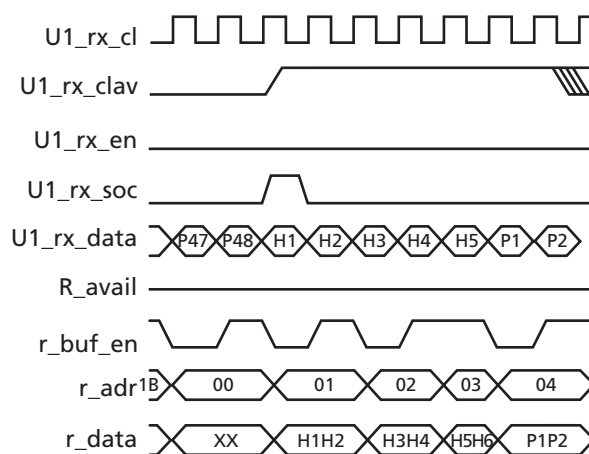


Figure 11 • Back-to-Back Read Cell Transfer

Ordering Information

Order CoreU1PHY through your local Actel sales representative. Use the following numbering convention when ordering: CoreU1PHY-XX, where XX is listed in [Table 4](#).

Table 4 • Ordering Codes

| XX | Description |
|-----------|---|
| EV | Evaluation Version |
| SN | Netlist for single-use on Actel Devices |
| AN | Netlist for unlimited use on Actel devices |
| SR | RTL for single-use on Actel Devices |
| AR | RTL for unlimited use on Actel devices |
| UR | RTL for unlimited use and not restricted to Actel devices |

List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v4.0) | Page |
|------------------|---|------|
| v3.0 | The "Supported Families" section was updated to include Fusion. | 1 |
| | Table 1 was updated to include Fusion data. | 2 |
| v2.0 | The "Supported Families" section was added. | 1 |
| | Table 1 • Device Utilization and Performance was updated. | 2 |

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA

Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom

Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan

www.jp.actel.com

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan

Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong

www.actel.com.cn

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong

Phone +852 2185 6460
Fax +852 2185 6488

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