High Performance RF Transmitter for Narrowband Systems

Applications

- One-way narrowband ultra low power wireless systems with channel spacing down to 6.25 kHz
- 170 / 315 / 433 / 868 / 915 / 920 / 950 MHz ISM/SRD band systems
- Wireless Metering and Wireless Smart Grid (AMR and AMI)
- IEEE 802.15.4g systems
- Home and building automation
- Wireless alarm and security systems
- Industrial monitoring and control
- Wireless healthcare applications
- Wireless sensor networks and Active RFID

Regulations

Suitable for systems targeting compliance with:

Europe	ETSI EN 300 220 ETSI EN 54-25
US	FCC CFR47 Part 15 FCC CFR47 Part 90, 24 and 101
Japan	ARIB RCR STD-T30 ARIB STD-T67 ARIB STD-T108

Key Features

- High performance single chip transmitter
  - Very low phase noise: -111 dBc/Hz at 10 kHz offset
- High spectral efficiency (9.6 kbps in 12.5 kHz channel in compliance with FCC narrowbanding mandate)
- Programmable output power up to +16 dBm with 0.4 dB step size
- Power Supply
  - Wide supply voltage range (2.0 V - 3.6 V)
  - Low current consumption:
    - TX: 45 mA at +14 dBm
  - Power down: 0.3 µA
- Automatic output power ramping
- Configurable data rates: 0 to 200 kbps
- Supported modulation formats: 2-FSK, 2- GFSK, 4-FSK, 4-GFSK, MSK, OOK
- RoHS compliant 5x5mm QFN 32 package

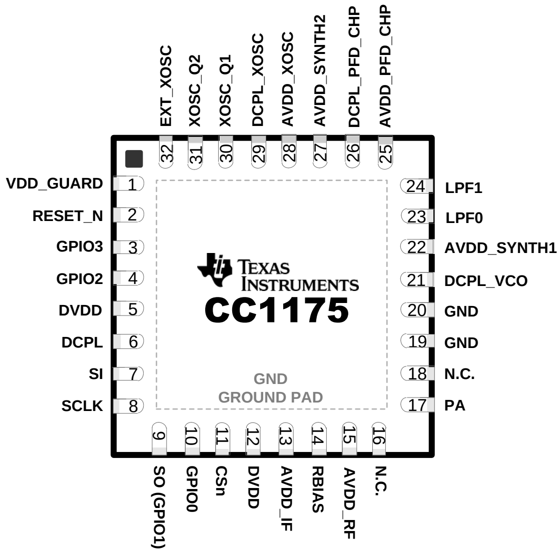
Peripherals and Support Functions

- 128-byte TX FIFO
- TCXO support and control, also in power modes
- Optional Coding Gain feature for increased range and robustness
- Support for seamless integration with the **CC1190** for increased range giving up to +27dBm output power
- Temperature sensor

Description

The **CC1175** is a fully integrated single-chip transmitter designed for high performance at very low power and low voltage operation in cost effective wireless systems. All filters are integrated, removing the need for costly external SAW and IF filters. The device is mainly intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency bands at 164-192 MHz, 274-320 MHz, 410-480 MHz and 820-960 MHz.

The **CC1175** provides extensive hardware support for packet handling, data buffering and burst transmissions. The **CC1175** main operating parameters can be controlled via an SPI interface. In a typical system, the **CC1175** will be used together with a microcontroller and only few external passive components.



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1 Electrical Specifications

All measurements performed on CC1120EM_868_915 rev.1.0.1, CC1120EM_955 rev.1.2.1, CC1120EM_420_470 rev.1.0.1 or CC1120EM_169 rev.1.2

1.1 Absolute Max Ratings

Parameter	Min	Typ	Max	Unit	Condition
Supply Voltage ("VDD")	-0.3		3.9	V	
Storage Temperature Range	-40		125	°C	
ESD			2000	V	HBM
ESD			500	V	CDM
Voltage on Any Digital Pin	-0.3		VDD+0.3 max 3.9	V	
Voltage on Analog Pins (including "DCPL" pins)	-0.3		2.0	V	

1.2 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Voltage Supply Range	2.0		3.6	V	
Temperature Range	-40		85	°C	

1.3 RF Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency Bands	820		960	MHz	
	410		480	MHz	
	274		320	MHz	Please see application note AN115 "*Using the CC112x/CC1175 at 274 to 320 MHz*" for more information
	164		192	MHz	
Frequency Resolution		30		Hz	In 820-960 MHz band
		15		Hz	In 410-480 MHz band
		6		Hz	In 164-192 MHz band
Datarate	0		200	kbps	Packet mode
	0		100	kbps	Transparent mode
Datarate Step Size		1e-4		bps	

1.4 Regulatory Standards

Performance Mode	Frequency Band	Suitable for compliance with	Comments
High Performance Mode	820 – 960 MHz	ARIB T-108 ARIB T-96 ETSI EN 300 220 ETSI EN 54-25 FCC PART 101 FCC PART 24 SUBMASK D FCC PART 15.247 FCC PART 15.249 FCC PART 90 MASK G FCC PART 90 MASK J	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender such as the **CC1190**
	410 – 480 MHz	ARIB T-67 ARIB RCR STD-30 ETSI EN 300 220 FCC PART 90 MASK D FCC PART 90 MASK G	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
	164 – 192 MHz	ETSI EN 300 220 FCC PART 90 MASK D	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
Low Power Mode	820 – 960 MHz	ETSI EN 300 220 FCC PART 15.247 FCC PART 15.249	
	410 – 480 MHz	ETSI EN 300 220	
	164 – 192 MHz	ETSI EN 300 220	

1.5 Current Consumption, Static Modes

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Power Down with Retention		0.3	1	µA	
		0.5		µA	Low-power RC oscillator running
XOFF Mode		170		µA	Crystal oscillator / TCXO disabled
IDLE Mode		1.3		mA	Clock running, system waiting with no radio activity

1.6 Current Consumption, Transmit Modes

950 MHz band (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +10 dBm		37		mA	
TX Current Consumption 0 dBm		26		mA	

868/915/920 MHz bands (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +14 dBm		45		mA	
TX Current Consumption +10 dBm		34		mA	

434 MHz band (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +15 dBm		50		mA	
TX Current Consumption +14 dBm		45		mA	
TX Current Consumption +10 dBm		34		mA	

170 MHz band (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +15 dBm		54		mA	
TX Current Consumption +14 dBm		49		mA	
TX Current Consumption +10 dBm		41		mA	

Low Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +10 dBm		32		mA	

1.7 Transmit Parameters

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Max Output Power		+12		dBm	At 950 MHz
		+14		dBm	At 915/920 MHz
		+15		dBm	At 915/920 MHz with VDD = 3.6 V
		+15		dBm	At 868 MHz
		+16		dBm	At 868 MHz with VDD = 3.6 V
		+15		dBm	At 433 MHz
		+16		dBm	At 433 MHz with VDD = 3.6 V
		+15		dBm	At 170 MHz
		+16		dBm	At 170 MHz with VDD = 3.6 V
Min Output Power		-11		dBm	Within fine step size range
		-40		dBm	Within coarse step size range
Output Power Step Size		0.4		dB	Within fine step size range
Adjacent Channel Power		-75		dBc	4-GFSK 9.6 kbps in 12.5 kHz channel, measured in 100 Hz bandwidth at 434 MHz (FCC Part 90 Mask D compliant)
		-58		dBc	4-GFSK 9.6 kbps in 12.5 kHz channel, measured in 8.75 kHz bandwidth (ETSI 300 220 compliant)
		-61		dBc	2-GFSK 2.4 kbps in 12.5 kHz channel, 1.2 kHz deviation
Spurious Emissions (Not including harmonics)		< -60		dBm	
Harmonics 2nd Harm, 170 MHz 3rd Harm, 170 MHz 2nd Harm, 433 MHz 3rd Harm, 433 MHz 2nd Harm, 450 MHz 3rd Harm, 450 MHz 2nd Harm, 868 MHz 3rd Harm, 868 MHz 2nd Harm, 915 MHz 3rd Harm, 915 MHz 4th Harm, 915 MHz 2nd Harm, 950 MHz 3rd Harm, 950 MHz		 -39 -58 -56 -51 -60 -45 -40 -42 56 52 60 -58 -42		 dBm dBm dBm dBm dBm dBm dBm dBm dBuV/m dBuV/m dBuV/m dBm dBm	Transmission at +14 dBm (or maximum allowed in applicable band where this is less than +14 dBm) using TI reference design Emissions measured according to ARIB T-96 in 950 MHz band, ETSI EN 300-220 in 170, 433 and 868 MHz bands and FCC part 15.247 in 450 and 915 MHz band Fourth harmonic in 915 MHz band will require extra filtering to meet FCC requirements if transmitting in long intervals (>50 ms periods)
Optimum Load Impedance 868 / 915 / 920 MHz bands 433 MHz band 169 MHz band		 35 + j35 55 + j25 80 + j0		 Ω Ω Ω	

1.8 PLL Parameters

High Performance Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Phase Noise in 950 MHz Band		-99		dBc/Hz	± 10 kHz offset
		-99		dBc/Hz	± 100 kHz offset
		-123		dBc/Hz	± 1 MHz offset
Phase Noise in 868/915/920 MHz Bands		-99		dBc/Hz	± 10 kHz offset
		-100		dBc/Hz	± 100 kHz offset
		-122		dBc/Hz	± 1 MHz offset
Phase Noise in 433 MHz Band		-106		dBc/Hz	± 10 kHz offset
		-107		dBc/Hz	± 100 kHz offset
		-127		dBc/Hz	± 1 MHz offset
Phase Noise in 170 MHz Band		-111		dBc/Hz	± 10 kHz offset
		-116		dBc/Hz	± 100 kHz offset
		-135		dBc/Hz	± 1 MHz offset

Low Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Phase Noise in 950 MHz Band		-90		dBc/Hz	± 10 kHz offset
		-92		dBc/Hz	± 100 kHz offset
		-124		dBc/Hz	± 1 MHz offset
Phase Noise in 868/915 MHz Bands		-95		dBc/Hz	± 10 kHz offset
		-95		dBc/Hz	± 100 kHz offset
		-124		dBc/Hz	± 1 MHz offset
Phase Noise in 433 MHz Band		-98		dBc/Hz	± 10 kHz offset
		-102		dBc/Hz	± 100 kHz offset
		-129		dBc/Hz	± 1 MHz offset
Phase Noise in 170 MHz Band		-106		dBc/Hz	± 10 kHz offset
		-110		dBc/Hz	± 100 kHz offset
		-136		dBc/Hz	± 1 MHz offset

1.9 Wake-up and Timing

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Powerdown to IDLE		0.4		ms	Depends on crystal
IDLE to TX		166		µs	Calibration disabled
		461		µs	Calibration enabled
TX to IDLE time		296		µs	Calibrate when leaving TX enabled
		0		µs	Calibrate when leaving TX disabled
Frequency Synthesizer Calibration		0.4		ms	When using SCAL strobe

1.10 High Speed Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Crystal Frequency	32		44	MHz	Note: It is recommended that the crystal frequency is chosen so that the RF channel(s) are >1 MHz away from multiples of XOSC
Load Capacitance (C_L)		10		pF	
ESR			60	Ω	Simulated over operating conditions
Start-up Time		0.4		ms	Depends on crystal

1.11 High Speed Clock Input (TCXO)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Clock Frequency	32		44	MHz	
Clock input amplitude (peak-to-peak)	0.8		VDD	V	Simulated over operating conditions

1.12 32 kHz Clock Input

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Clock Frequency		32		kHz	
32 kHz Clock Input Pin Input High Voltage	0.8×VDD			V	
32 kHz Clock Input Pin Input Low Voltage			0.2×VDD	V	

1.13 Low Speed RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition
Frequency		32/40		kHz	After Calibration (calibrated against the high speed XOSC)
Frequency Accuracy After Calibration		±0.1		%	Relative to frequency reference (i.e. 32 MHz crystal or TCXO)
Initial Calibration Time		1.6		ms	

1.14 I/O and Reset

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Logic Input High Voltage	0.8×VDD			V	
Logic Input Low Voltage			0.2×VDD	V	
Logic Output High Voltage	0.8×VDD			V	At 4 mA output load or less
Logic Output Low Voltage			0.2×VDD	V	
Power-on Reset Threshold		1.3		V	Voltage on DVDD pin

1.15 Temperature Sensor

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Temperature Sensor Range	-40		85	°C	
Temperature Coefficient		2.66		mV / °C	Change in sensor output voltage vs change in temperature
Typical Output Voltage		794		mV	Typical sensor output voltage at T_A = 25°C, VDD = 3.0 V
VDD Coefficient		1.17		mV / V	Change in sensor output voltage vs change in VDD

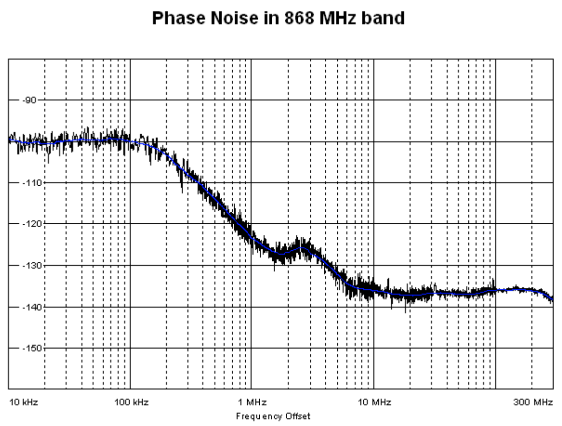
The **CC1175** can be configured to provide a voltage proportional to temperature on GPIO1. Using the information above, the temperature can be estimated by measuring this voltage. Please refer to the **CC1175** user guide for more information.

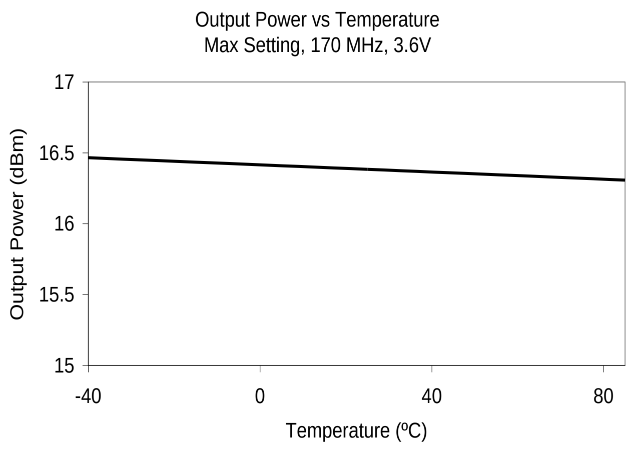
2 Typical Performance Curves

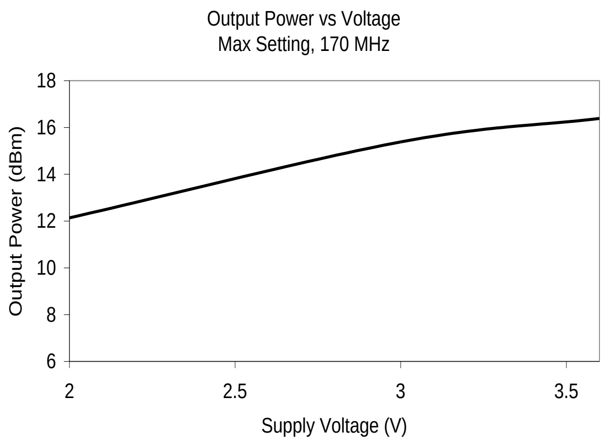
T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

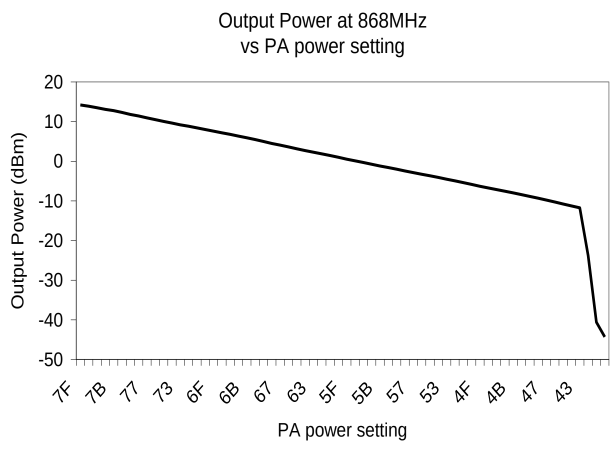
All measurements performed on CC1120EM_868_915 rev.1.0.1, CC1120EM_955 rev.1.2.1, CC1120EM_420_470 rev.1.0.1 or CC1120EM_169 rev.1.2 (f_{xosc} = 32 MHz), and CC1125EM_868_915 rev.1.1.0, CC1125EM_420_470 rev.1.1.0, CC1125EM_169 rev.1.1.0, CC1125EM-Cat1-868 (f_{xosc} = 40 MHz)

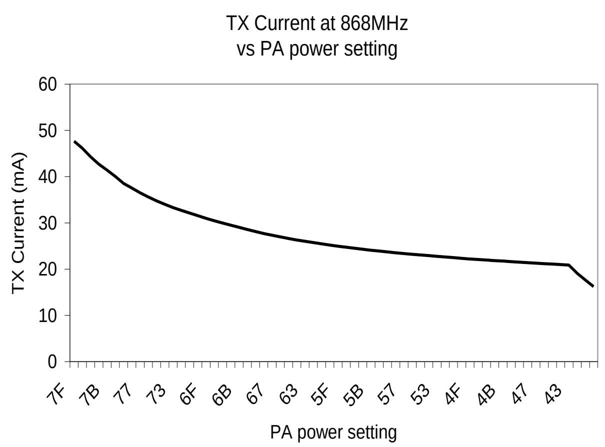
Note that the "output power vs load impedance" plot was measured at the 50 Ω antenna connector

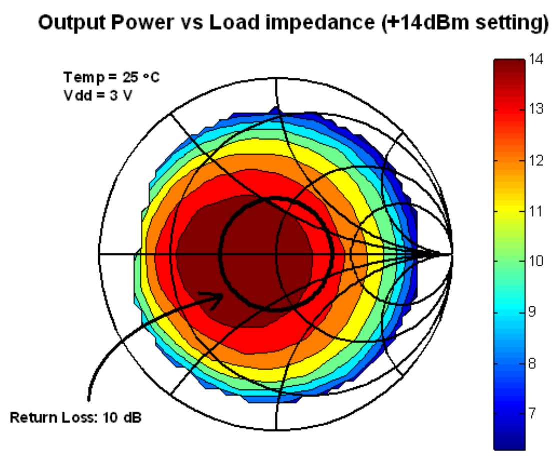


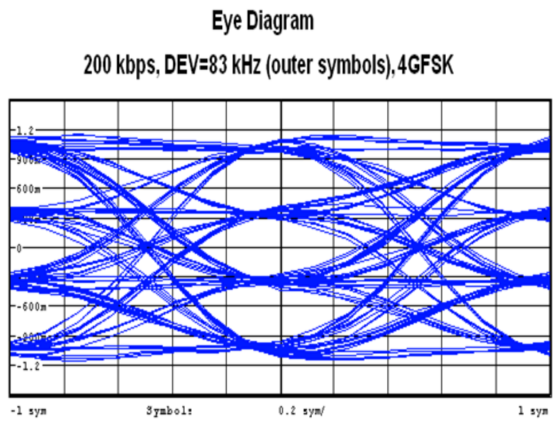


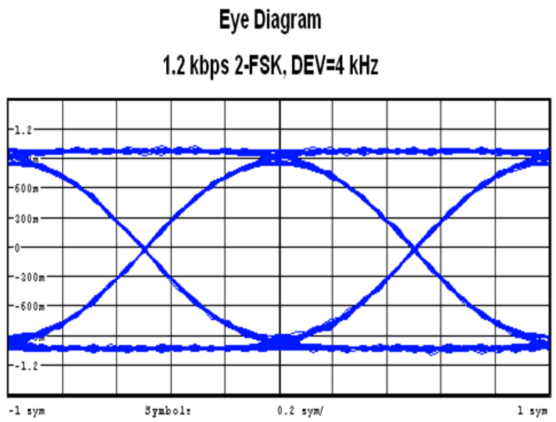


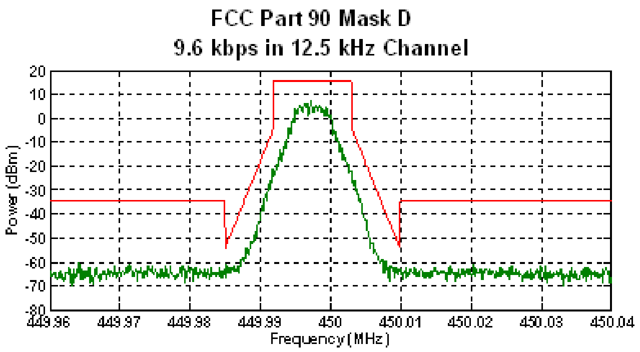


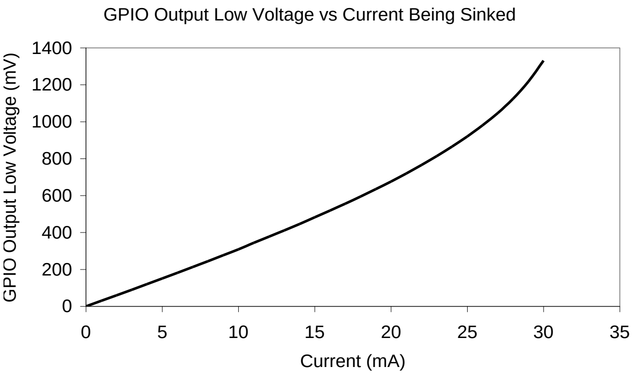


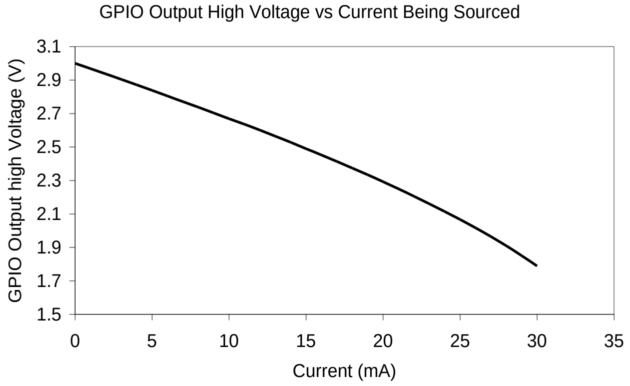



Eye Diagram
200 kbps, DEV=83 kHz (outer symbols), 4GFSK
-1 sym
Symbols
0.2 sym/
1 sym


Eye Diagram
1.2 kbps 2-FSK, DEV=4 kHz
-1 sym
Symbols
0.2 sym/
1 sym


FCC Part 90 Mask D
9.6 kbps in 12.5 kHz Channel
Power (dBm)
Frequency (MHz)


GPIO Output Low Voltage vs Current Being Sinked
GPIO Output Low Voltage (mV)
Current (mA)


GPIO Output High Voltage vs Current Being Sourced
GPIO Output high Voltage (V)
Current (mA)

3 Pin Configuration

The **CC1175** pin-out is shown in the table below.

Pin #	Pin name	Type / direction	Description
1	VDD_GUARD	Power	2.0 - 3.6 V VDD
2	RESET_N	Digital Input	Asynchronous, active-low digital reset
3	GPIO3	Digital Input/Output	General purpose IO
4	GPIO2	Digital Input/Output	General purpose IO
5	DVDD	Power	2.0 - 3.6 VDD to internal digital regulator
6	DCPL	Power	Digital regulator output to external decoupling capacitor
7	SI	Digital Input	Serial data in
8	SCLK	Digital Input	Serial data clock
9	SO(GPIO1)	Digital Input/Output	Serial data out (General purpose IO)
10	GPIO0	Digital Input/Output	General purpose IO
11	CSn	Digital Input	Active-low chip-select
12	DVDD	Power	2.0 - 3.6 V VDD
13	AVDD_IF	Power	2.0 - 3.6 V VDD
14	RBIAS	Analog	External high precision R
15	AVDD_RF	Power	2.0 - 3.6 V VDD
16	NC		Not connected
17	PA	Analog	Single-ended TX output
18	Not connected		
19	GND1	Analog	Analog GND
20	GND0	Analog	Analog GND
21	DCPL_VCO	Power	Pin for external decoupling of VCO supply regulator
22	AVDD_SYNTH1	Power	2.0 - 3.6 V VDD
23	LPF0	Analog	External loopfilter components
24	LPF1	Analog	External loopfilter components
25	AVDD_PFD_CHP	Power	2.0 - 3.6 V VDD
26	DCPL_PFD_CHP	Power	Pin for external decoupling of PFD and CHP regulator
27	AVDD_SYNTH2	Power	2.0 - 3.6 V VDD
28	AVDD_XOSC	Power	2.0 - 3.6 V VDD
29	DCPL_XOSC	Power	Pin for external decoupling of XOSC supply regulator
30	XOSC_Q1	Analog	Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to EXT_XOSC is used)
31	XOSC_Q2	Analog	Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to EXT_XOSC is used)
32	EXT_XOSC	Digital Input	Pin for external XOSC input (must be grounded if a regular XOSC connected to XOSC_Q1 and XOSC_Q2 is used)
-	GND	Ground Pad	The ground pad must be connected to a solid ground plane

4 Block Diagram

A system block diagram of **CC1175** is shown Figure 4.1.

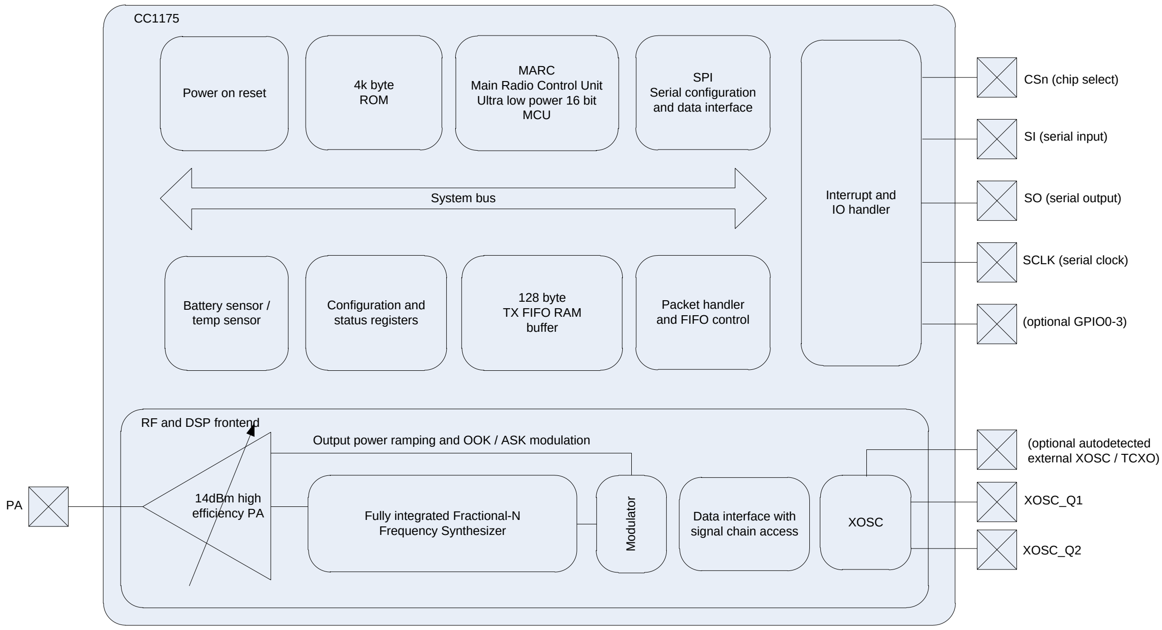


Figure 4.1 : System Block Diagram

4.1 Frequency Synthesizer

At the heart of **CC1175** there is a fully integrated, fractional-N, ultra high performance frequency synthesizer. The frequency synthesizer is designed for excellent phase noise performance. The system is designed to comply with the most stringent regulatory spectral masks at maximum transmit power.

Either a crystal can be connected to XOSC_Q1 and XOSC_Q2, or a TCXO can be connected to the EXT_XOSC input. The oscillator generates the reference frequency for the synthesizer, as well as clocks for the digital part. If a TCXO is used, the **CC1175** will automatically turn the TCXO on and off when needed to support low power modes.

4.2 Transmitter

The **CC1175** transmitter is based on direct synthesis of the RF frequency (in-loop modulation). To achieve effective spectrum usage, **CC1175** has extensive data filtering and shaping in TX to support high throughput data communication in narrowband channels. The modulator also controls power ramping to remove issues such as spectral splattering when driving external high power RF amplifiers.

The modulator also controls the PA power level to support on/off keying (OOK) and amplitude shift keying (ASK).

4.3 Radio Control and User Interface

The **CC1175** digital control system is built around MARC (Main Radio Control) implemented using a high performance 16 bit ultra low power MCU. MARC handles power modes, radio sequencing and protocol timing.

A 4-wire SPI serial interface is used for configuration and data buffer access. The digital baseband includes support for channel configuration, packet handling, and data buffering. The host MCU can burst write data to TX FIFO and stay in power down until the RF packet has been transmitted, greatly reducing the power consumption required from the host MCU.

The **CC1175** radio control and user interface is designed from the widespread sub-GHz **CC1101** transceiver to enable easy SW transition between the two platforms. The command strobes and the main radio states are the same on the two platforms.

For legacy formats **CC1175** also has support for two serial modes. In synchronous serial mode **CC1175** provides the MCU with a bit clock for sampling input data. In transparent mode **CC1175** samples the input pin at a configurable rate.

4.4 Low Power / High Performance Mode

The **CC1175** is highly configurable, enabling trade-offs between power and performance to be made based on the needs of the application. This data sheet describes two modes - low power mode and high performance mode - which represent configurations where the device is optimized for either power or performance.

5 Typical Application Circuit

Very few external components are required for the operation of **CC1175**. A typical application circuit is shown below. Note that it does not show how the board layout should be done, which will greatly influence the RF performance of **CC1175**.

This section is meant as an introduction only. Note that decoupling capacitors for power pins are not shown in the figure below.

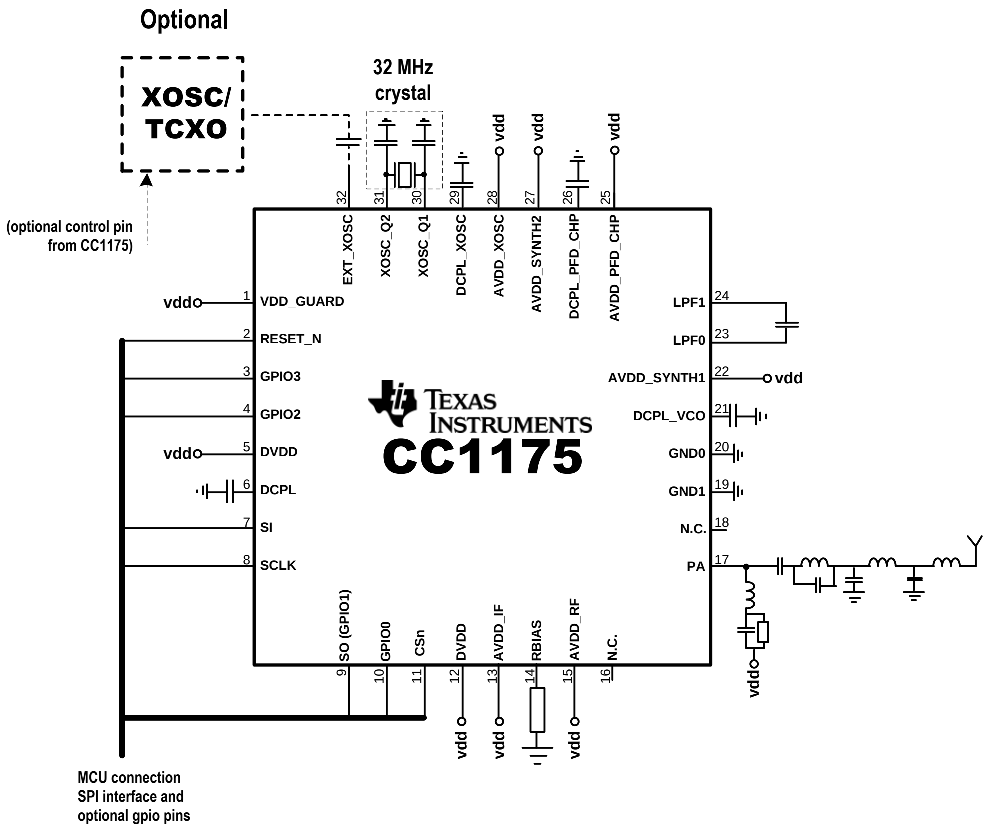


Figure 5.1 : Typical Application Circuit

6 History

Revision	Date	Description / Changes
SWRS116C	March 2013	Added ARIB T-108 to list of regulations Added optimum load impedance Added missing unit "dBm" in output power section Added temperature sensor data Clarified how the typical performance curves have been measured Pin CS_N renamed to CSn to comply with naming convention used in the user guide Added support for higher frequency crystals / external TCXOs Updated typical frequency of low frequency RCOSC to show that it scales with the reference it is calibrated against (i.e. the high speed XOSC) Clarified under max ratings that I/O voltages should not exceed device supply voltage by more than 0.3 V Various minor spelling errors corrected
SWRS116B	April 2012	Added ground pad on page 1 pin-out and pin description Fixed typo in EM list: CC1120EM_420_970 is corrected to CC1120EM_420_470 Added TCXO clock input voltage requirement Changed wording in some sections, and fixed various typos/case errors Added 274 - 320 MHz band and pointed to app note for more info (added mention of 315 MHz band on front page) Removed reflow temperature from abs max ratings Moved ESR to max column Added history section
SWRS116A	Nov. 2011	Initial release

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1175RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1175	Samples
CC1175RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1175	Samples
CC1175RHMR	ACTIVE	VQFN	RHM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1175	Samples
CC1175RHMT	ACTIVE	VQFN	RHM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1175	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

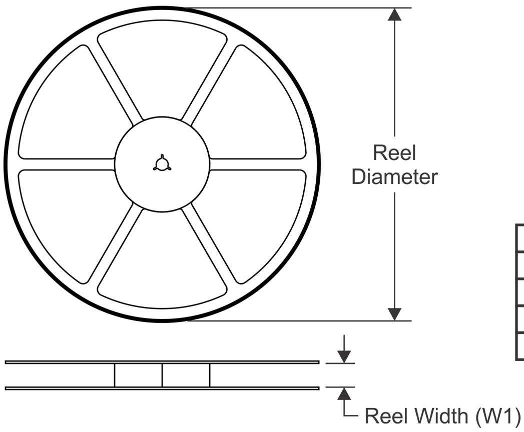
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

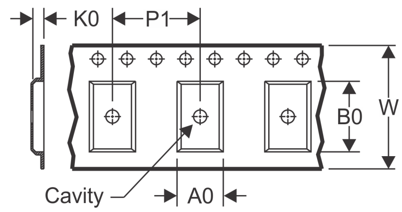
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

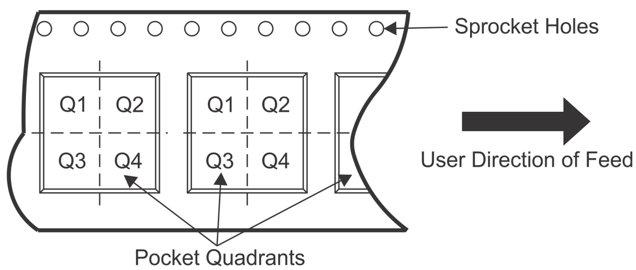


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

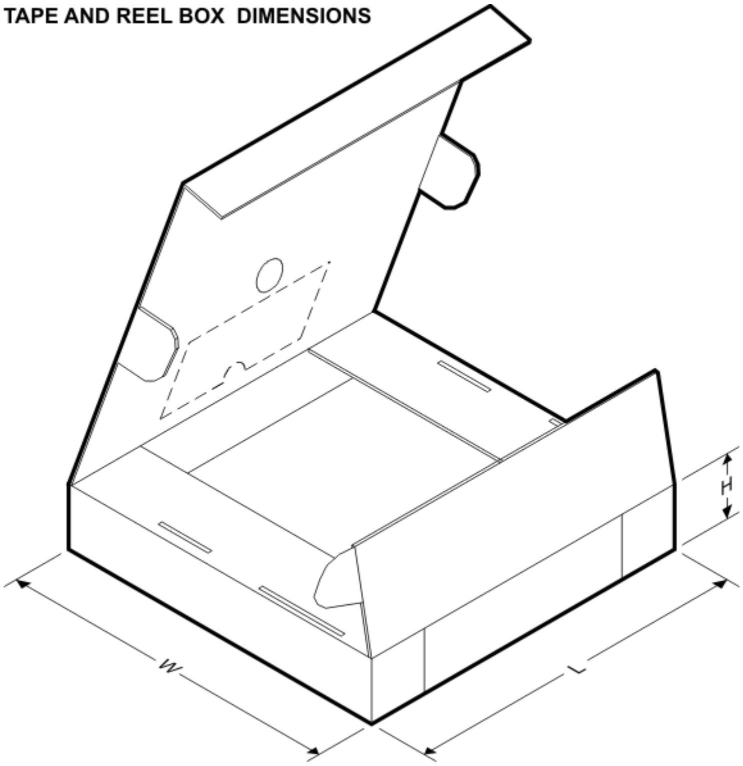
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1175RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CC1175RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

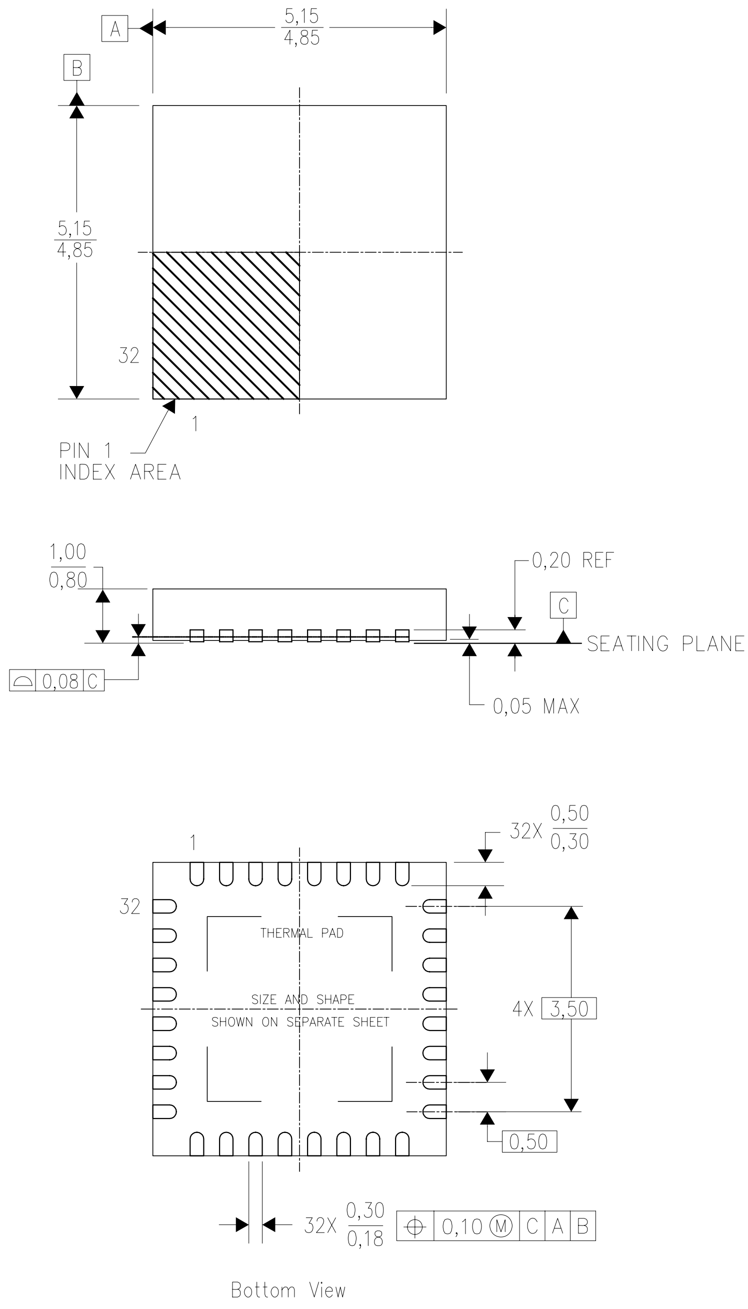
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1175RHBR	VQFN	RHB	32	3000	338.1	338.1	20.6
CC1175RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

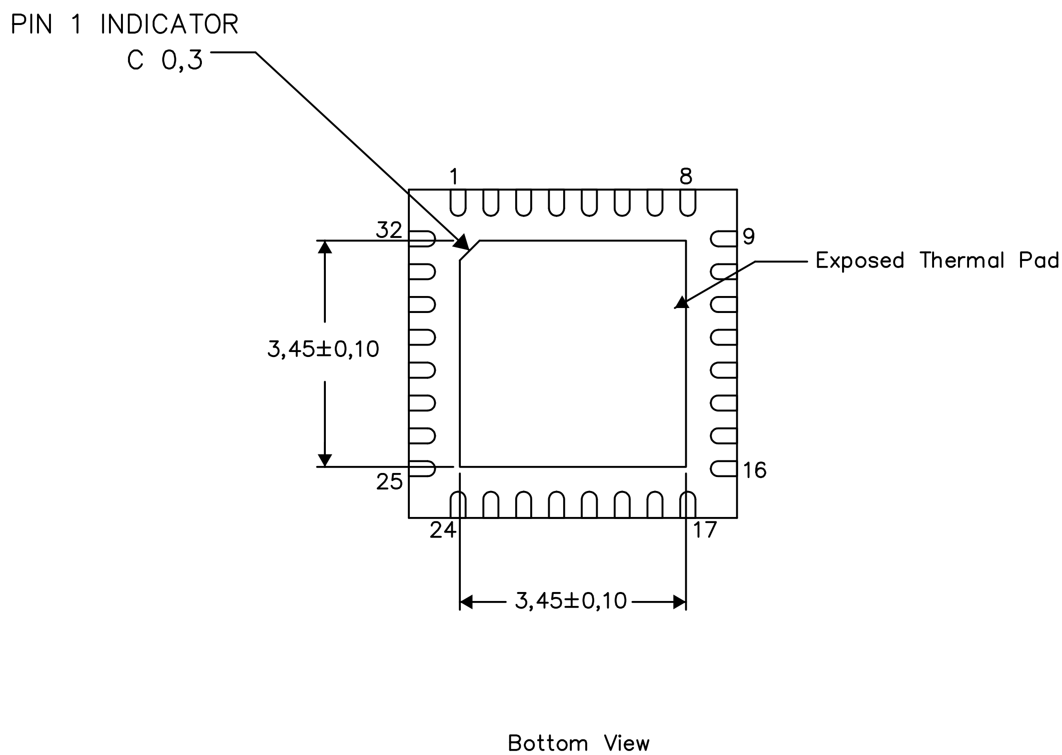
RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

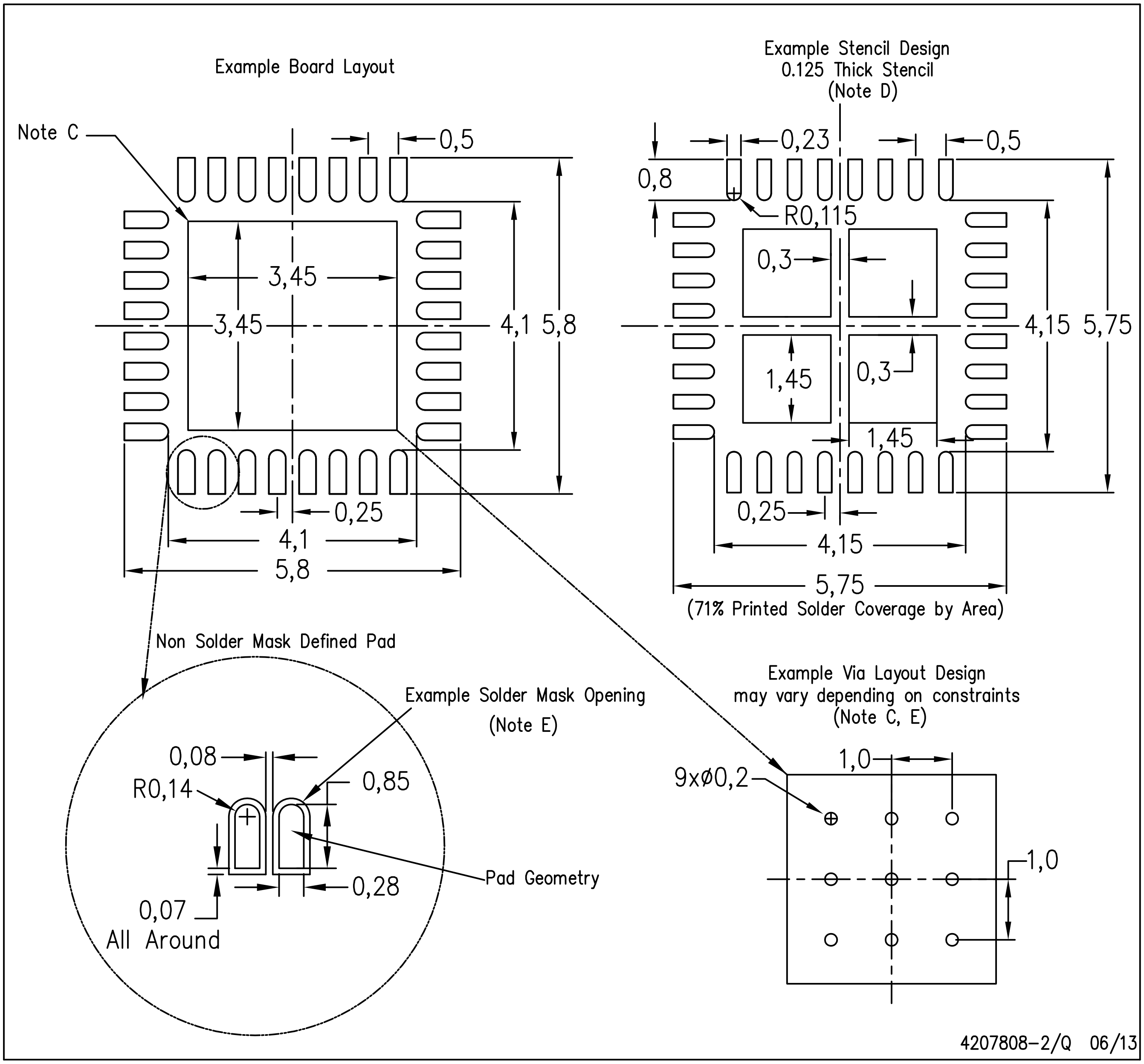


Exposed Thermal Pad Dimensions

4206356-2/Y 06/13

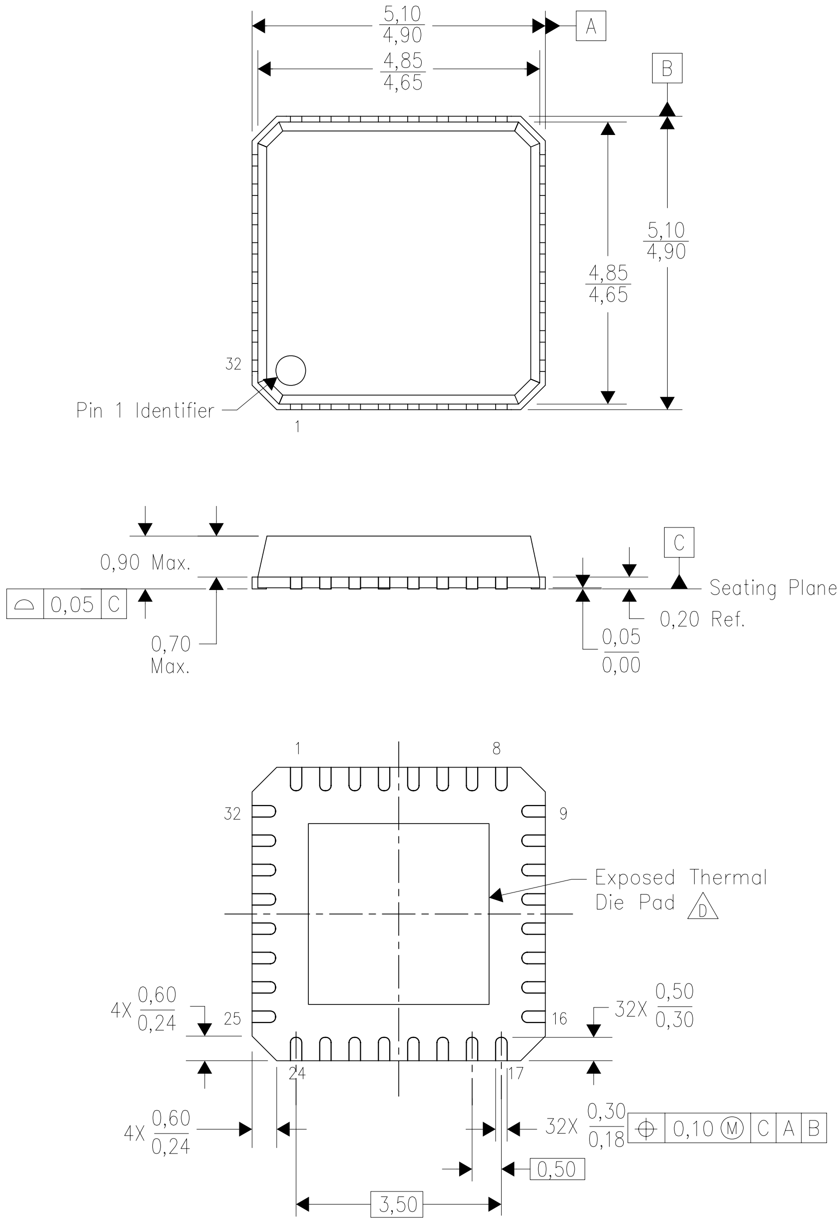
NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RHM (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



4205347/B 04/10

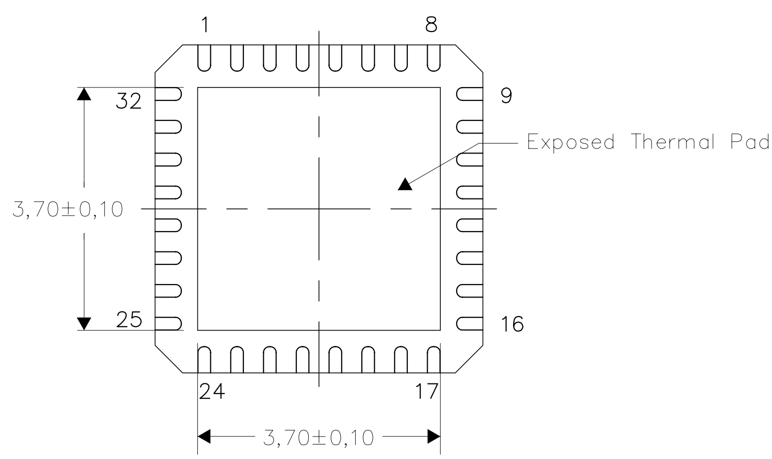
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

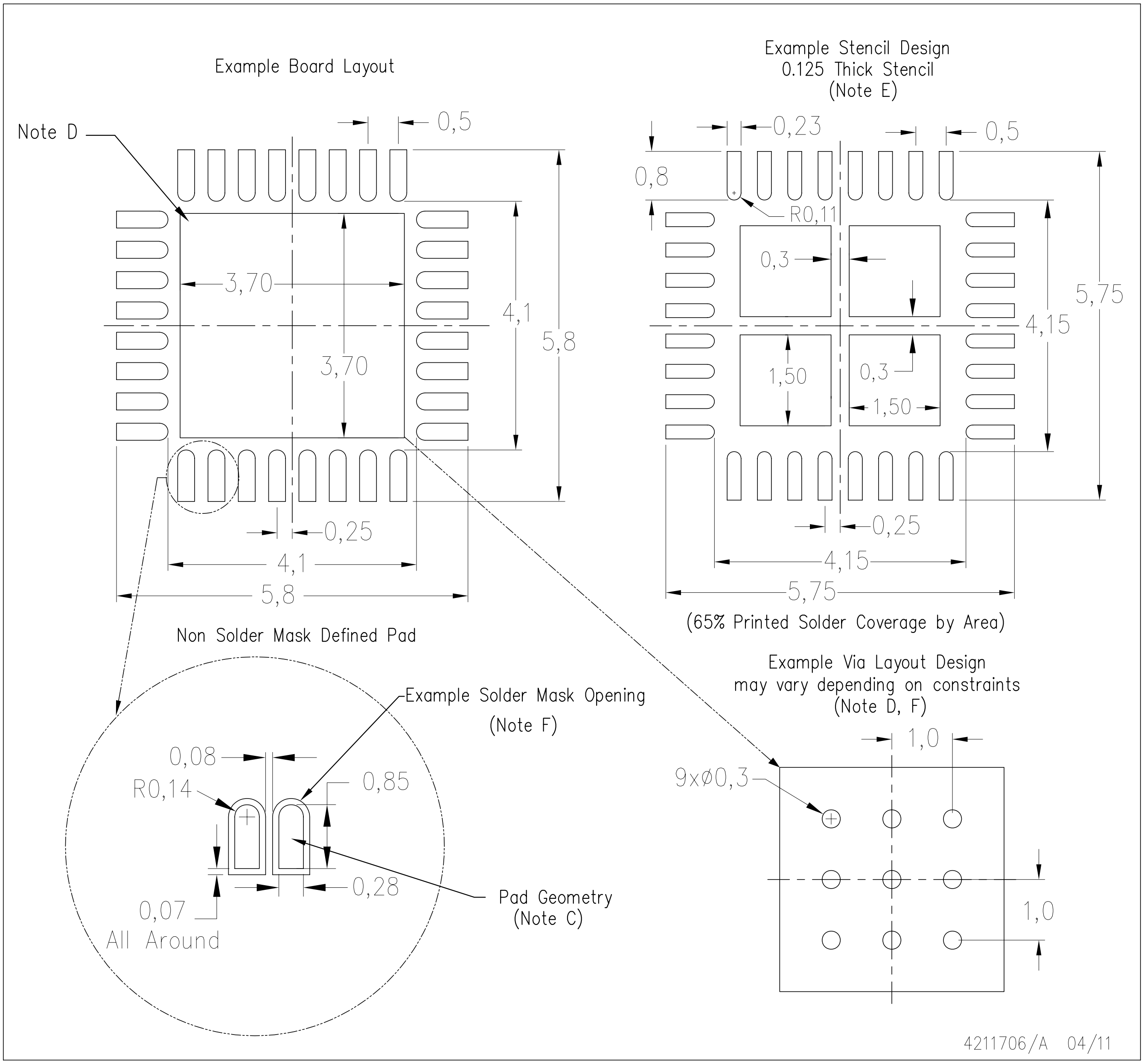


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHM (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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