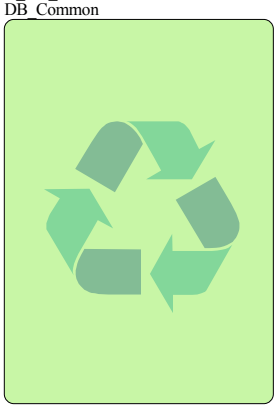
U_DB_Common
DB_Common



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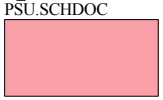
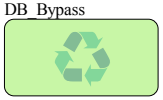
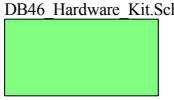
PSU.SCHDOC



U_Bypass_Board
DB_Bypass



U_DB46_Hardware_Kit
DB46_Hardware_Kit.SchDoc



Sheet Title	***DB46 Top Level***	
Project Title	***DB46 - Virtex4 SX35***	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:03 PM	Sheet 1 of 23	
File: DB46_Top.SchDoc		

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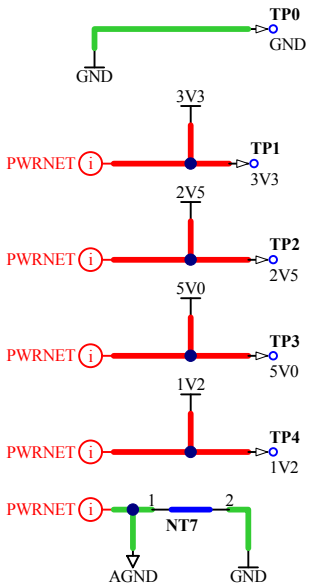

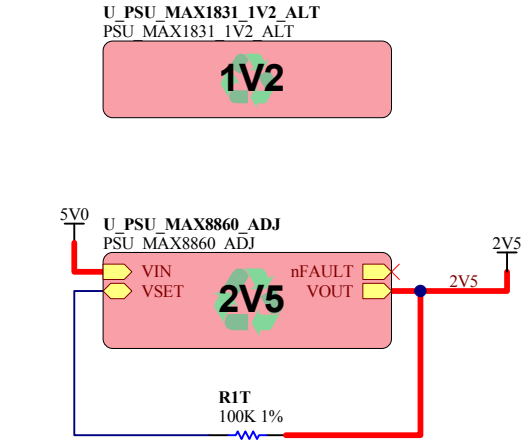

Analog power for the FPGA VCCAUX is set to a nominal 2.5V by the 100K feedback resistor.

Sheet Title	*Power Supply Top Level*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:03 PM	Sheet 2 of 23	
File: PSU.SCHDOC			

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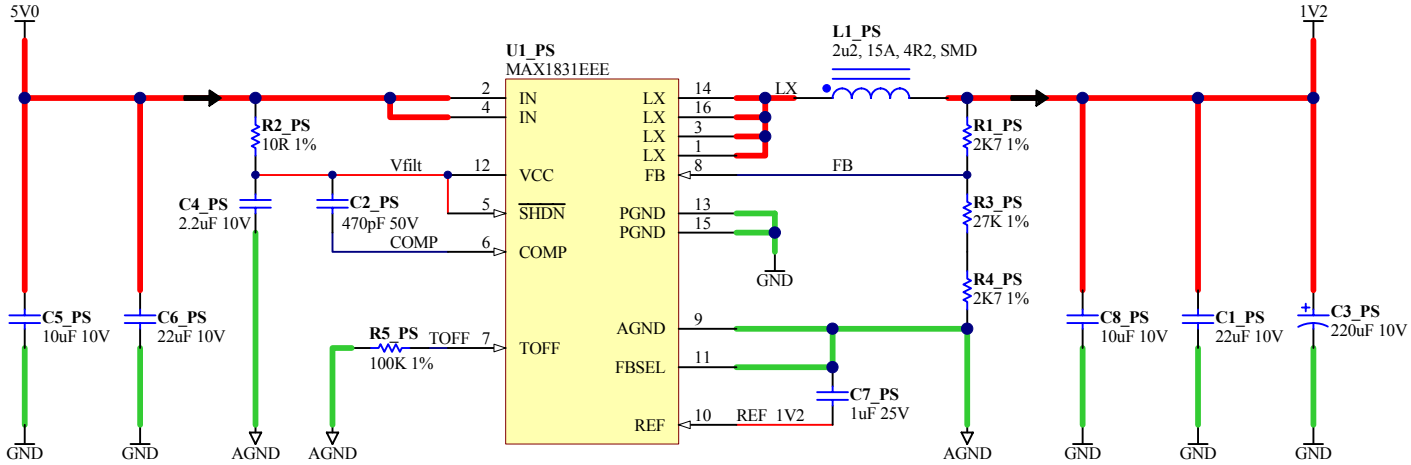

Sheet Title	***Power Supply MAX1831 (1V2)***	
Project Title	***DB46 - Virtex4 SX35***	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 3 of 23
File: PSU_MAX1831_1V2_ALT.SchDoc		

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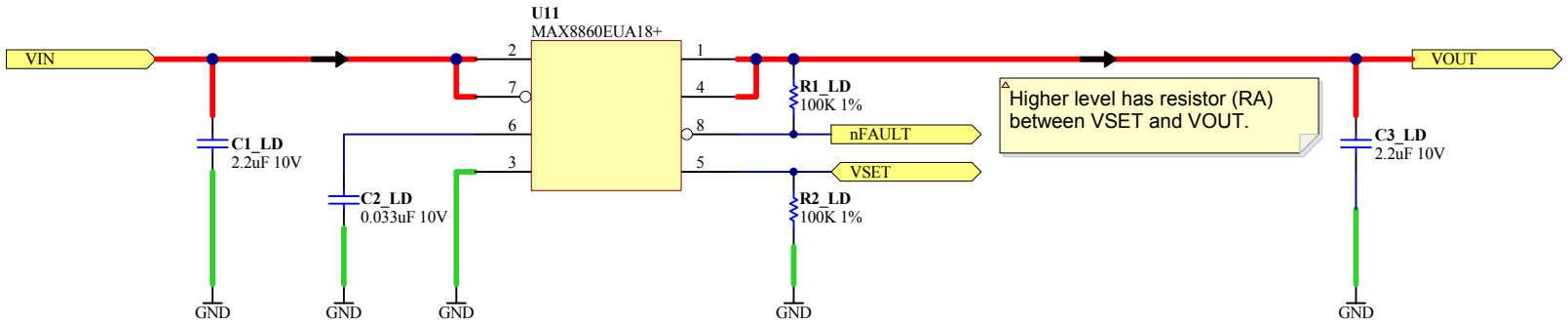

The voltage provided by the MAX8860 linear regulator is determined by the addition of a resistor between VOUT and VSET.

This additional resistor (RA) is located on the higher-level schematic.

The voltage produced by the MAX8860 is calculated as follows:
VOUT = 1.25 * (1 + RA / 100k)

If RA = 20k, VOUT = 1.25 * (1 + 20k/100k) = 1.50 Volts
If RA = 100k, VOUT = 1.25 * (1 + 100k/100k) = 2.50 Volts
If RA = 164k, VOUT = 1.25 * (1 + 164k/100k) = 3.30 Volts

Note that if VSET is grounded (on the higher-level schematic), VOUT=1.8 Volts

Note also that VIN must be a minimum of 0.18 Volts above VOUT.

Sheet Title: *Power Supply MAX8860 (2V5)*		
Project Title: *DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:04 PM		Sheet 4 of 23
File: PSU_MAX8860_ADJ.SchDoc		

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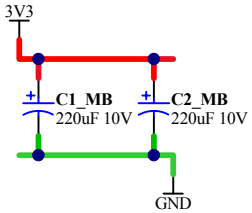

These decoupling capacitors are intended to assist the voltage rails on the PCB - where the decoupling capacitors for the FPGA are not close.

Sheet Title	*Board Bypass Capacitors*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:04 PM	Sheet 5 of 23	
File: DB_Bypass.SchDoc		

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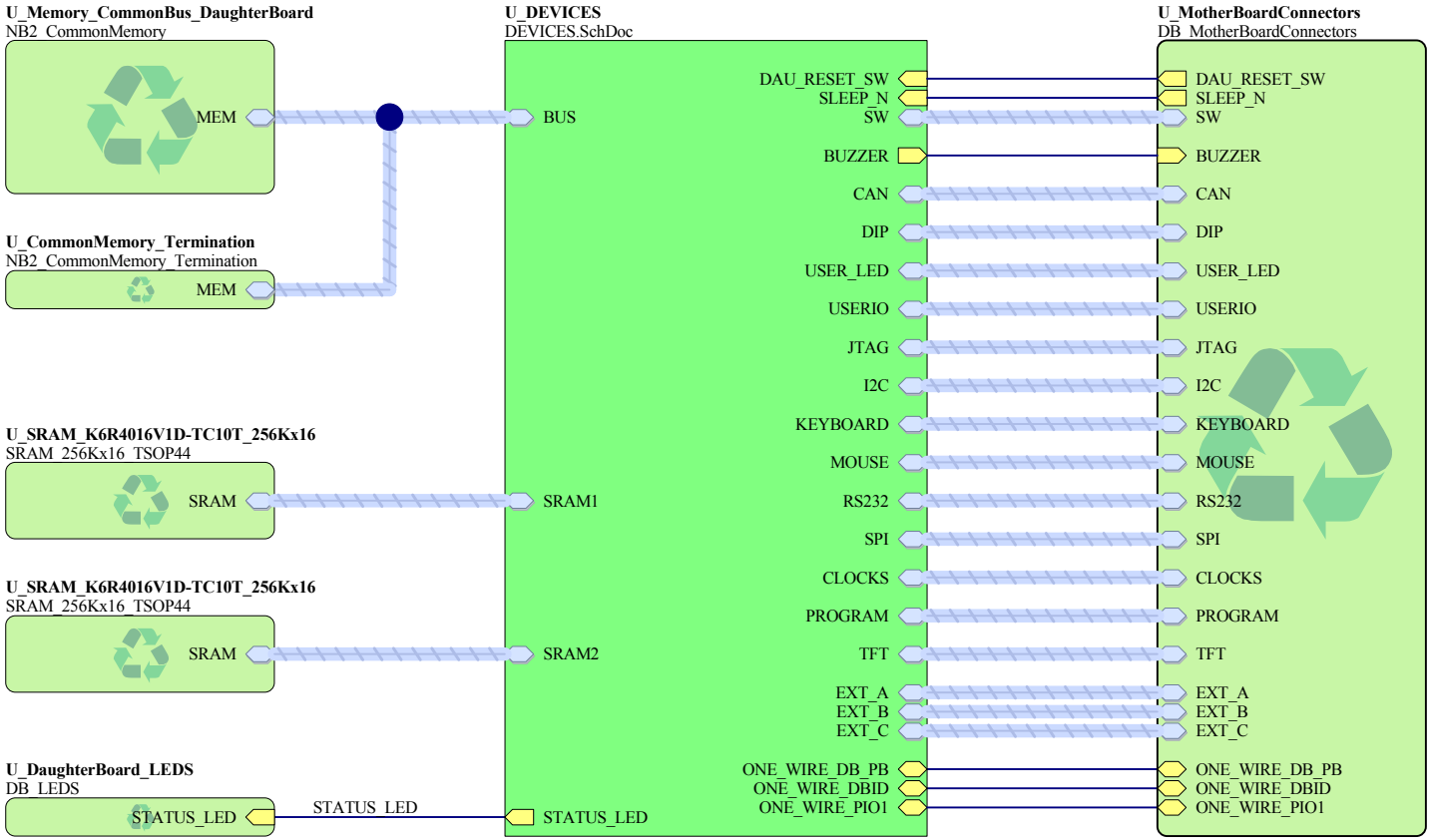
Top Level Schematic For Daughter Board Design
Both FPGA-Only and FPGA + MCU

This Device Sheet is the same for all designs.
It relies on being instantiated in a project that contains a device-specific sheet named DEVICES.SchDoc .



Sheet Title	*Daughter Board Top Level*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:04 PM		Sheet 6 of 23
File: DB_Common.SchDoc		

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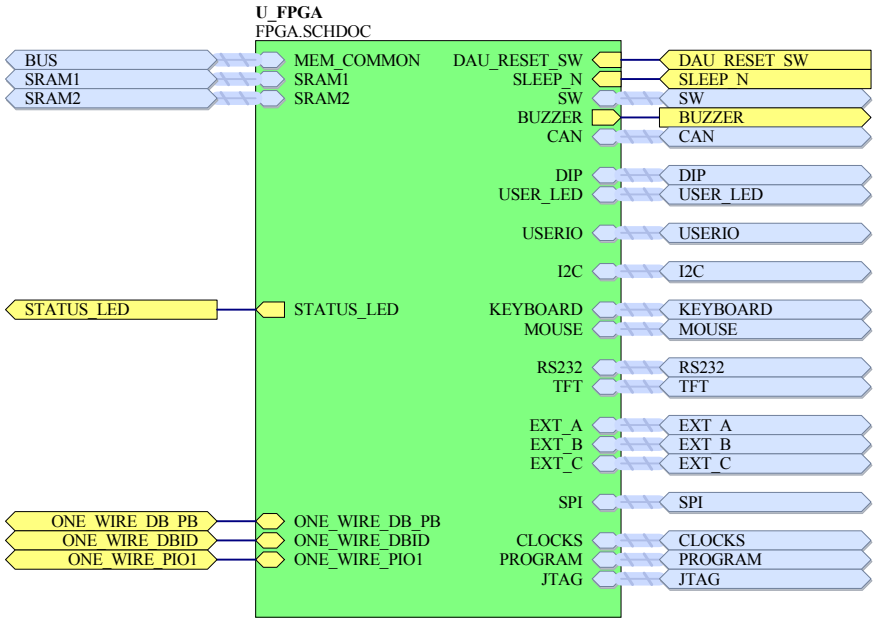

Device Specific Section of Daughter Board Design

This schematic sheet (plus any child sheets) will contain the device specific parts of any daughter board designs.

This will include any FPGA or MCU devices as well as dedicated power supplies, connectors etc.

Sheet Title	*FPGA, LEDs and SRAM Memory*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:04 PM	Sheet 7 of 23	
File: DEVICES.SchDoc		

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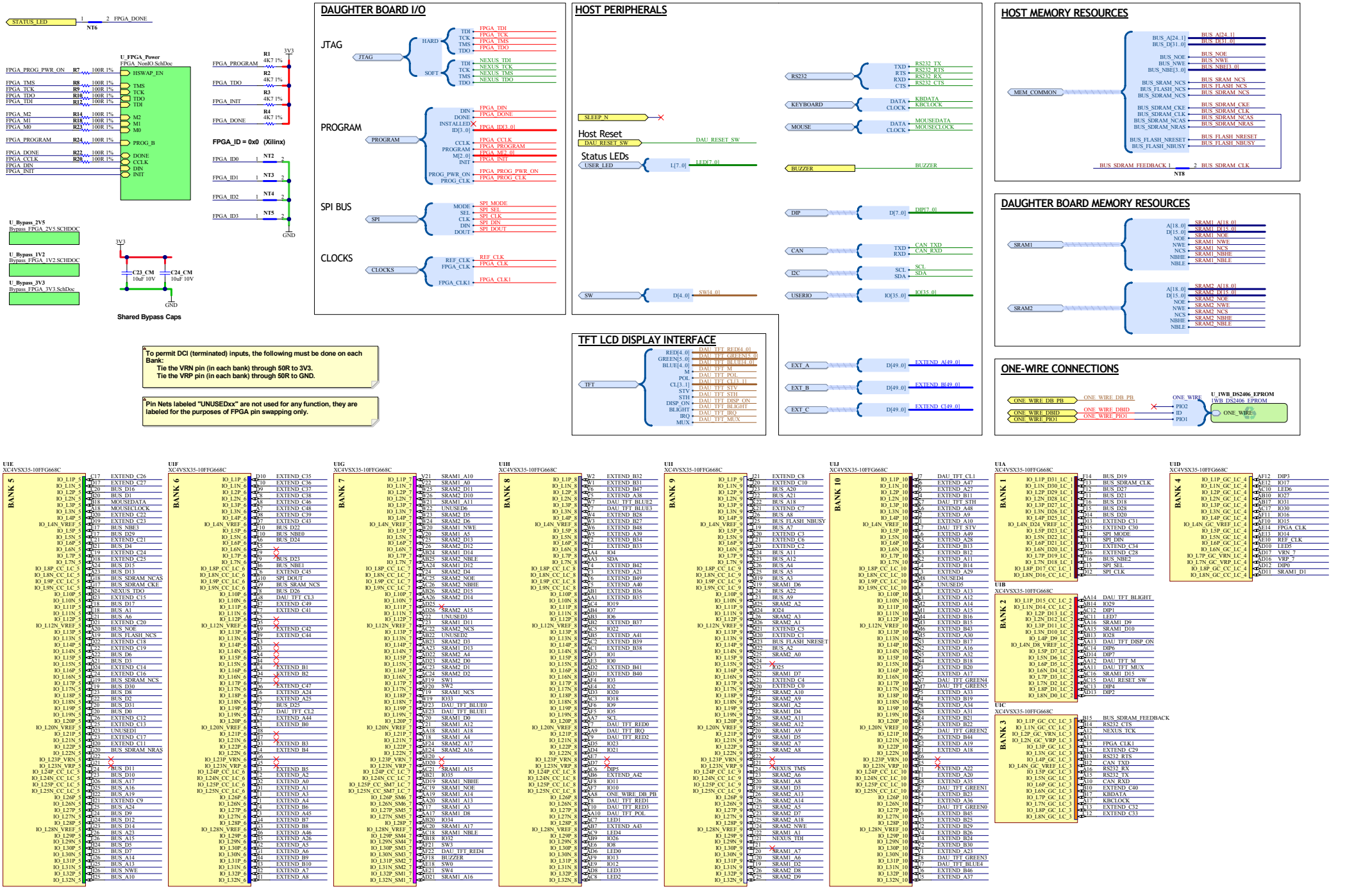
DAUGHTER BOARD I/O
HOST PERIPHERALS
HOST MEMORY RESOURCES
DAUGHTER BOARD MEMORY RESOURCES
ONE-WIRE CONNECTIONS
TFT LCD DISPLAY INTERFACE
JTAG
PROGRAM
SPI BUS
CLOCKS
Host Reset
Status LEDs
RS232
KEYBOARD
MOUSE
BUZZER
DIP
CAN
I2C
USERIO
EXT_A
EXT_B
EXT_C
SRAM1
SRAM2
MEM_COMMON
U_FPGA_Power
FPGA_NonIO.SchDoc
HSWAP_EN
PROG_B
DONE
CCLK
DIN
INIT
M2
M1
M0
TMS
TCK
TDO
TDI
U_Bypass_2V5
Bypass_FPGA_2V5.SCHDOC
U_Bypass_1V2
Bypass_FPGA_1V2.SCHDOC
U_Bypass_3V3
Bypass_FPGA_3V3.SchDoc
Shared Bypass Caps
FPGA_ID = 0x0 (Xilinx)
To permit DCI (terminated) inputs, the following must be done on each Bank:
Tie the VRN pin (in each bank) through 50R to 3V3.
Tie the VRP pin (in each bank) through 50R to GND.
Pin Nets labeled "UNUSEDxx" are not used for any function, they are labeled for the purposes of FPGA pin swapping only.
U1E
U1F
U1G
U1H
U1I
U1J
U1A
U1B
U1C
U1D
BANK 5
BANK 6
BANK 7
BANK 8
BANK 9
BANK 10
BANK 1
BANK 2
BANK 3
BANK 4
XC4VSX35-10FFG668C
Sheet Title FPGA Connections
Project Title DB46 - Virtex4 SX35
Size: A2
Assy: D-820-0031
Revision:02
Date: 27/11/2008
Time: 4:51:04 PM
Sheet 8 of 23
File: FPGA.SCHDOC
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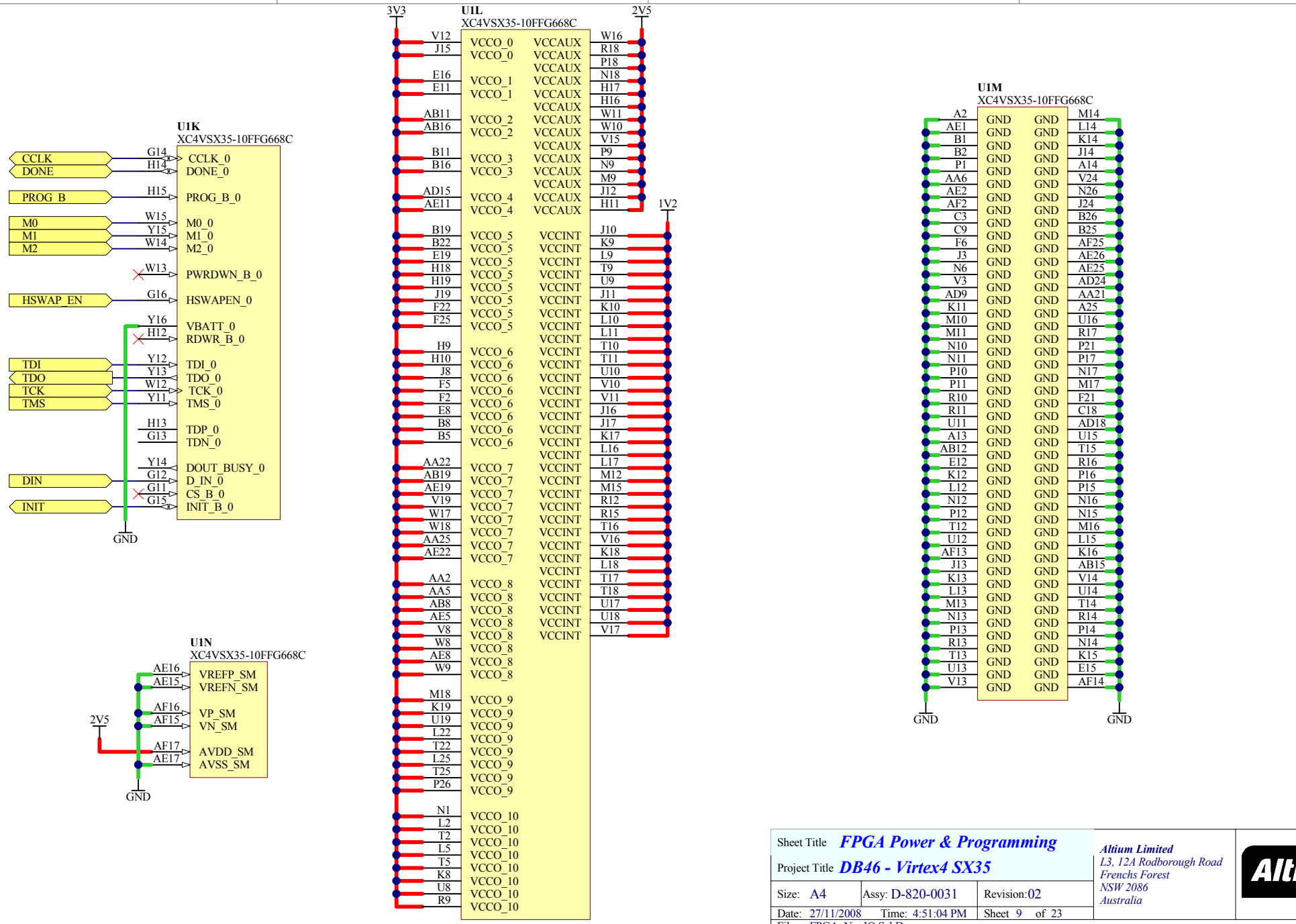
U1K
XC4VSX35-10FFG668C
CCLK
DONE
PROG_B
M0
M1
M2
HSWAP_EN
TDI
TDO
TCK
TMS
DIN
INIT
G14 CCLK_0
H14 DONE_0
H15 PROG_B_0
W15 M0_0
Y15 M1_0
W14 M2_0
W13 PWRDWN_B_0
G16 HSWAPEN_0
Y16 VBATT_0
H12 RDWR_B_0
Y12 TDI_0
Y13 TDO_0
W12 TCK_0
Y11 TMS_0
H13 TDP_0
G13 TDN_0
Y14 DOUT_BUSY_0
G12 D_IN_0
G11 CS_B_0
G15 INIT_B_0
GND
U1N
XC4VSX35-10FFG668C
2V5
AE16 VREFP_SM
AE15 VREFN_SM
AF16 VP_SM
AF15 VN_SM
AF17 AVDD_SM
AE17 AVSS_SM
GND
3V3
U1L
XC4VSX35-10FFG668C
2V5
1V2
V12 VCCO_0
J15 VCCO_0
E16 VCCO_1
E11 VCCO_1
AB11 VCCO_2
AB16 VCCO_2
B11 VCCO_3
B16 VCCO_3
AD15 VCCO_4
AE11 VCCO_4
B19 VCCO_5
B22 VCCO_5
E19 VCCO_5
H18 VCCO_5
H19 VCCO_5
J19 VCCO_5
F22 VCCO_5
F25 VCCO_5
H9 VCCO_6
H10 VCCO_6
J8 VCCO_6
F5 VCCO_6
F2 VCCO_6
E8 VCCO_6
B8 VCCO_6
B5 VCCO_6
AA22 VCCO_7
AB19 VCCO_7
AE19 VCCO_7
V19 VCCO_7
W17 VCCO_7
W18 VCCO_7
AA25 VCCO_7
AE22 VCCO_7
AA2 VCCO_8
AA5 VCCO_8
AB8 VCCO_8
AE5 VCCO_8
V8 VCCO_8
W8 VCCO_8
AE8 VCCO_8
W9 VCCO_8
M18 VCCO_9
K19 VCCO_9
U19 VCCO_9
L22 VCCO_9
T22 VCCO_9
L25 VCCO_9
T25 VCCO_9
P26 VCCO_9
N1 VCCO_10
L2 VCCO_10
T2 VCCO_10
L5 VCCO_10
T5 VCCO_10
K8 VCCO_10
U8 VCCO_10
R9 VCCO_10
VCCAUX
W16 VCCAUX
R18 VCCAUX
P18 VCCAUX
N18 VCCAUX
H17 VCCAUX
H16 VCCAUX
W11 VCCAUX
W10 VCCAUX
V15 VCCAUX
P9 VCCAUX
N9 VCCAUX
M9 VCCAUX
J12 VCCAUX
H11 VCCAUX
VCCINT
J10 VCCINT
K9 VCCINT
L9 VCCINT
T9 VCCINT
U9 VCCINT
J11 VCCINT
K10 VCCINT
L10 VCCINT
L11 VCCINT
T10 VCCINT
T11 VCCINT
U10 VCCINT
V10 VCCINT
V11 VCCINT
J16 VCCINT
J17 VCCINT
K17 VCCINT
L16 VCCINT
L17 VCCINT
M12 VCCINT
M15 VCCINT
R12 VCCINT
R15 VCCINT
T16 VCCINT
V16 VCCINT
K18 VCCINT
L18 VCCINT
T17 VCCINT
T18 VCCINT
U17 VCCINT
U18 VCCINT
V17 VCCINT
U1M
XC4VSX35-10FFG668C
GND
A2 GND
AE1 GND
B1 GND
B2 GND
P1 GND
AA6 GND
AE2 GND
AF2 GND
C3 GND
C9 GND
F6 GND
J3 GND
N6 GND
V3 GND
AD9 GND
K11 GND
M10 GND
M11 GND
N10 GND
N11 GND
P10 GND
P11 GND
R10 GND
R11 GND
U11 GND
A13 GND
AB12 GND
E12 GND
K12 GND
L12 GND
N12 GND
P12 GND
T12 GND
U12 GND
AF13 GND
J13 GND
K13 GND
L13 GND
M13 GND
N13 GND
P13 GND
R13 GND
T13 GND
U13 GND
V13 GND
GND M14
GND L14
GND K14
GND J14
GND A14
GND V24
GND N26
GND J24
GND B26
GND B25
GND AF25
GND AE26
GND AE25
GND AD24
GND AA21
GND A25
GND U16
GND R17
GND P21
GND P17
GND N17
GND M17
GND F21
GND C18
GND AD18
GND U15
GND T15
GND R16
GND P16
GND P15
GND N16
GND N15
GND M16
GND L15
GND K16
GND AB15
GND V14
GND U14
GND T14
GND R14
GND P14
GND N14
GND K15
GND E15
GND AF14
GND
GND
Sheet Title FPGA Power & Programming
Project Title DB46 - Virtex4 SX35
Size: A4
Assy: D-820-0031
Revision: 02
Date: 27/11/2008
Time: 4:51:04 PM
Sheet 9 of 23
File: FPGA_NonIO.SchDoc
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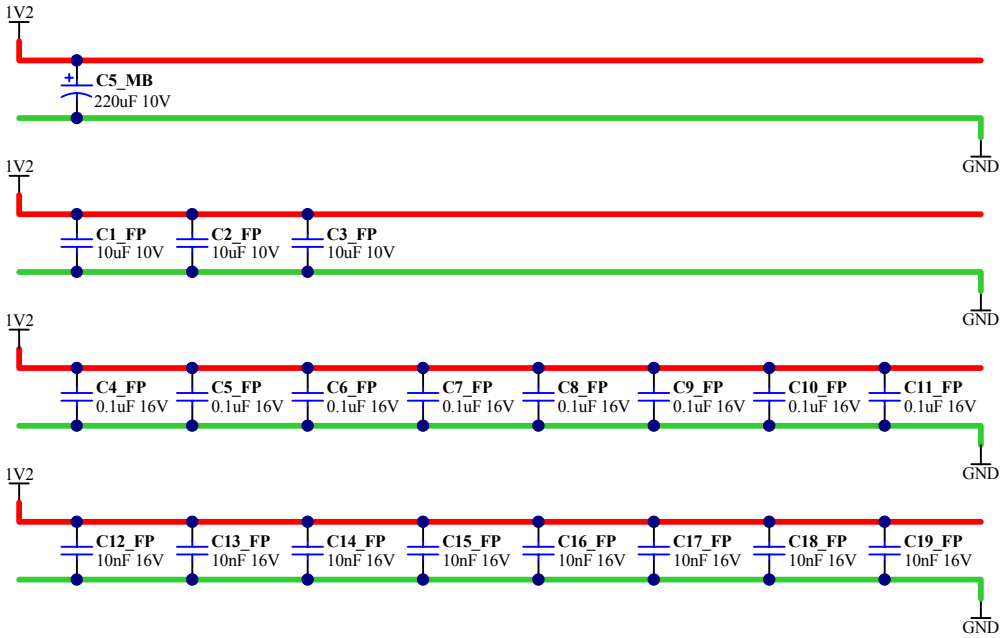

Sheet Title	***FPGA Bypass Capacitors for 1V2***		
Project Title	***DB46 - Virtex4 SX35***		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 10 of 23	
File: Bypass_FPGA_1V2.SCHDOC			

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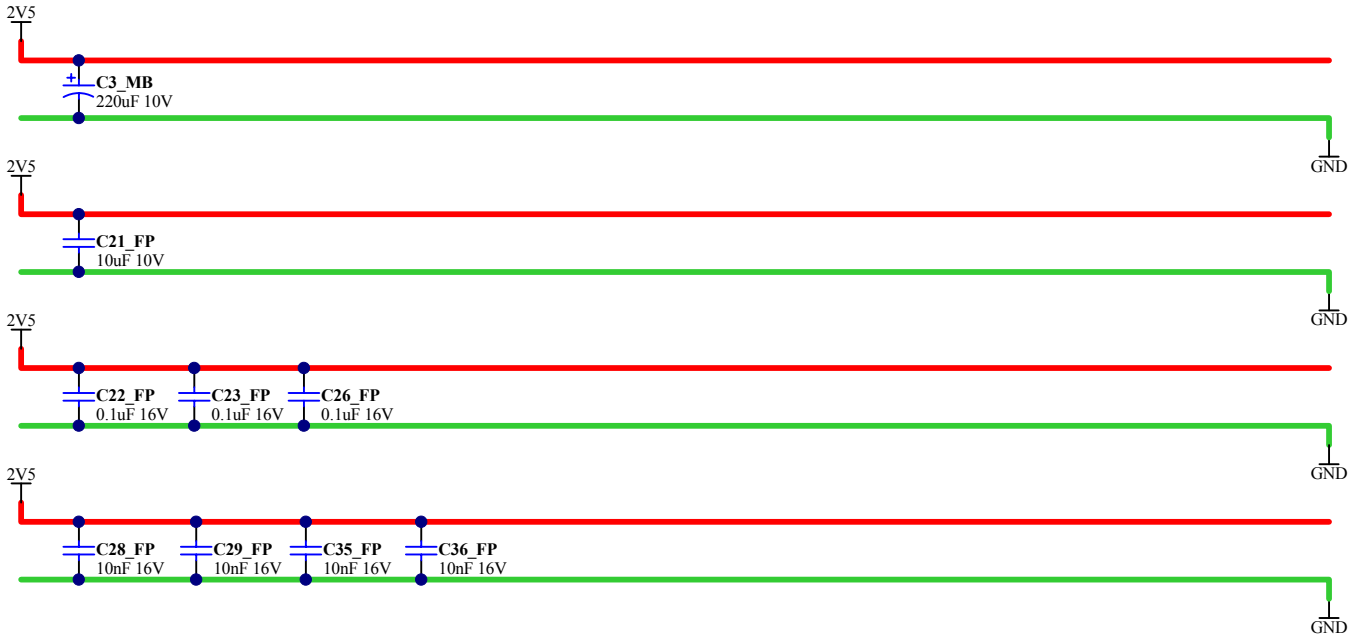

Sheet Title	*FPGA Bypass Capacitors for 2V5*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 11 of 23	
File: Bypass_FPGA_2V5.SCHDOC			

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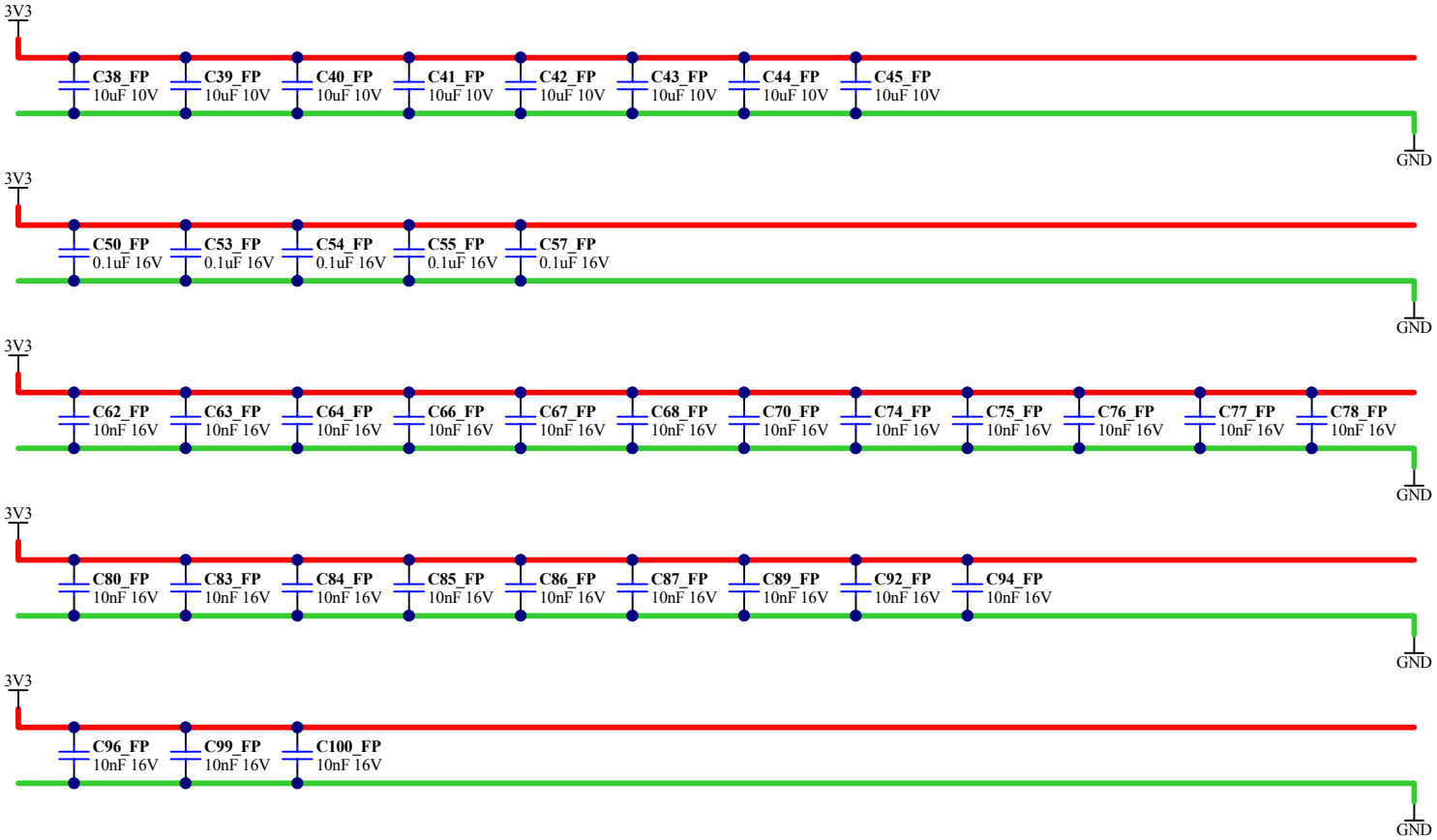

Sheet Title	***FPGA Bypass Capacitors for 3V3***		
Project Title	***DB46 - Virtex4 SX35***		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 12 of 23	
File: Bypass_FPGA_3V3.SchDoc			

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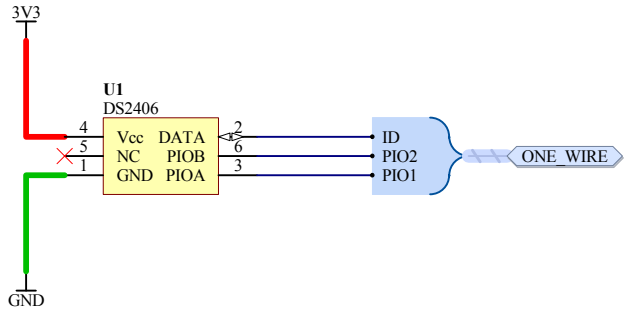

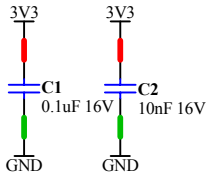

Sheet Title *1-Wire Bus ID*		
Project Title *DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:04 PM		Sheet 13 of 23
File: 1WB_DS2406_EPROM.SchDoc		

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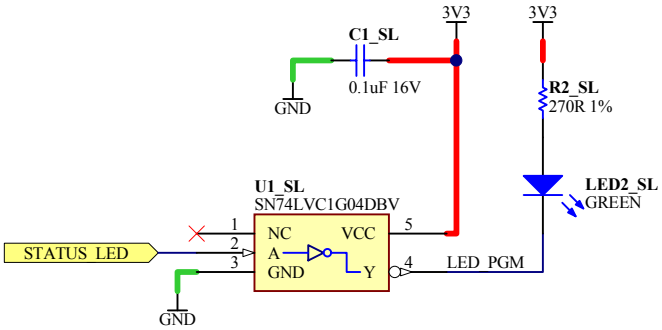
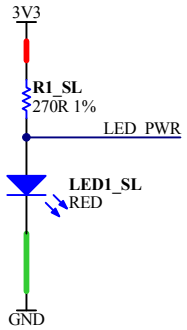
STATUS LED



POWER LED



Sheet Title	*Daughter Board LEDs*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 14 of 23
File: DB_LEDS.SchDoc		

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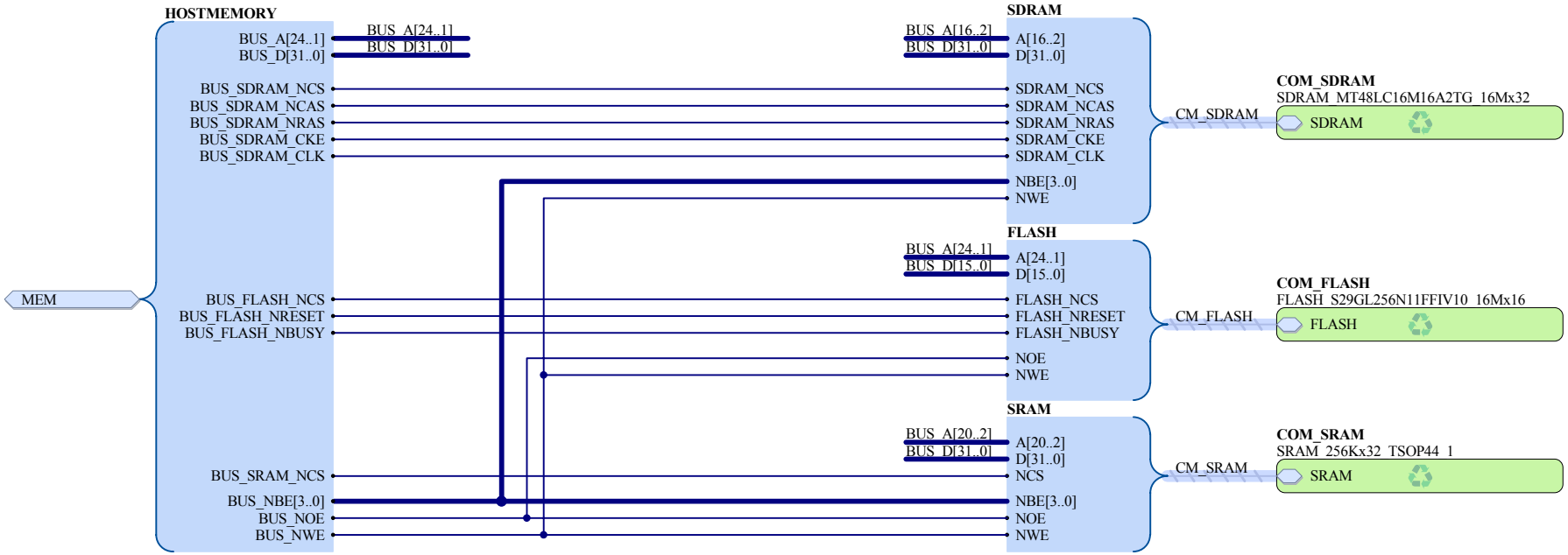

Common-Bus Memory Block

256K x 32-bit SRAM (1 MByte)
16M x 32-Bit SDRAM (64 MByte)
16M x 16-Bit Flash (32 MByte)

Sheet Title	*Common-Bus Memory Block*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 15 of 23
File: NB2_CommonMemory.SchDoc		

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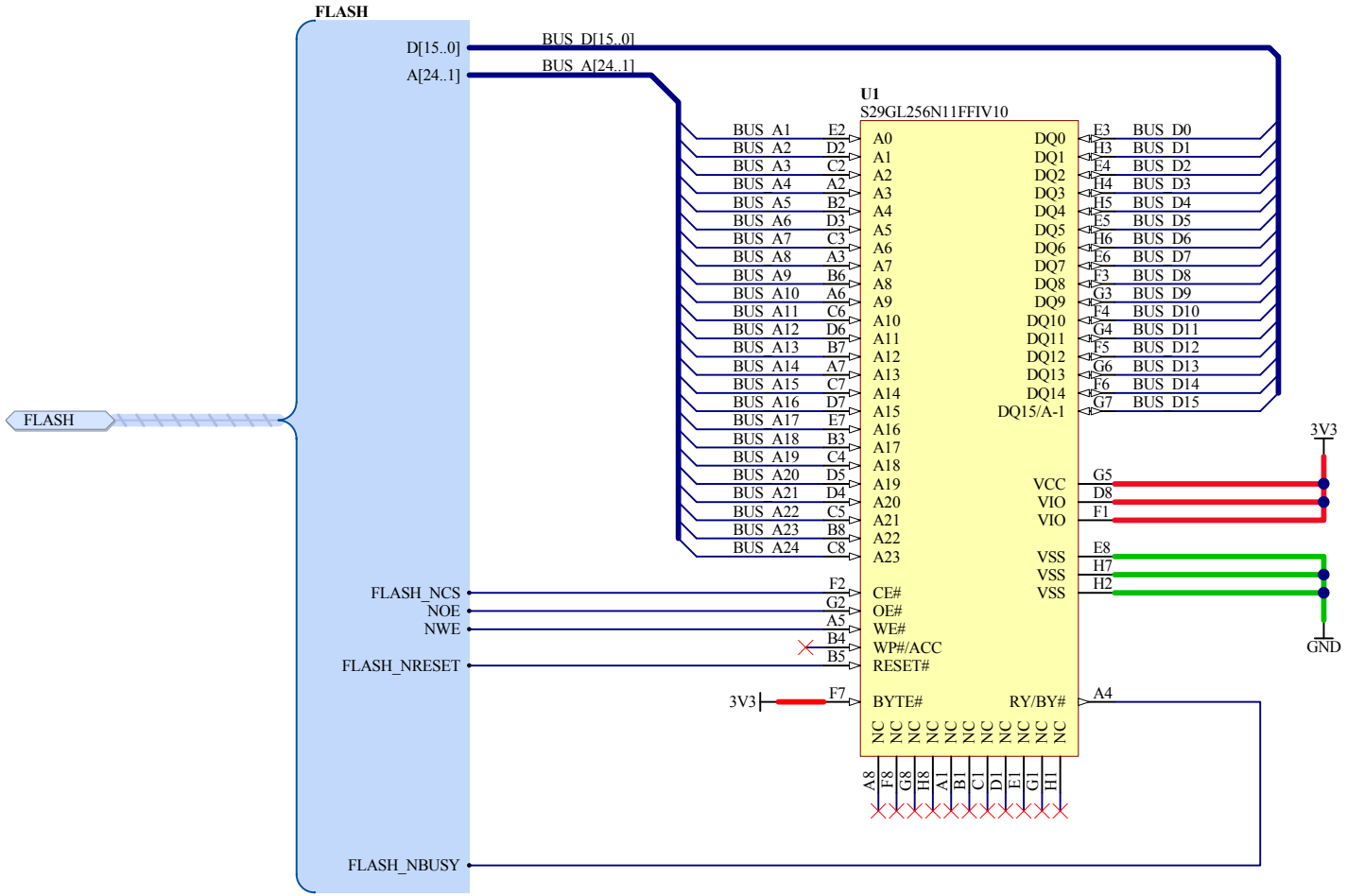

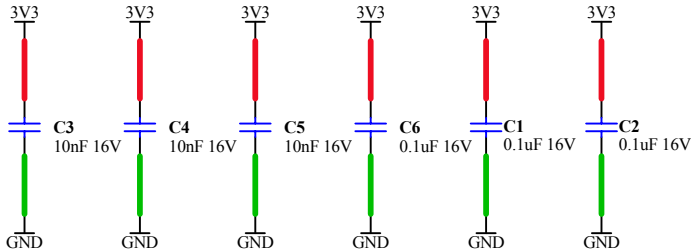

Sheet Title	*16M x 16 Flash Memory (BGA)*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 16 of 23
File: FLASH_S29GL256N11FFIV10_16Mx16.SchDoc		

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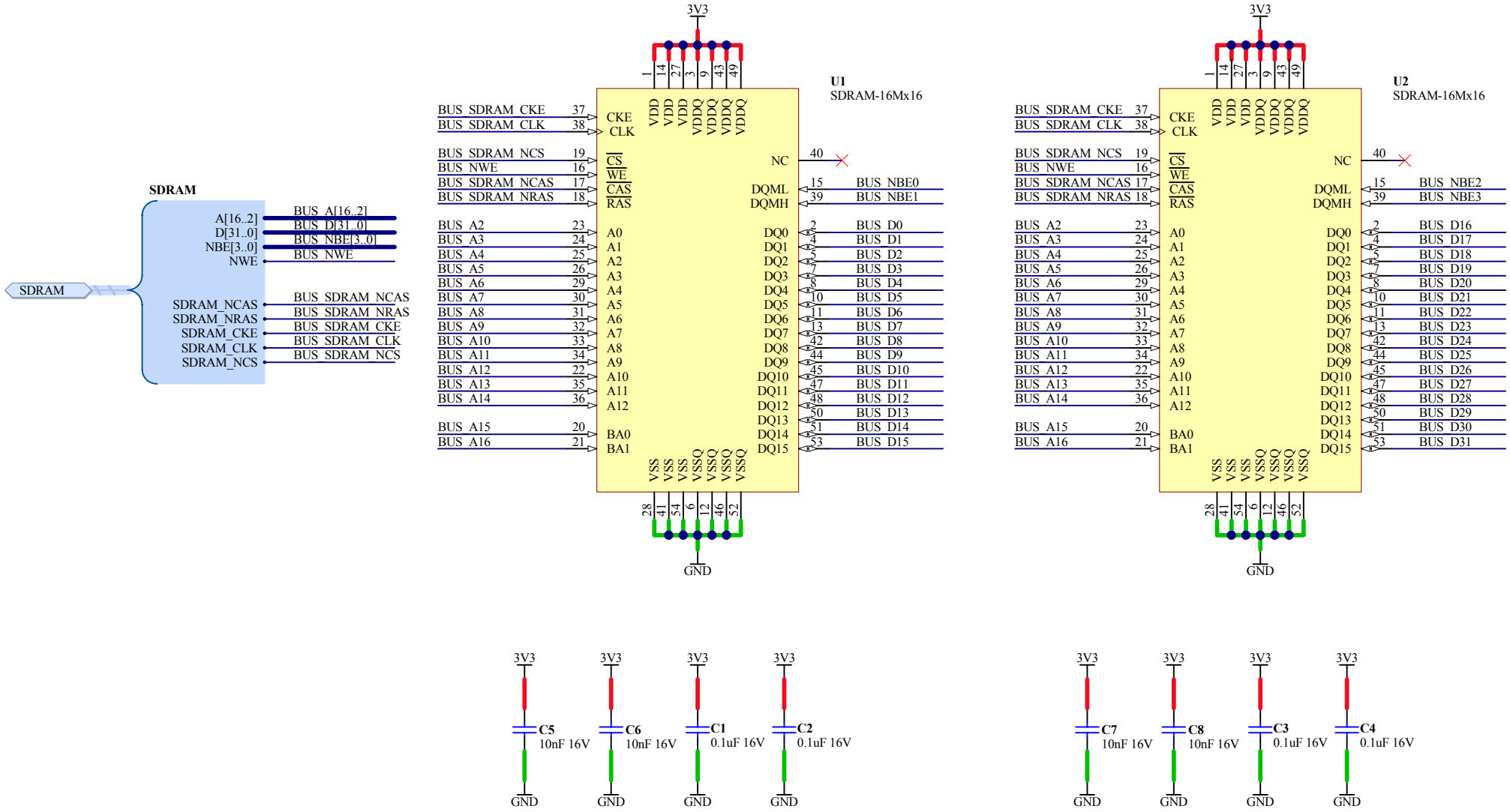

Sheet Title	***16M x 32 SDRAM TSOP54 x 2***	
Project Title	***DB46 - Virtex4 SX35***	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 17 of 23
File: SDRAM_MT48LC16M16A2TG_16Mx32.SchDoc		

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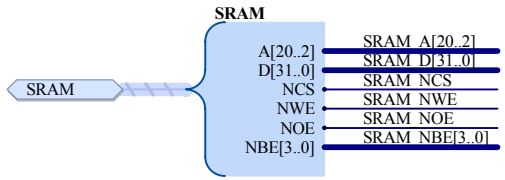
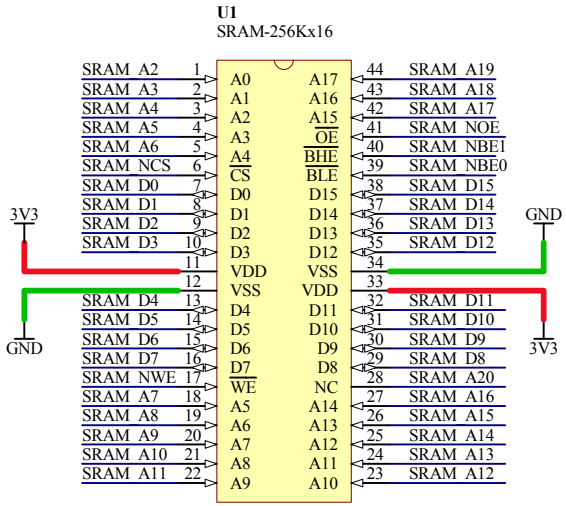
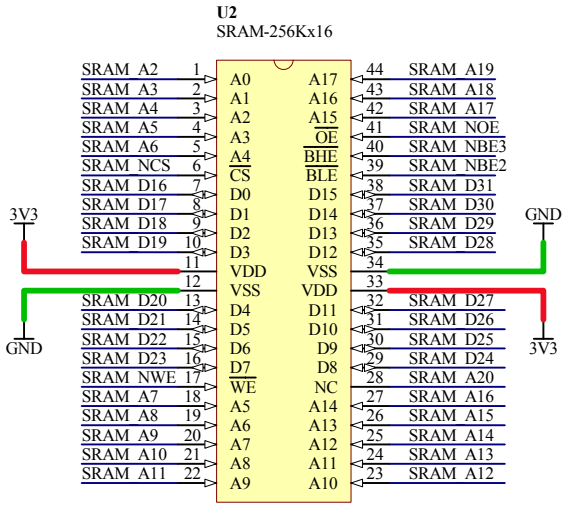
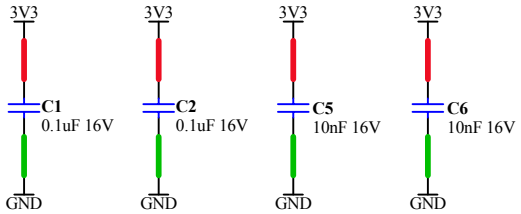
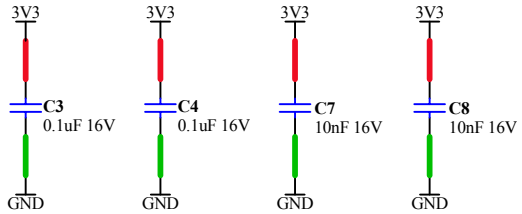
A18 is connected so that 512KBx16 device can be fitted











Sheet Title	*256K x 32 SRAM - TSOP44 x 2*		
Project Title	*DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 18 of 23	
File: SRAM_256Kx32_TSOP44_1.SchDoc			

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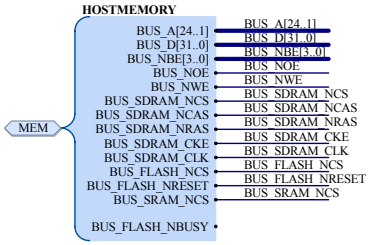
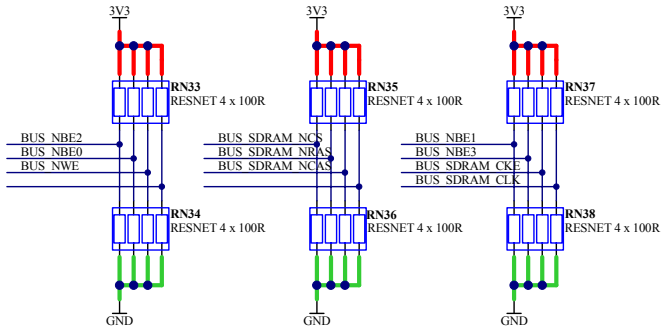


THESE SIGNALS TERMINATE AT THE SDRAM DEVICE



All devices using controlled impedance outputs from the source (ie. FPGA) should use 50 ohm (2 parallel 100 ohm resistors) termination.

The Flash should be located closest to the source (FPGA).
The SRAM should be located next furthest from the source (FPGA).
The SDRAM should be located next furthest from the source (FPGA).
Terminations are to be located at the furthest distance from the source (FPGA).

Note that pins 5,6,7 and 8 of the following resnet "groups" are pin-swappable within that "group":
- all "power" resnets that terminate the FLASH-only signals (ie. RN1 and RN3).
- all "ground" resnets that terminate the FLASH-only signals (ie. RN2 and RN4).
- all "power" resnets that terminate the FLASH-SRAM-only signals (ie. RN5 and RN7).
- all "ground" resnets that terminate the FLASH-SRAM-only signals (ie. RN6 and RN8).
- all "power" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN9, RN11, RN13, RN15, RN17, RN19, RN21, RN23, RN25, RN27, RN29, RN31, RN33, RN35).
- all "ground" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN10, RN12, RN14, RN16, RN18, RN20, RN22, RN24, RN26, RN28, RN30, RN32, RN34, RN36).

To remove any confusion by the PCB assembler, the following devices have been deleted entirely from the design: RN1 to RN16, and RN17 to RN32.

Note that high current (up to 1.25 Amps) is drawn from the 3V3 rail when all 19 pairs of resnets are loaded. The addition of up to 4.1 watts of heat was significantly warming the PCB.

Testing has confirmed that the loading of only 3 pairs of resnets (RN33/34, RN35/36 and RN37/38) provides good operation at speeds up to 96MHz. This consumes up to 0.20 amps, ie. up to 0.65 watts of heat.

The loading of the 3 pairs of resnets terminates only the output control signals from the FPGA to the SDRAM. The bidirectional data bus and address bus is not terminated. Signals that do not connect to the SDRAM (ie. signals to the slower flash and SRAM devices only) are also not terminated.

Sheet Title	*Memory CommonBus Terminations*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A3	Assy: D-820-0031	Revision: 02
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 19 of 23
File: NB2_CommonMemory_Termination.SchDoc		

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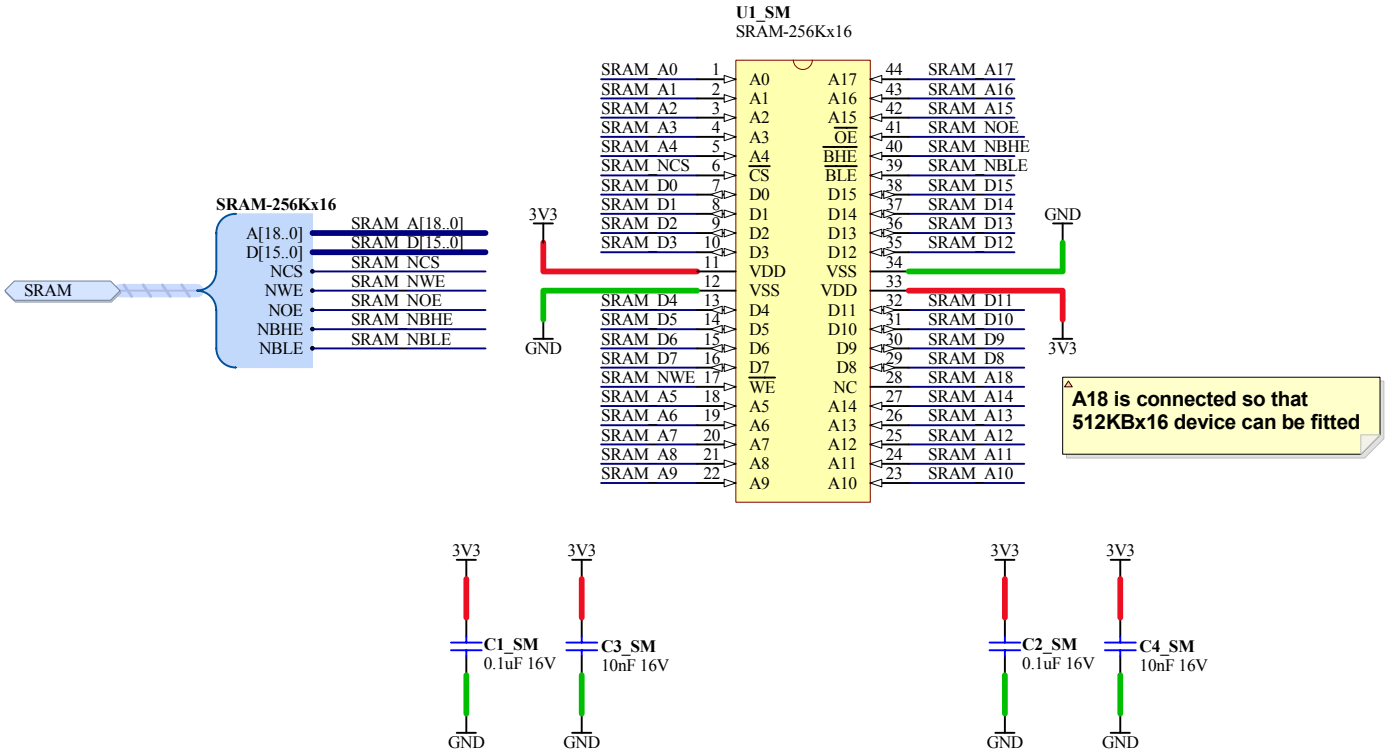

Sheet Title	*256K x 16-Bit SRAM*	
Project Title	*DB46 - Virtex4 SX35*	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:04 PM	Sheet 20 of 23	
File: SRAM_256Kx16_TSOP44.SchDoc		

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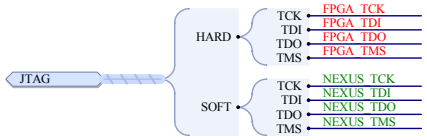
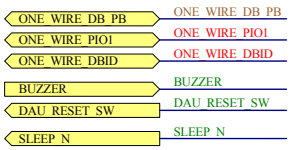
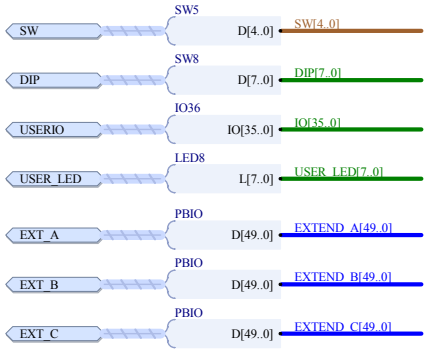
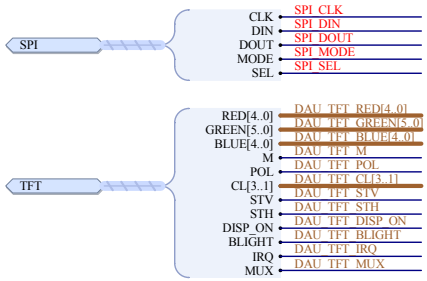
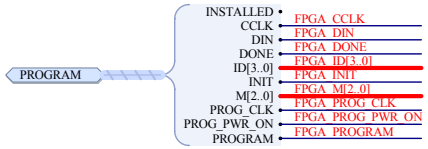
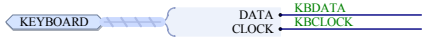


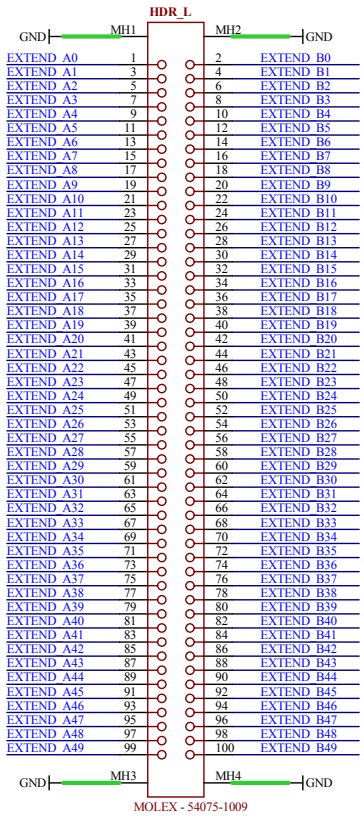


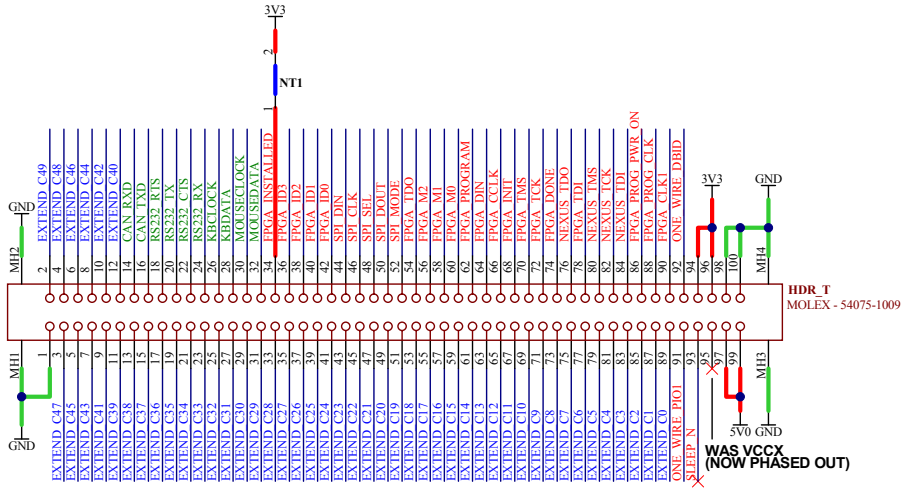






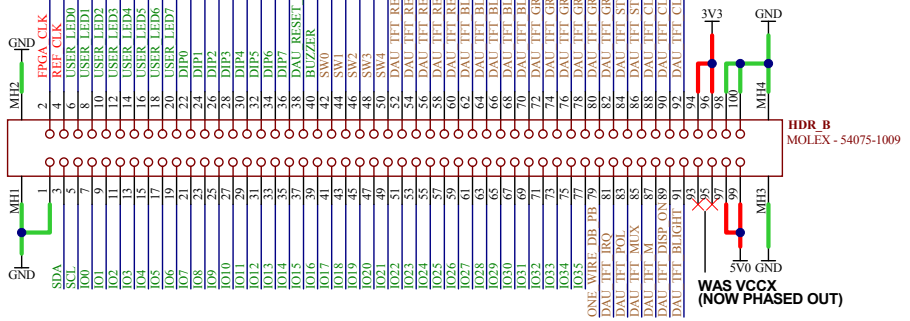






Note that the signal ONE_WIRE_DBID was previously called FPGA_CLK2.

This signal was included in NB1 design, but never used. Hence it has now been reallocated.



Red Connections are locked for NB1 compatibility. They are hardwired on the NB1 and therefore can NOT be changed.

Green connections are I/O pins connected to NB1 compatible PCB resources on the mother board. These can be changed.

Blue connections are connected to the New NB2 compatible resources on the motherboard. These can be changed.

Sheet Title	NB2 to Daughter Board Connectors		
Project Title	DB46 - Virtex4 SX35		
Size: A3	Assy: D-820-0031	Revision: 02	
Date: 27/1/2008	Time: 4:51:05 PM	Sheet 21 of 23	
File: DB_MotherBoardConnectors.SchDoc			

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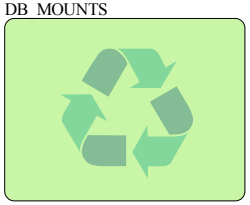
PCB1
DB46 Blank PCB
Printed Circuit Board (Bare)

U_MOUNTS
DB_MOUNTS



Fiducial Alignment Components

FD1
Fiducial - Round

FD2
Fiducial - Round

Sheet Title	***DB46 Hardware Kit***	
Project Title	***DB46 - Virtex4 SX35***	
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:05 PM	Sheet 22 of 23	
File: DB46_Hardware_Kit.SchDoc		

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MH1
MOUNTING HOLE 3MM

MH2
MOUNTING HOLE 3MM

MH3
MOUNTING HOLE 3MM

Altium Logo Top1

Altium Logo Bot1

Sheet Title *Mounts, Logo & Label*		
Project Title *DB46 - Virtex4 SX35*		
Size: A4	Assy: D-820-0031	Revision: 02
Date: 27/11/2008 Time: 4:51:05 PM		Sheet 23 of 23
File: DB_MOUNTS.SchDoc		

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