

Cross point mixer for telephones

BU8241F / BU8241FS / BU8242F / BU8244F

The BU8241F, BU8241FS, BU8242F, and BU8244F are ICs developed for use with cordless telephones, and are equipped with switching and mixing functions. In addition, these ICs are provided with an internal power save function which enables the circuit to be run on line current if the power supply fails, by connecting a switch between the circuit and a new handset, reducing line current consumption. A series of these ICs is also under development, based on the number of circuits.

| Product | No. of circuits |
|--------------------|-----------------|
| BU8241F / BU8241FS | 8×8 matrix |
| BU8242F | 6×6 matrix |
| BU8244F | 4×4 matrix |

●Applications

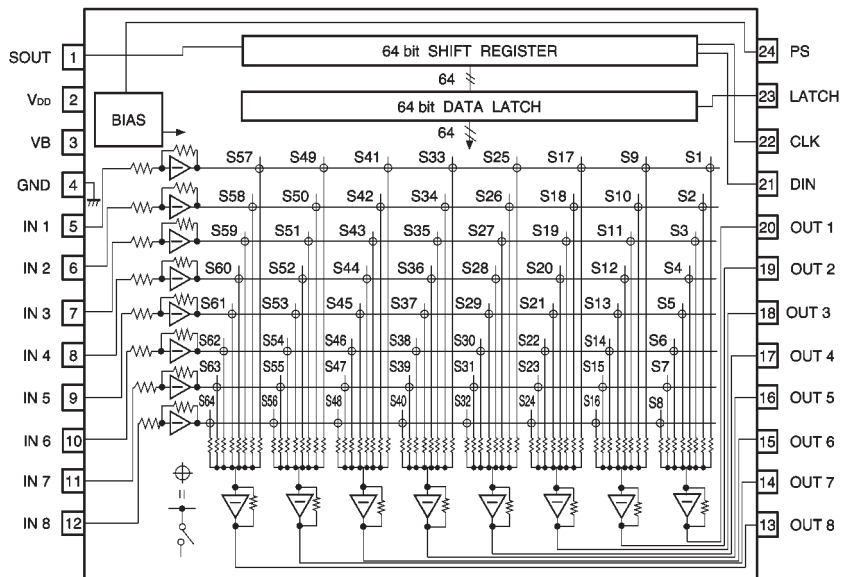
Telephones, telephone answering machines, cordless telephones

●Features

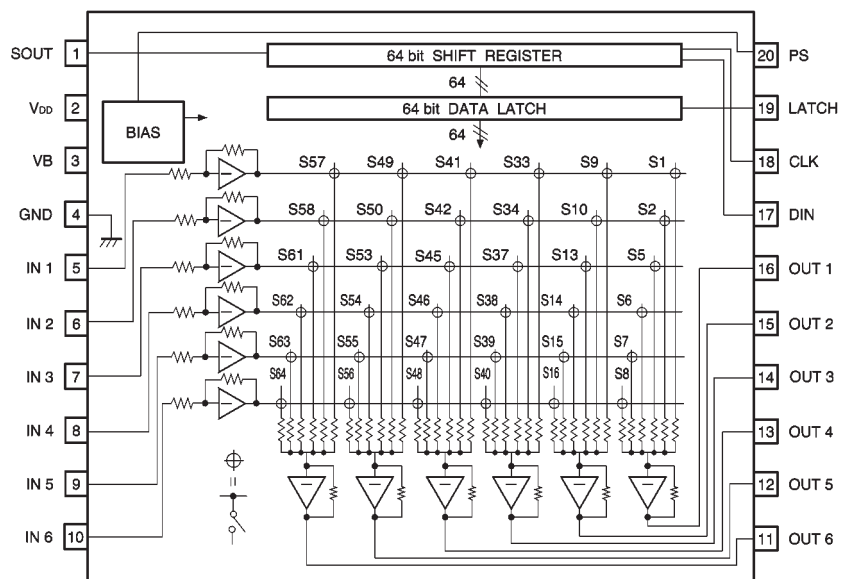
- 1) Eight input signals are selected and mixed by a cross-point, and output to eight pins (BU8241F/BU8241FS).
- 2) A power save mode enables the circuit to run on line current if the power supply fails.
 1. Line current consumption reduced
($I_{DD2} = 580\mu\text{A}$)
 2. $\text{IN1} \rightarrow \text{OUT1}$ and $\text{IN2} \rightarrow \text{OUT2}$ only are on
 - 3) Serial binary data input.
 - 4) Low voltage and current consumption.

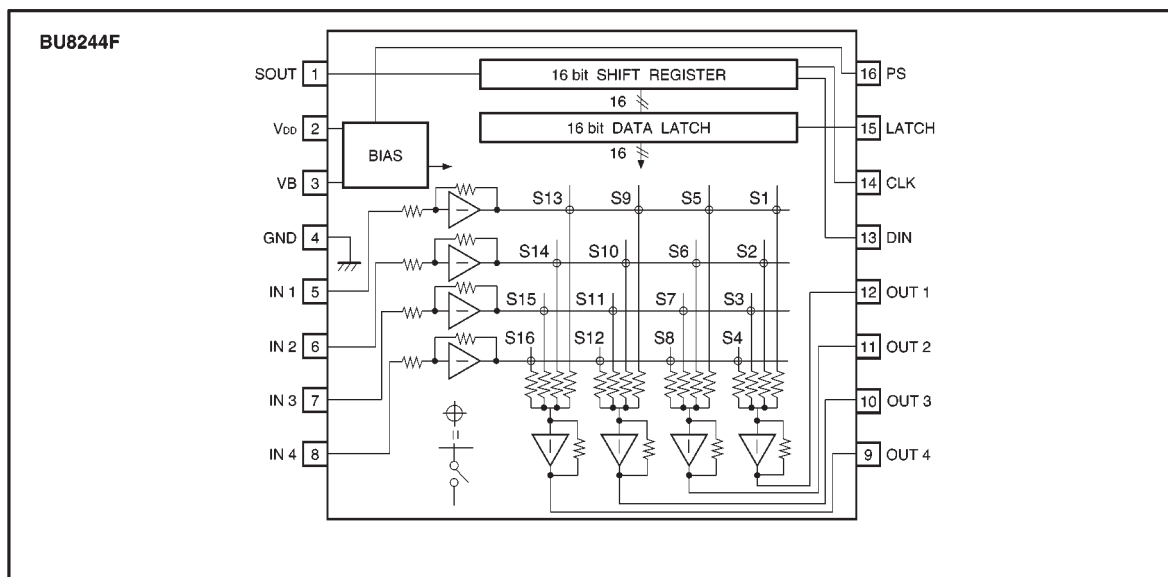
● Block diagram

BU8241F/BU8241FS



BU8242F





● Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

| Parameter | Symbol | Limits | Unit |
|-----------------------|-----------|----------------------------------|------------------|
| Power supply voltage | V_{DD} | 7 | V |
| Input voltage | V_{IN} | $\text{GND}-0.3 \sim V_{DD}+0.3$ | V |
| Output voltage | V_{OUT} | $\text{GND}-0.3 \sim V_{DD}+0.3$ | V |
| Power dissipation | P_d | 550 (BU8241F / BU8242F) *1 | mW |
| | | 800 (BU8241FS) *2 | |
| | | 500 (BU8244F) *3 | |
| Operating temperature | T_{opr} | $-25 \sim +75$ | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | $-55 \sim +125$ | $^\circ\text{C}$ |

*1 Reduced by 5.5mW for each increase in T_a of 1°C over 25°C .

*2 Reduced by 8mW for each increase in T_a of 1°C over 25°C .

*3 Reduced by 5mW for each increase in T_a of 1°C over 25°C .

● Recommended operating range ($T_a = 25^\circ\text{C}$)

| Parameter | Symbol | Range | Unit | Conditions |
|------------------------|-----------|-----------|------------|--|
| Power supply voltage | V_{DD} | 2.7~5.5 | V | |
| Input voltage | v_{in} | ≤ 0 | dBV | |
| Clock frequency | f_{CLK} | ≤ 1 | MHz | Duty 50% |
| Output load resistance | R_L | $10 \leq$ | k Ω | Complete analog signal output terminal |

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|--------------------------------------|------------------|--------------------|------|--------------------|------|---|
| Supply current 1 | I _{DD1} | 3.2 | 4.8 | 8.0 | mA | Normal operation, with output pins open *1 |
| | | 1.5 | 2.5 | 4.0 | mA | Normal operation, with output pins open *2 |
| Supply current 2 | I _{DD2} | 400 | 580 | 760 | μA | In power save mode, with output pins open, at V _{DD} = 3 V |
| Input high level voltage | V _{IH} | 0.8V _{DD} | — | V _{DD} | V | DIN, CLK, LATCH, and PS pins |
| Input low level voltage | V _{IL} | GND | — | 0.2V _{DD} | V | DIN, CLK, LATCH, and PS pins |
| Input high level current | I _{IH} | — | — | 2 | μA | DIN, CLK, LATCH, and PS pins |
| Input low level current | I _{IL} | — | — | 2 | μA | DIN, CLK, LATCH, and PS pins |
| Output saturation high level voltage | V _{OH} | 0.9V _{DD} | — | — | V | I _{OH} = -100 μA, SOUT pin |
| Output saturation low level voltage | V _{OL} | — | — | 0.1V _{DD} | V | I _{OL} = 100 μA, SOUT pin |
| VB pin voltage | V _{VB} | 2.13 | 2.50 | 2.88 | V | No load |
| Input impedance | Z _{IN} | 48 | 80 | 112 | kΩ | f _{in} = 1kHz, v _{in} = 0dBV, all analog input pins |

〈Cross-point unit〉

| | | | | | | |
|--|-------------------|----|-----|-----|-----|--|
| Gain | GT | -1 | 0 | 1 | dB | f _{in} = 1kHz, v _{in} = 0dBV |
| Distortion | DT | — | 0.1 | 0.5 | % | f _{in} = 1kHz, v _{in} = -10dBV |
| Maximum output level | v _{OM} | 0 | 3 | — | dBV | f _{in} = 1kHz, THD = 5% |
| Noise level 1 | NT1 | — | -80 | -70 | dBV | BPF = 400 to 30 kHz, 4-channel mixing |
| Noise level 2 | NT2 | — | -90 | — | dBV | BPF = 400 to 30 kHz, any one channel |
| Muting ratio | v _{MR} | — | -90 | -80 | dB | f _{in} = 1kHz, v _{in} = 0dBV, BPF = 1kHz*3 |
| Crosstalk | v _{CT} | — | -80 | -70 | dB | f _{in} = 1kHz, v _{in} = 0dBV, BPF = 1kHz*4 |
| Minimum operating power supply voltage | V _{Min.} | — | — | 2.4 | V | Operation is guaranteed at these values, but the characteristics noted on this table are not guaranteed. |

〈Shift register and data latch unit〉

| | | | | | | |
|------------------|-----------------|-----|---|---|------|-----------|
| Data setup time | t _{SU} | 100 | — | — | nsec | DIN→CLK |
| Data hold time | t _H | 100 | — | — | nsec | CLK→DIN |
| Clock latch time | t _{CL} | 100 | — | — | nsec | CLK→LATCH |

*1 Applicable to the BU8241F, BU8241FS and BU8242F.

*2 Applicable to the BU8244F.

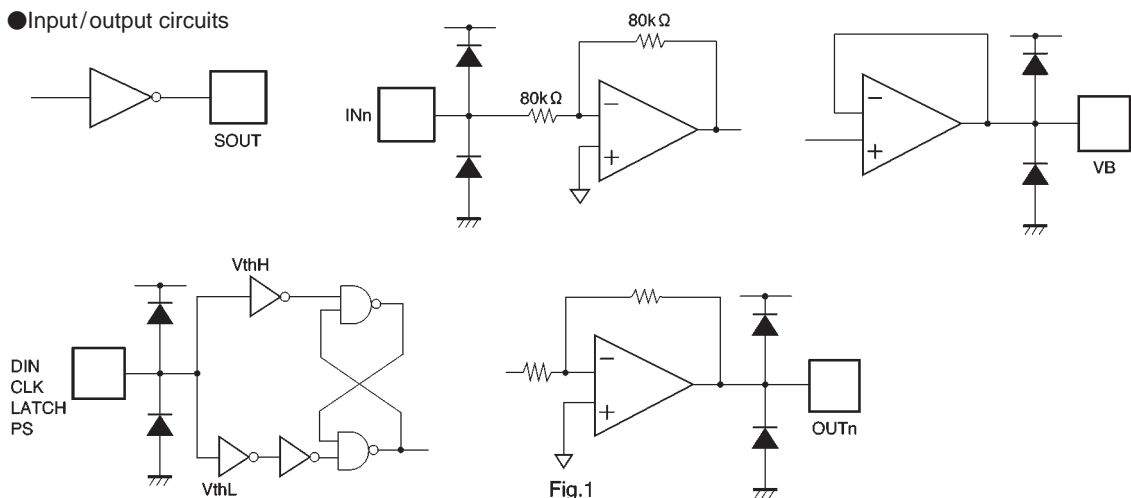
*3 On/Off ratio for the same channel.

*4 Signal leakage between different channels.

● Pin descriptions

| BU8241F / BU8241FS Pin No. | BU8242F Pin No. | BU8244F Pin No. | Pin name | Function |
|-------------------------------|--------------------|--------------------|-----------------|---|
| 1 | 1 | 1 | SOUT | Serial output data pin for cascade connection |
| 2 | 2 | 2 | V _{DD} | Power supply pin |
| 3 | 3 | 3 | VB | Bias decoupling pin |
| 4 | 4 | 4 | GND | Ground pin |
| 5 | 5 | 5 | IN1 | Signal input pin |
| 6 | 6 | 6 | IN2 | Signal input pin |
| 7 | 7 | 7 | IN3 | Signal input pin |
| 8 | 8 | 8 | IN4 | Signal input pin |
| 9 | 9 | — | IN5 | Signal input pin |
| 10 | 10 | — | IN6 | Signal input pin |
| 11 | — | — | IN7 | Signal input pin |
| 12 | — | — | IN8 | Signal input pin |
| 13 | — | — | OUT8 | Signal output pin |
| 14 | — | — | OUT7 | Signal output pin |
| 15 | 11 | — | OUT6 | Signal output pin |
| 16 | 12 | — | OUT5 | Signal output pin |
| 17 | 13 | 9 | OUT4 | Signal output pin |
| 18 | 14 | 10 | OUT3 | Signal output pin |
| 19 | 15 | 11 | OUT2 | Signal output pin |
| 20 | 16 | 12 | OUT1 | Signal output pin |
| 21 | 17 | 13 | DIN | Serial input data pin |
| 22 | 18 | 14 | CLK | Shift clock input pin for shift register |
| 23 | 19 | 15 | LATCH | Latch input pin for data latch |
| 24 | 20 | 16 | PS | Power save setting input pin |

● Input/output circuits



●Circuit operation

Sections (1) to (3) below describe operation using the BU8241F and BU8241FS as examples.

(1) Analog signals pass through an input amplifier and are supplied to eight switches.

The analog input signals are turned on and off by the switches and can thus be directed to any desired output amplifier. Using mixing resistors connected to the outputs of the switches, and feedback resistors, each output amplifier can output a signal that is a mix of up to eight input signals.

(2) The switch states are set using a 64-bit shift register and data latch.

The shift register reads the data at the rising edge of the shift clock, and stores it until the next data is read at the rising edge of the next shift clock.

After the 64 data bits have been read, supply of the rising edge of the clock is stopped, the LATCH pin is set to HIGH, and the switches are set. (See Figure 2 for the timing waveform.)

To change a switch setting, new setting data and shift clocks must be supplied for 64 bits of data, and the LATCH pin set to HIGH. If the LATCH pin is set to HIGH before 64 shift clocks have been supplied, or after more than 64 have been supplied, the switches cannot be set properly. (See Table 1 for the logic of switch settings.)

Table.1 Switch Sn stage (Note 6)

| Data Dn (Note 6) | Switch Sn state (Note 6) |
|------------------|--------------------------|
| H | ON |
| L | OFF |

(Note 11) Equivalent to $n = 1 \sim 64$

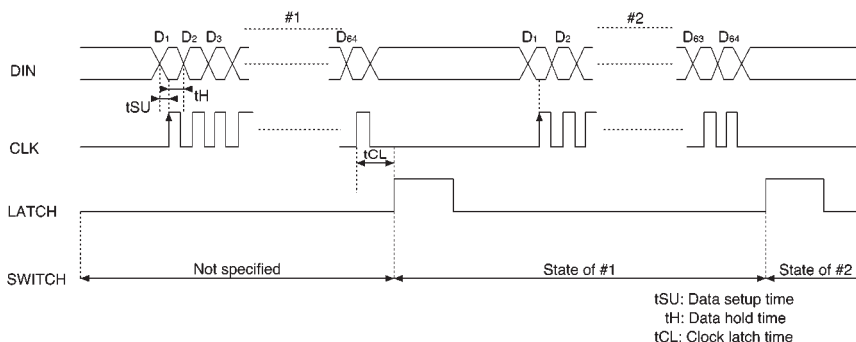


Fig. 2 Timing waveform

(3) The power save mode is set as long as the PS pin is kept HIGH. (See Table 2 for the power save setting logic.) In the power save mode, the following are fixed : IN1 → OUT1 (S1 = ON) and IN2 → OUT2 (S10 = ON). (The other 62 switches are off.) In addition, the line current is reduced. When the PS pin goes from HIGH to LOW, the IC state switches from the power save mode back to normal operation. At that point, the state of the switch remains in the power save mode (only S1 and S10 are on). (See Figure 3 for the timing waveform in the power save mode.)

(4) With the BU8242F, of the 64 data bits, the following should be input at LOW level : D₃, D₄, D₁₁, D₁₂, D₁₇ to D₃₂, D₃₅, D₃₆, D₄₃, D₄₄, D₅₁, D₅₂, D₅₉, and D₆₀.

(5) With the BU8244F, DIN is 16 bits.

The ON path in the power save mode is the same for the BU8241F and BU8241FS, but the pertinent switches are S1 and S6.

Table.2 Power save setting theory

| PS pin | State |
|--------|-----------------------|
| L | Normal operating mode |
| H | Power save mode |

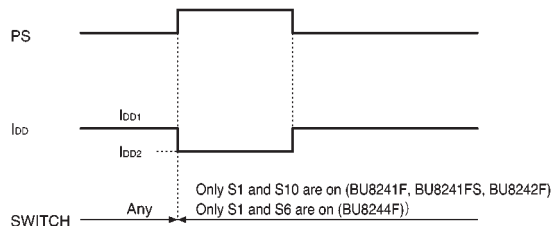


Fig. 3 Power save mode timing waveform

●Application example

The BU8241F and BU8241FS are shown in this example.

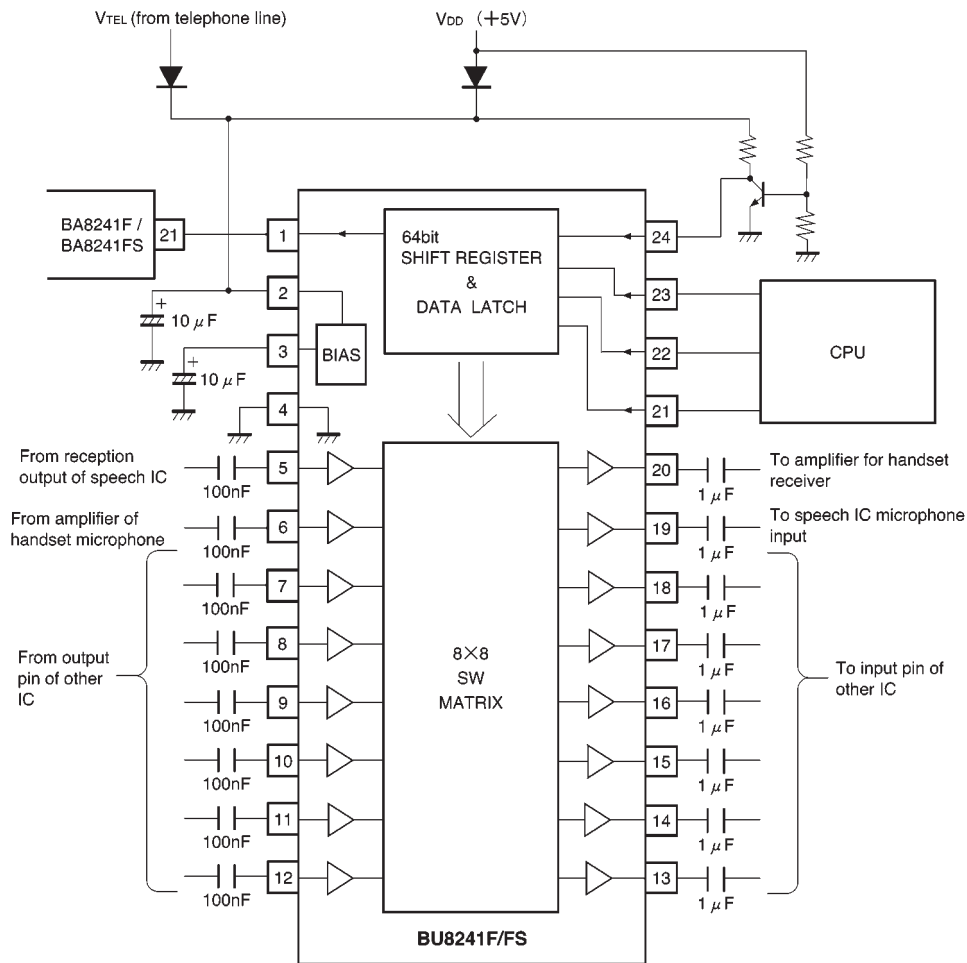


Fig.4

● Selecting attached components

1) Components related to power supply and bias

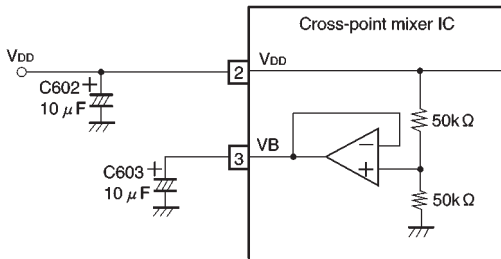


Fig. 5 Power supply and bias circuit

C602: V_{DD} bias capacitor; normally $10\mu\text{F}$

C603: VB decoupling capacitor; normally $10\mu\text{F}$

2) Components related to input pins

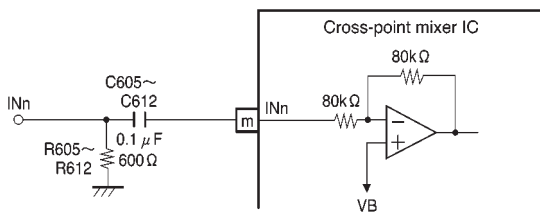


Fig. 6 Input circuit

C605 to C612: DC cutoff capacitor. A value should be selected which does not attenuate voice signals in the high band (300 Hz ~).

R605 to R612: Resistor which sets the input level. This should normally be left open.

The constants shown in Figure 8 are set to match the oscillator output impedance.

3) Components related to output pins

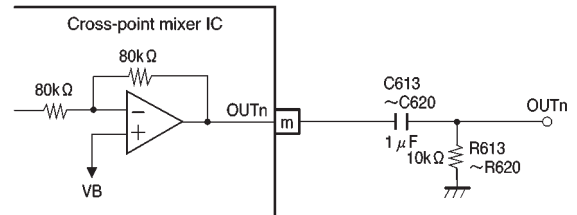


Fig. 7 Output circuit

C613 to C620: DC cutoff capacitor. A value should be selected which does not attenuate voice signals in the high band (300 Hz ~).

R613 to R620: Output load resistors. This should normally be left open.

If using R615 to R620, select values that result in a total input impedance of $10\text{k}\Omega$ or greater on the output side. If the total impedance is less than $10\text{k}\Omega$, the load on the output amplifier of the cross-point mixer will be excessive, and signals may be lost.

● Operation notes

(1) Turning on the power supply

When the power supply is turned on, the shift register is in an indeterminate state. After turning on the power supply, switch settings should be entered by supplying shift clock pulses to shift 64 bits of data into the shift register, and then setting the LATCH pin to HIGH. (For the BU8244, send 16 clock pulses.)

(2) Setting serial data

If the number of bits shifted or clock pulses applied is less than or more than the number stated above, the switches will not be set properly. Never apply shift clock pulses when the LATCH pin is HIGH. Doing so will change the data latch contents.

(3) Drive impedance

The input impedance Z_{in} is $80 \pm 32 \text{ k}\Omega$.

To suppress input gain and loss, we recommend using the drive impedance shown in the table below.

If the level is to be attenuated at the input pin, make sure the level is not affected by the internal resistance of the IC, as shown in Figure 10. This can cause gain and/or loss.

| Gain/loss | Drive impedance |
|-------------|-------------------|
| 1 dB max. | 4 k Ω max. |
| 0.5 dB max. | 2 k Ω max. |

(4) Gain and noise when mixing signals

Increasing the number of signals mixed in a single output (increasing the number of switches connected to the same output amplifier that are on) causes a slight drop in gain. With the BU8241 and BU8241FS/BU8242F, increasing the number of signals mixed in a single output (increasing the number of switches connected to the same output amplifier that are on) causes a slight increase in the noise level in terms of logic. If noise is a problem, we recommend limiting the number of signals mixed in a single output.

(5) Output load capacitance

The capacitance connected to GND in relation to an output pin (the output load capacitance) should be kept to 50pF or lower. (BU8241F/BU8241FS/ BU8242F)

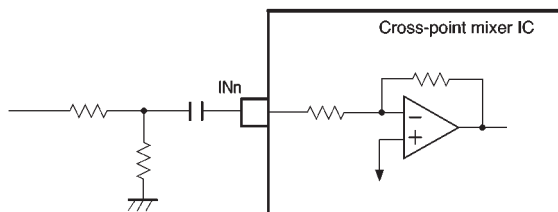


Fig. 8 Attenuation circuit with input

● Electrical characteristic curves

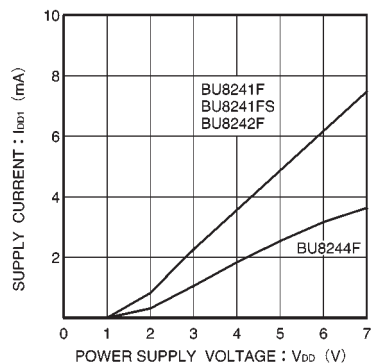


Fig. 9 Supply current vs. power supply voltage

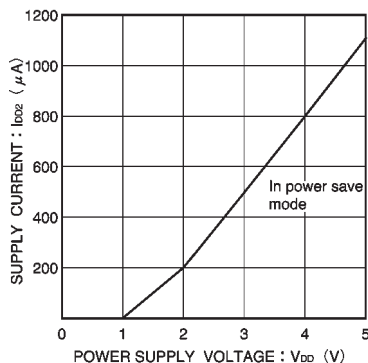


Fig. 10 Supply current vs. power supply voltage (power save mode)

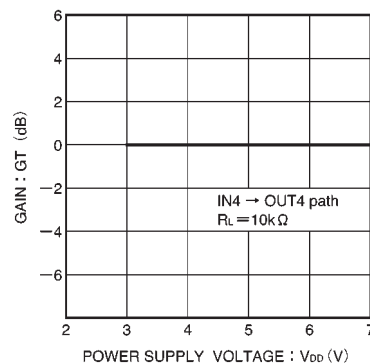


Fig. 11 Gain vs. power supply voltage

●Electrical characteristic curves

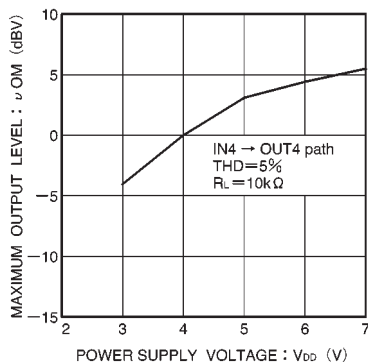


Fig. 12 Maximum output level vs. power supply voltage

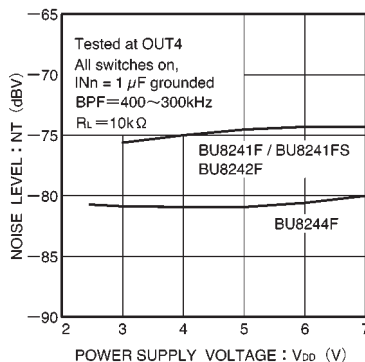


Fig. 13 Noise level vs. power supply voltage

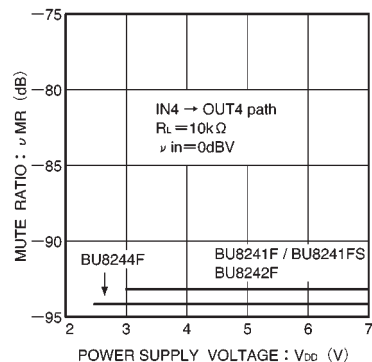


Fig. 14 Mute ratio vs. power supply voltage

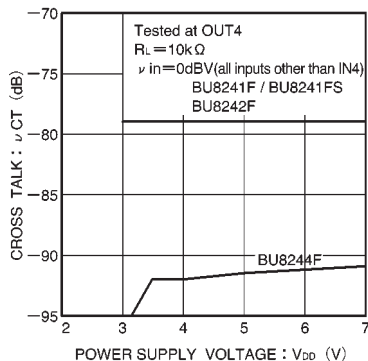


Fig. 15 Crosstalk vs. power supply voltage

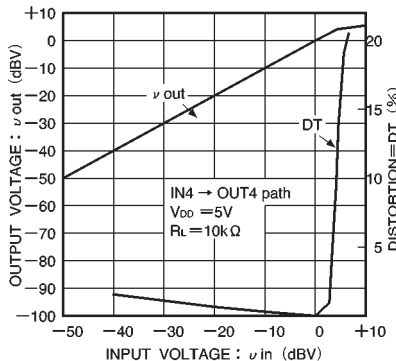


Fig. 16 Input/output characteristic

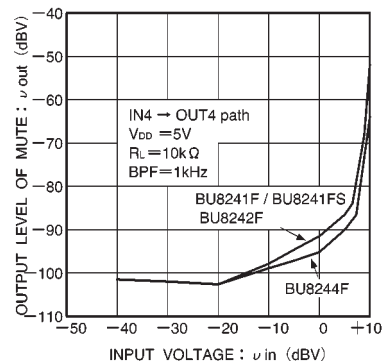


Fig. 17 Output level when muted vs. input voltage

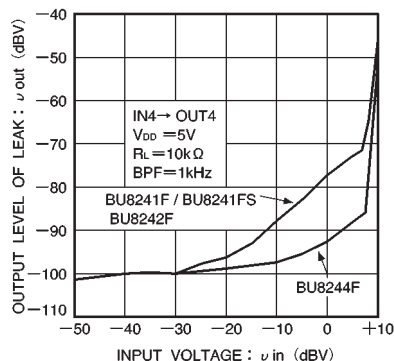
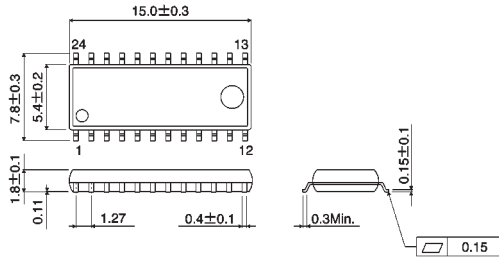


Fig. 18 Output leakage level vs. input voltage

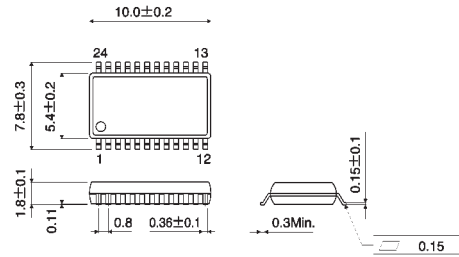
● External dimensions (Units: mm)

BU8241F



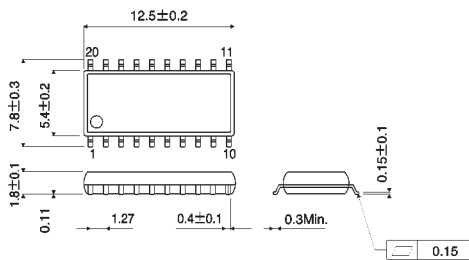
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BU8241FS



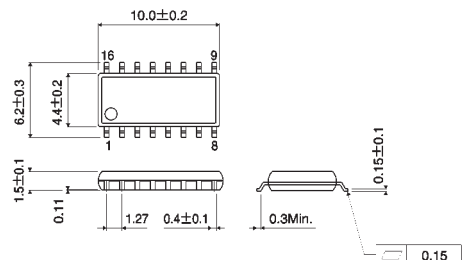
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BU8242F



SOP20

BU8244F



SOP16

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