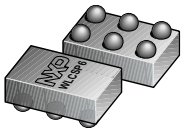


BGS8M2UK

SiGe:C low-noise amplifier MMIC with bypass switch for LTE

Rev. 1 — 17 November 2016 Product data sheet

1. General description

The BGS8M2UK is a Low-Noise Amplifier (LNA) with bypass switch for LTE receiver applications, available in a Wafer-Level Chip-Scale Package (WLCSP). This product is only to be used in an overmolded module.

The BGS8M2UK delivers system-optimized gain for both primary and diversity applications where sensitivity improvement is required. The high linearity of this low noise device ensures the required receive sensitivity independent of cellular transmit power level in Frequency Division Duplex (FDD) systems. When receive signal strength is sufficient, the BGS8M2UK can be switched off to operate in bypass mode at a 1 μA current. And to lower power consumption. The BGS8M2UK requires only one external matching inductor.

The BGS8M2UK is optimized for 1805 MHz to 2200 MHz.

2. Features and benefits

- Operating frequency from 1805 MHz to 2200 MHz
- Noise figure = 0.75 dB
- Gain 15.4 dB
- High input 1 dB compression point of −3.5 dBm
- Bypass switch insertion loss of −1.9 dB
- High in band $IP3_i$ of 2.5 dBm
- Supply voltage 1.5 V to 3.1 V
- Integrated supply decoupling capacitor
- Optimized performance at a supply current of 5.8 mA
- Bypass mode current consumption < 1 μA
- Integrated temperature stabilized bias for easy design
- Requires only one input matching inductor
- Input and output AC coupled
- ESD protection on all pins (HBM > 2 kV)
- Integrated matching for the output
- Available in a WLCSP 0.69 mm × 0.44 mm × 0.2 mm: SOT1445-1
- 180 GHz transit frequency - SiGe:C technology
- Moisture sensitivity level 1

3. Applications

- LNA for LTE reception in smart phones
- Feature phones
- Tablet PCs
- RF front-end modules

4. Quick reference data

Table 1. Quick reference data

f = 1960 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)} \geq 0.8$ V; T_{amb} = 25 °C; input matched to 50 Ω using a 3.9 nH inductor in series; see Figure 4. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
I_{CC}	supply current	in gain mode	-	5.8	-	mA
		in bypass mode; 0.1 V ≤ $V_{I(CTRL)}$ ≤ 0.3 V	-	8	15	µA
G_p	power gain	in gain mode [1]	-	15.4	-	dB
		in bypass mode [1]	-	–1.9	-	dB
NF	noise figure	[1][2]	-	0.75	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	[1]	-	–3.5	-	dBm
$IP3_i$	input third-order intercept point	[1]	-	2.5	-	dBm

[1] E-UTRA operating band 2 (1930 MHz to 1990 MHz).

[2] PCB losses are subtracted.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BGS8M2UK	WLCSP6	wafer level chip-scale package; 6 bumps; 0.69 × 0.44 × 0.29 mm	SOT1445-1

6. Marking

Table 3. Marking codes

Type number	Marking code
BGS8M2UK	single character, indicating assembly month[1]

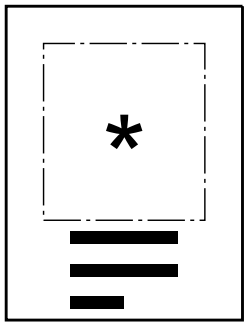
[1] Month codes, see Table 4.

Table 4. Calender marking month code

The character from the table replaces the asterisk (*), see Figure 1.

Year[1]	Month											
	J	F	M	A	M	J	J	A	S	O	N	D
2015	A	B	C	D	E	F	G	H	I	J	K	L
2016	M	N	O	P	Q	R	S	T	U	V	W	X
2017	Y	Z	b	d	f	h	3	4	5	6	7	8

[1] Rotates every 3 years.



Pin A1 location: the marking stripes below character indicate the side where pin A1 is located.

Fig 1. Marking code description

7. Block diagram

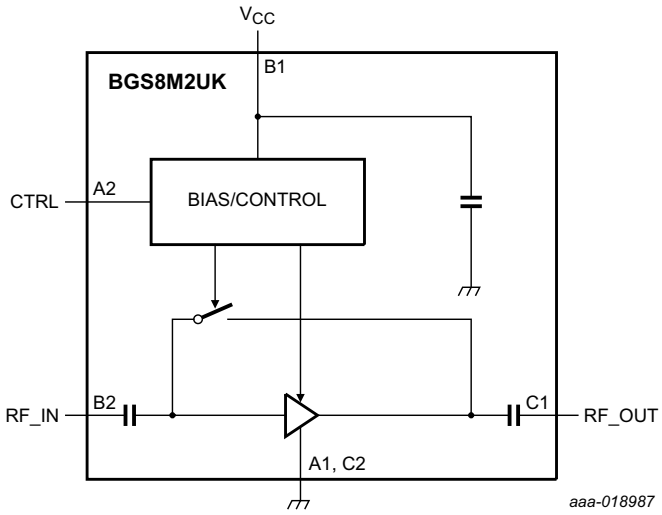
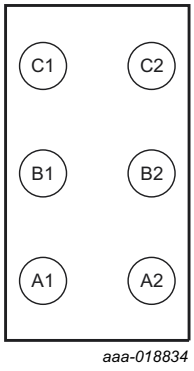


Fig 2. Block diagram

8. Pinning information

8.1 Pinning



Bump side view

Fig 3. Bump mapping

8.2 Pin description

Table 5. Bump description

Symbol	Pad	Description
GND	A1	ground
V_{CC}	B1	supply voltage
RF_OUT	C1	RF output

Table 5. Bump description *…continued*

Symbol	Pad	Description
CTRL	A2	gain control, switch between gain and bypass mode
RF_IN	B2	RF input
GND_RF	C2	ground RF

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Absolute Maximum Ratings are given as Limiting Values of stress conditions during operation, that must not be exceeded under the worst probable conditions.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	RF input AC coupled [1]	−0.5	+5.0	V
$V_{I(CTRL)}$	input voltage on pin CTRL	$V_{I(CTRL)} < V_{CC} + 0.6$ V [1][2]	−0.5	+5.0	V
$V_{I(RF\_IN)}$	input voltage on pin RF_IN	DC; $V_{I(RF\_IN)} < V_{CC} + 0.6$ V [1][2][3]	−0.5	+5.0	V
$V_{I(RF\_OUT)}$	input voltage on pin RF_OUT	DC; $V_{I(RF\_OUT)} < V_{CC} + 0.6$ V [1][2][3]	−0.5	+5.0	V
P_i	input power	[1]	-	10	dBm
P_{tot}	total power dissipation	$T_{sp} \leq 130$ °C	-	55	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001	-	±2	kV
		Charged Device Model (CDM) according to JEDEC standard JESD22-C101C	-	±1	kV

[1] Stressed with pulses of 200 ms in duration.

[2] Warning: Due to internal ESD diode protection, to avoid excess current, the applied DC voltage must not exceed VCC + 0.6 V or 5.0 V.

[3] The RF input and output are AC coupled through internal DC blocking capacitors.

10. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
T_{amb}	ambient temperature		−40	+25	+85	°C
$V_{I(CTRL)}$	input voltage on pin CTRL	bypass mode	-	-	0.25	V
		ON state	0.8	-	-	V

11. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		225	K/W

12. Characteristics

Table 9. Characteristics

1805 MHz ≤ f ≤ 2200 MHz; V_{CC} = 1.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C. Input matched to 50 Ω using a 3.9 nH inductor in series, see Figure 4. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current	$V_{I(CTRL)}$ ≥ 0.8 V	-	5.5	-	mA
G_p	power gain	f = 1843 MHz [1]	-	15.5	-	dB
		f = 1960 MHz [2]	-	15.0	-	dB
		f = 2140 MHz [3]	-	14.0	-	dB
RL_{in}	input return loss	f = 1843 MHz [1]	-	5.5	-	dB
		f = 1960 MHz [2]	-	6.0	-	dB
		f = 2140 MHz [3]	-	7.0	-	dB
RL_{out}	output return loss	f = 1843 MHz [1]	-	12	-	dB
		f = 1960 MHz [2]	-	12	-	dB
		f = 2140 MHz [3]	-	10	-	dB
ISL	isolation	f = 1843 MHz [1]	-	24	-	dB
		f = 1960 MHz [2]	-	24	-	dB
		f = 2140 MHz [3]	-	23	-	dB
NF	noise figure	f = 1843 MHz [1][4]	-	0.7	-	dB
		f = 1960 MHz [2][4]	-	0.75	-	dB
		f = 2140 MHz [3][4]	-	0.85	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 1843 MHz [1]	-	−8.5	-	dBm
		f = 1960 MHz [2]	-	−8	-	dBm
		f = 2140 MHz [3]	-	−6.5	-	dBm
$IP3_i$	input third-order intercept point	f = 1843 MHz [1]	-	0.5	-	dBm
		f = 1960 MHz [2]	-	1.5	-	dBm
		f = 2140 MHz [3]	-	2.5	-	dBm
K	Rollett stability factor		1	-	-	-
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON to 90 % of the gain	-	-	4	µs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF to 10 % of the gain	-	-	1	µs
Bypass mode						
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.3 V	-	-	1	µA
G_p	power gain	f = 1843 MHz [1]	-	−1.9	-	dB
		f = 1960 MHz [2]	-	−2.0	-	dB
		f = 2140 MHz [3]	-	−2.2	-	dB
RL_{in}	input return loss	f = 1843 MHz [1]	-	13	-	dB
		f = 1960 MHz [2]	-	12	-	dB
		f = 2140 MHz [3]	-	11	-	dB
RL_{out}	output return loss	f = 1843 MHz [1]	-	12	-	dB
		f = 1960 MHz [2]	-	11.5	-	dB
		f = 2140 MHz [3]	-	11	-	dB

[1] E-UTRA operating band 3 (1805 MHz to 1880 MHz).

[2] E-UTRA operating band 2 (1930 MHz to 1990 MHz).

[3] E-UTRA operating band 1 (2110 MHz to 2170 MHz).

[4] PCB losses are subtracted.

Table 10. Characteristics

1805 MHz ≤ f ≤ 2200 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C. Input matched to 50 Ω using a 3.9 nH inductor in series, see Figure 4; Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current	$V_{I(CTRL)}$ ≥ 0.8 V	-	5.8	-	mA
G_p	power gain	f = 1843 MHz [1]	-	15.8	-	dB
		f = 1960 MHz [2]	-	15.4	-	dB
		f = 2140 MHz [3]	-	14.6	-	dB
RL_{in}	input return loss	f = 1843 MHz [1]	-	5.5	-	dB
		f = 1960 MHz [2]	-	6.5	-	dB
		f = 2140 MHz [3]	-	7.5	-	dB
RL_{out}	output return loss	f = 1843 MHz [1]	-	12	-	dB
		f = 1960 MHz [2]	-	12	-	dB
		f = 2140 MHz [3]	-	10	-	dB
ISL	isolation	f = 1843 MHz [1]	-	24	-	dB
		f = 1960 MHz [2]	-	24	-	dB
		f = 2140 MHz [3]	-	23	-	dB
NF	noise figure	f = 1843 MHz [1][4]	-	0.7	-	dB
		f = 1960 MHz [2][4]	-	0.75	-	dB
		f = 2140 MHz [3][4]	-	0.80	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 1843 MHz [1]	-	−4.5	-	dBm
		f = 1960 MHz [2]	-	−3.5	-	dBm
		f = 2140 MHz [3]	-	−2.5	-	dBm
$IP3_i$	input third-order intercept point	f = 1843 MHz [1]	-	1.5	-	dBm
		f = 1960 MHz [2]	-	2.5	-	dBm
		f = 2140 MHz [3]	-	3.0	-	dBm
K	Rollett stability factor		1	-	-	-
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON to 90 % of the gain	-	-	4	µs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF to 10 % of the gain	-	-	1	µs
Bypass mode						
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.3 V	-	-	1	µA
G_p	power gain	f = 1843 MHz [1]	-	−1.8	-	dB
		f = 1960 MHz [2]	-	−1.9	-	dB
		f = 2140 MHz [3]	-	−2.1	-	dB
RL_{in}	input return loss	f = 1843 MHz [1]	-	13	-	dB
		f = 1960 MHz [2]	-	12	-	dB
		f = 2140 MHz [3]	-	10.5	-	dB

Table 10. Characteristics *...continued*

1805 MHz ≤ f ≤ 2200 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C. Input matched to 50 Ω using a 3.9 nH inductor in series, see Figure 4; Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RL_{out}	output return loss	f = 1843 MHz	[1]	-	12.5	-	dB
		f = 1960 MHz	[2]	-	12	-	dB
		f = 2140 MHz	[3]	-	11	-	dB

[1] E-UTRA operating band 3 (1805 MHz to 1880 MHz).

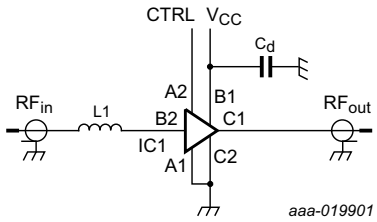
[2] E-UTRA operating band 2 (1930 MHz to 1990 MHz).

[3] E-UTRA operating band 1 (2110 MHz to 2170 MHz).

[4] PCB losses are subtracted.

13. Application information

13.1 LTE LNA



For a list of component, see Table 11.

Fig 4. Schematics LTE LNA evaluation board

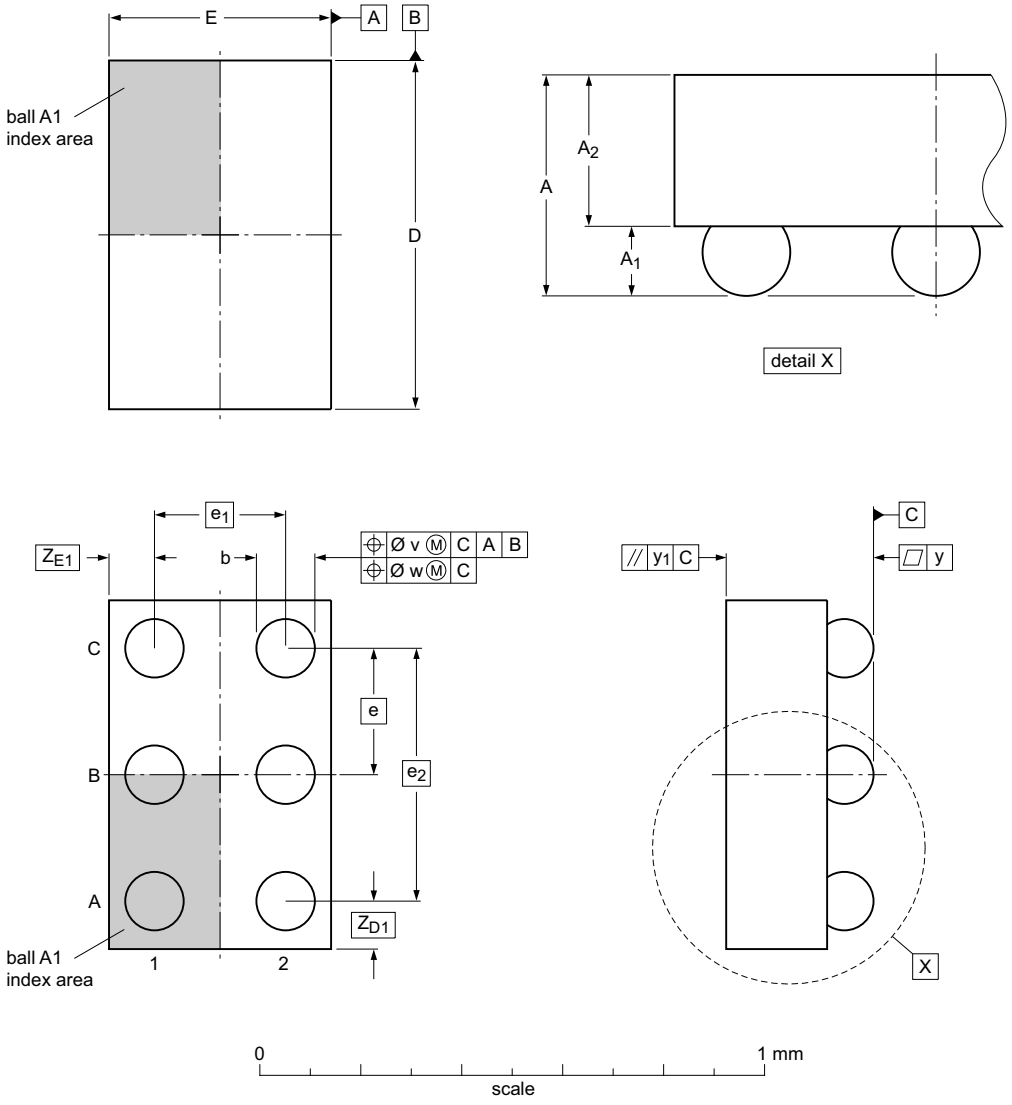
Table 11. List of components

For schematics, see Figure 4

Component	Description	Value	Remarks
C_d	decoupling capacitor	1 µF	Required to suppress power supply noise
IC1	BGS8M2UK	-	NXP Semiconductors N.V.
L1	high-quality matching inductor	3.9 nH	Murata LQW15A

14. Package outline

WLCSP6: wafer level chip-scale package; 6 bumps; 0.69 x 0.44 x 0.29 mm **SOT1445-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1	Z_{D1}	Z_{E1}
	max	0.31	0.105	0.215	0.131	0.705	0.455								0.105	0.10
mm	nom	0.29	0.090	0.200	0.116	0.690	0.440	0.25	0.26	0.50	0.15	0.05	0.015	0.05	0.095	0.09
	min	0.27	0.075	0.185	0.101	0.675	0.425								0.085	0.08

sot1445-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1445-1						~~15-05-11~~ 16-07-11

Fig 5. Package outline SOT1445-1 (WLCSP6)

15. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

16. Mounting

This WLCSP is only to be used in an over-molded module (using MUF)

17. Abbreviations

Table 12. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MUF	Molded Underfill
PCB	Printed-Circuit Board
SiGe:C	Silicon Germanium Carbon

18. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGS8M2UK v.1	20161117	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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21. Contents

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