TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74LCX138F, TC74LCX138FN, TC74LCX138FT

## LOW VOLTAGE 3-TO-8 LINE DECODER WITH 5V TOLERANT INPUTS AND OUTPUTS

(Note) The JEDEC SOP (FN) is not The TC74LCX138 is a high performance CMOS 3-to-8 available in Japan. DECODER. Designed for use in 3.3 Volt systems, it TC74LCX138F achieves high speed operation while maintaining the CMOS low power dissipation. The device is designed for low-voltage (3.3V) V<sub>CC</sub> applications, but it could be used to interface to 5V supply environment for inputs. When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ( $\overline{Y}0-\overline{Y}7$ ) will go low. When enable input G1 is held low or either  $\overline{G}2A$  or  $\overline{G}2B$ SOP16-P-300-1.27 is held high, decoding function is inhibited and all TC74LCX138FN outputs go high. G1,  $\overline{G}2A$ , and  $\overline{G}2B$  inputs are provided to ease cascade connection and for use as an address decoder for memory systems. All inputs are equipped with protection circuits against static discharge. SOL16-P-150-1.27 **FEATURES** TC74LCX138FT Low voltage operation :  $V_{CC} = 2.0 \sim 3.6V$ High speed operation :  $t_{pd} = 6.0$ ns (Max.)  $(\dot{V}_{CC} = 3.0 \sim 3.6 \text{V})$  $||_{OH}| / |_{OL} = 24 \text{mA} \text{ (Min.)}$ **Output current**  $(V_{CC} = 3.0V)$ 

- Latch-up performance : ±500mA
- Available in JEDEC SOP, EIAJ SOP and TSSOP
- Power down protection is provided on all inputs and outputs. Weight
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 138 type.



TSSOP16-P-0044-0.65 : 0.06g (Typ.)

#### 961001EBA2

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**PIN ASSIGNMENT** 



(TOP VIEW)

#### TRUTH TABLE

INPUTS					OUTPUTS									
ENABLE		SELECT			<u> </u>	<u></u> <u> </u>	<b></b> <u></u>	<b>∀</b> 3	<u>¥</u> 4	<b></b> ¥5	¥6	<b>Y</b> 7	SELECTED OUTPUT	
G1	G2A	G2B	С	В	Α				15	14				
L	X	Х	Х	Х	Х	Н	Н	н	Н	н	Н	н	Н	NONE
Х	н	Х	Х	Х	Х	н	Н	н	н	н	н	н	Н	NONE
Х	X	Н	Х	Х	Х	н	Н	н	Н	н	н	н	Н	NONE
Н	L	L	L	L	L	L	Н	н	н	н	н	н	н	<u></u> ¥0
Н	L	L	L	L	Н	Н	L	н	Н	н	н	н	н	<u></u> <u> </u>
Н	L	L	L	Н	L	н	Н	L	н	н	н	н	н	<u>¥</u> 2
Н	L	L	L	Н	Н	н	Н	н	L	н	н	н	Н	<u>¥</u> 3
Н	L	L	Н	L	L	н	Н	н	н	L	н	н	н	<u>¥</u> 4
Н	L	L	Н	L	Н	Н	Н	н	Н	н	L	н	Н	<u>¥</u> 5
Н	L	L	Н	Н	L	Н	Н	н	н	н	н	L	н	<u>¥</u> 6
Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	<u></u> 77

#### X : Don't Care

#### IEC LOGIC SYMBOL



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#### SYSTEM DIAGRAM



#### MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	Vcc	-0.5~7.0	V
DC Input Voltage	VIN	-0.5~7.0	V
DC Output Voltage	Vaur	-0.5~7.0 (Note 1)	v
DC Output Voltage	VOUT	-0.5~V <sub>CC</sub> +0.5 (Note 2)	v
Input Diode Current	lік	– 50	mA
Output Diode Current	Іок	±50 (Note 3)	mA
DC Output Current	Ιουτ	± 50	mA
Power Dissipation	PD	180	mW
DC V <sub>CC</sub> /Ground Current	ICC/IGND	± 100	mA
Storage Temperature	T <sub>stg</sub>	- 65~150	°C

(Note 1) VCC = 0V

(Note 2) High or Low State.  $I_{OUT}$  absolute maximum rating must be observed. (Note 3)  $V_{OUT}$ <GND,  $V_{OUT}$ > $V_{CC}$ 

### **RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	RATING	UNIT		
Supply Voltage	Vaa	2.0~3.6	v		
Supply Voltage	Vcc	1.5~3.6 (Note 4)			
Input Voltage	VIN	0~5.5	V		
Quitaut Valtaga	Value	0~5.5 (Note 5)	v		
Output Voltage	VOUT	0~ V <sub>CC</sub> (Note 6)			
Output Current	law/law	±24 (Note 7)	<b>س</b> ۸		
Output Current	OH/IOL	± 12 (Note 8)	mA		
Operating Temperature	T <sub>opr</sub>	- 40~85	°C		
Input Rise And Fall Time	dt/dv	0~10 (Note 9)	ns / V		

(Note 4) Data Retention Only

(Note 4) Data Retention Only (Note 5) VCC = 0V (Note 6) High or Low State (Note 7)  $V_{CC} = 3.0 \sim 3.6V$ (Note 8)  $V_{CC} = 2.7 \sim 3.0V$ (Note 9)  $V_{IN} = 0.8 \sim 2.0V$ ,  $V_{CC} = 3.0V$ 

#### **ELECTRICAL CHARACTERISTICS**

DC characteristics (Ta =  $-40 \sim 85^{\circ}$ C)

PARAI	METER	SYMBOL	TEST CON	V <sub>CC</sub> (V)	MIN.	MAX.	UNIT	
Input	"H" Level VIH				2.7~3.6	2.0	—	V
Voltage	"L" Level	VIL			2.7~3.6	_	0.8	v
				I <sub>OH</sub> = -100μA	2.7~3.6	V <sub>CC</sub> - 0.2	_	
	"H" Level	Voн	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = – 12mA	$\begin{array}{c c c c c c c c c c c c c c c c c c c $			
				I <sub>OH</sub> = – 18mA	3.0	2.4	—	
				$I_{OH} = -24mA$	3.0	2.2	—	
voltage	"L" Level	VOL	$V_{IN} = V_{IH}$ or $V_{IL}$	l <sub>OL</sub> = 100μA	2.7~3.6	_	0.2	
				I <sub>OL</sub> = 12mA	2.7	_	0.4	
				I <sub>OL</sub> = 16mA	3.0		0.4	
Output Voltage       "H" Level       VOH $V_{IN} = V_{IH}$ or $V_{IL}$ $IOH = -100\mu A$ $2.7 \sim 3.6$ $V_{CC}$ -0.2         IOH = -12mA $2.7$ $2.2$ $IOH = -12mA$ $2.7$ $2.2$ IOH = -24mA $3.0$ $2.4$ $IOH = -24mA$ $3.0$ $2.4$ IOH = -24mA $3.0$ $2.2$ $IOL = 100\mu A$ $2.7 \sim 3.6$ $$ IOL = 100 $\mu A$ $2.7 \sim 3.6$ $$ $IOL = 100\mu A$ $2.7 \sim 3.6$ $$ Input Leakage Current $IIN$ $V_{IN} = V_{IH}$ or $V_{IL}$ $IOL = 100\mu A$ $2.7 \sim 3.6$ $$ Input Leakage Current $IIN$ $V_{IN} = 0 \sim 5.5V$ $2.7 \sim 3.6$ $$ Power Off Leakage       IOFF $VIN / VOUT = 5.5V$ $0$ $$ Quiescent Supply       ICC $VIN = V_{CC}$ or GND $2.7 \sim 3.6$ $$ Quiescent Supply       ICC $VIN = V_{CC}$ or GND $2.7 \sim 3.6$ $$ Increase In Icc Per       ICC $VIN / VOUT = 3.6 \sim 5.5V$ $2.7 \sim 3.6$ $$	0.55							
Input Leaka	ge Current	<sup>I</sup> IN	V <sub>IN</sub> = 0~5.5V		2.7~3.6	_	± 5.0	μA
-		lOFF	V <sub>IN</sub> / V <sub>OUT</sub> = 5.5V		0	_	10.0	μΑ
Quiescent Supply			V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7~3.6		10.0	•
Current		ICC	$V_{IN} / V_{OUT} = 3.6 \sim 5.$	5V	2.7~3.6		± 10.0	μΑ
Increase In I <sub>CC</sub> Per Input		۵ICC	V <sub>IH</sub> = V <sub>CC</sub> – 0.6V		2.7~3.6	_	500	μΑ

AC characteristics (Ta =  $-40 \sim 85^{\circ}$ C)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	MIN.	MAX.	UNIT
Propagation Delay	t <sub>pLH</sub>	(Fig.1, 2)	2.7	_	7.0	20
Time (A, B, C- <u>Y</u> )	t <sub>pHL</sub>	(FIG. 1, 2)	3.3±0.3	1.5	6.0	ns
Propagation Delay	t <sub>pLH</sub>	(Fig.1, 2)	2.7	_	8.0	20
Time (G1- $\overline{Y}$ )	t <sub>pHL</sub>	(FIG. 1, 2)	3.3 ± 0.3	1.5	7.0	ns
Propagation Delay	t <sub>pLH</sub>	(Fig 1 2)	2.7	_	7.0	
Time ( $\overline{G}2-\overline{Y}$ )	t <sub>pHL</sub>	(Fig.1, 2)	3.3 ± 0.3	1.5	6.0	ns
Output To Output	tosLH	(Note 10)	2.7	_	_	20
Skew	t <sub>osHL</sub>		3.3±0.3	_	1.0	ns

(Note 10) Parameter guaranteed by design.

 $(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$ 

#### **CAPACITIVE CHARACTERISTICS** (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	ТҮР	UNIT
Input Capacitance	C <sub>IN</sub>			3.3	7	рF
Output Capacitance	COUT	—		0	8	рF
Power Dissipation Capacitance	C <sub>PD</sub>	f <sub>IN</sub> = 10MHz	(Note 11)	3.3	25	pF

(Note 11) CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation :

 $I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$ 

# **TOSHIBA**

### **TEST CIRCUIT**

Fig.1



### AC WAVEFORM

Fig.2 t<sub>pLH</sub>, t<sub>pHL</sub>





Weight : 0.18g (Typ.)

Unit : mm

#### OUTLINE DRAWING SOL16-P-150-1.27



Weight : 0.12g (Typ.)

## **TOSHIBA**

Unit : mm

#### OUTLINE DRAWING TSSOP16-P-0044-0.65







Weight : 0.06g (Typ.)

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