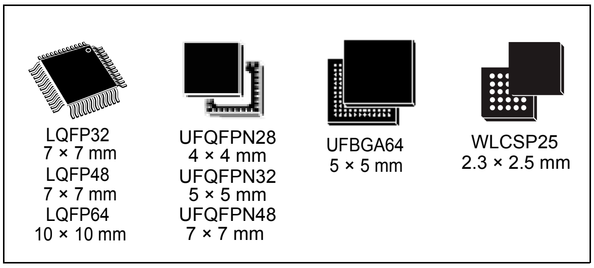
STM32G071x8/xB

Arm® Cortex®-M0+ 32-bit MCU, up to 128 KB Flash, 36 KB RAM, 4x USART, timers, ADC, DAC, comm. I/Fs, 1.7-3.6V

Datasheet - production data

Features

- Core: Arm® 32-bit Cortex®-M0+ CPU, frequency up to 64 MHz
- -40°C to 85°C/105°C/125°C operating temperature
- Memories
  - Up to 128 Kbytes of Flash memory with protection and securable area
  - 36 Kbytes of SRAM (32 Kbytes with HW parity check)
- CRC calculation unit
- Reset and power management
  - Voltage range: 1.7 V to 3.6 V
  - Power-on/Power-down reset (POR/PDR)
  - Programmable Brownout reset (BOR)
  - Programmable voltage detector (PVD)
  - Low-power modes: Sleep, Stop, Standby, Shutdown
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator with calibration
  - Internal 16 MHz RC with PLL option (±1 %)
  - Internal 32 kHz RC oscillator (±5 %)
- Up to 60 fast I/Os
  - All mappable on external interrupt vectors
  - Multiple 5 V-tolerant I/Os
- 7-channel DMA controller with flexible mapping
- 12-bit, 0.4 µs ADC (up to 16 ext. channels)
  - Up to 16-bit with hardware oversampling
  - Conversion range: 0 to 3.6V
- Two 12-bit DACs, low-power sample-and-hold
- Two fast low-power analog comparators, with programmable input and output, rail-to-rail
- 14 timers (two 128 MHz capable): 16-bit for advanced motor control, one 32-bit and five 16-bit general-purpose, two basic 16-bit, two low-power 16-bit, two watchdogs, SysTick timer
- Calendar RTC with alarm and periodic wakeup from Stop/Standby/Shutdown



- Communication interfaces
  - Two I^2C-bus interfaces supporting Fast-mode Plus (1 Mbit/s) with extra current sink, one supporting SMBus/PMBus and wakeup from Stop mode
  - Four USARTs with master/slave synchronous SPI; two supporting ISO7816 interface, LIN, IrDA capability, auto baud rate detection and wakeup feature
  - One low-power UART
  - Two SPIs (32 Mbit/s) with 4- to 16-bit programmable bitframe, one multiplexed with I^2S interface
  - HDMI CEC interface, wakeup on header
- USB Type-C™ Power Delivery controller
- Development support: serial wire debug (SWD)
- 96-bit unique ID
- All packages ECOPACK®2 compliant

Table 1. Device summary

Reference	Part number
STM32G071x8	STM32G071C8, STM32G071G8, STM32G071K8, STM32G071R8
STM32G071xB	STM32G071RB, STM32G071CB, STM32G071KB, STM32G071GB, STM32G071EB

Contents

List of tables

List of figures

1 Introduction

This document provides information on STM32G071x8/xB microcontrollers, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging, and ordering codes.

Information on memory mapping and control registers is object of reference manual.

Information on Arm®(a) Cortex®-M0+ core is available from the www.arm.com website.

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2 Description

The STM32G071x8/xB mainstream microcontrollers are based on high-performance Arm® Cortex®-M0+ 32-bit RISC core operating at up to 64 MHz frequency. Offering a high level of integration, they are suitable for a wide range of applications in consumer, industrial and appliance domains and ready for the Internet of Things (IoT) solutions.

The devices incorporate a memory protection unit (MPU), high-speed embedded memories (up to 128 Kbytes of Flash program memory with read protection, write protection, proprietary code protection, and securable area, and 36 Kbytes of SRAM), DMA and an extensive range of system functions, enhanced I/Os and peripherals. The devices offer standard communication interfaces (two I^2Cs, two SPIs / one I^2S, one HDMI CEC, and four USARTs), one 12-bit ADC (2.5 MSps) with up to 19 channels, one 12-bit DAC with two channels, two fast comparators, an internal voltage reference buffer, a low-power RTC, an advanced control PWM timer running at up to double the CPU frequency, five general-purpose 16-bit timers with one running at up to double the CPU frequency, a 32-bit general-purpose timer, two basic timers, two low-power 16-bit timers, two watchdog timers, and a SysTick timer. The STM32G071x8/xB devices provide a fully integrated USB Type-C Power Delivery controller.

The devices operate within ambient temperatures from -40 to 125°C. They can operate with supply voltages from 1.7 V to 3.6 V. Optimized dynamic consumption combined with a comprehensive set of power-saving modes, low-power timers and low-power UART, allows the design of low-power applications.

VBAT direct battery input allows keeping RTC and backup registers powered.

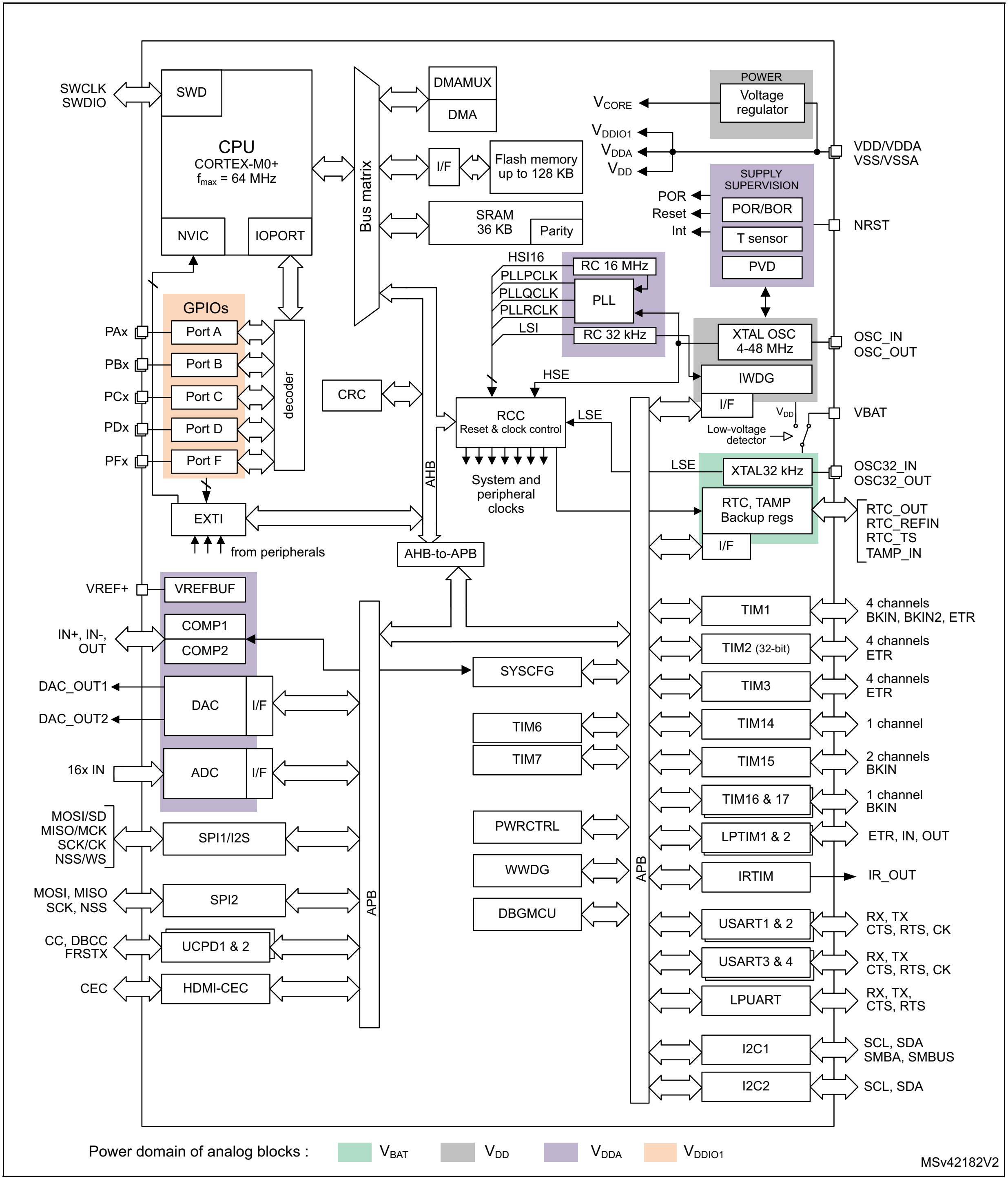
The devices come in packages with 28 to 64 pins.

Table 2. STM32G071x8/xB family device features and peripheral counts

Peripheral		STM32G071_												
		_EB	**_G8**	**_GB**	**_G8 xxN**	**_GB xxN**	**_K8**	**_KB**	**_K8 xxN**	**_KB xxN**	**_C8**	**_CB**	**_R8**	**_RB**
Flash memory (Kbyte)		128	64	128	64	128	64	128	64	128	64	128	64	128
SRAM (Kbyte)		32 (with parity) or 36 (without parity)												
Timers	Advanced control	1 (16-bit) high frequency												
	General-purpose	4 (16-bit) + 1 (16-bit) high frequency + 1 (32-bit)												
	Basic	2 (16-bit)												
	Low-power	2 (16-bit)												
	SysTick	1												
	Watchdog	2												
Comm. interfaces	SPI [I^2S][1]	2 [1]												
	I^2C	2												
	USART	4												
	LPUART	1												
	UCPD	(2)			2		(2)		2					
	CEC	1												
RTC		Yes												
Tamper pins		2												
Random number generator		No												
AES		No												
GPIOs		23	26				30				44		60	
Wakeup pins		4			3		4		3		4		5	
12-bit ADC channels		10 ext. + 2 int.			9 ext. + 2 int.		11 ext. + 2 int.		10 ext. + 2 int.		14 ext. + 3 int.		16 ext. + 3 int.	
12-bit DAC channels		2												
Internal voltage reference buffer		No									Yes			
Analog comparators		2												
Max. CPU frequency		64 MHz												
Operating voltage		1.7 to 3.6 V												
Operating temperature[3]		Ambient: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C												
Number of pins		25	28				32				48		64	

1. The numbers in brackets denote the count of SPI interfaces configurable as I^2S interface.
2. One port with only one CC line available (supporting limited number of use cases).
3. Depends on order code. Refer to *Section 7: Ordering information* for details.

Figure 1. Block diagram



3 Functional overview

3.1 Arm® Cortex®-M0+ core with MPU

The Cortex-M0+ is an entry-level 32-bit Arm Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture, easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area- and power-optimized 32-bit core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to embedded Arm core, the STM32G071x8/xB devices are compatible with Arm tools and software.

The Cortex-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC) described in *Section 3.13.1*.

3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded Flash memory

STM32G071x8/xB devices feature up to 128 Kbytes of embedded Flash memory available for storing code and data.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M0+ serial wire), boot in RAM and bootloader selection are disabled. This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
User memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. Erased upon RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU as instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. An additional option bit (PCROP_RDP) determines whether the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection
- readout of the ECC fail address from the ECC register

3.3.1 Securable area

A part of the Flash memory can be hidden from the application once the code it contains is executed. As soon as the write-once SEC_PROT bit is set, the securable memory cannot be accessed until the system resets. The securable area generally contains the secure boot code to execute only once at boot. This helps to isolate secret code from untrusted application code.

3.4 Embedded SRAM

STM32G071x8/xB devices have 32 Kbytes of embedded SRAM with parity. Hardware parity check allows memory data errors to be detected, which contributes to increasing functional safety of applications.

When the parity protection is not required because the application is not safety-critical, the parity memory bits can be used as additional SRAM, to increase its total size to 36 Kbytes.

The memory can be read/write-accessed at CPU clock speed, with 0 wait states.

3.5 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System memory
- boot from embedded SRAM

The boot pin is shared with a standard GPIO and can be enabled through the boot selector option bit. The boot loader is located in System memory. It manages the Flash memory reprogramming through USART on pins PA9/PA10, PC10/PC11 or PA2/PA3, through I^{2}C-bus on pins PB6/PB7 or PB10/PB11, or through SPI on pins PA4/PA5/PA6/PA7 or PB12/PB13/PB14/PB15.

3.6 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

3.7 Power supply management

3.7.1 Power supply schemes

The STM32G071x8/xB devices require a 1.7 V to 3.6 V operating supply voltage (V_{DD}). Several different power supplies are provided to specific peripherals:

- V_{DD} = 1.7 (1.6) to 3.6 V

  V_{DD} is the external power supply for the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD/VDDA pin.

  The minimum voltage of 1.7 V corresponds to power-on reset release threshold V_{POR}(max). Once this threshold is crossed and power-on reset is released, the functionality is guaranteed down to power-down reset threshold V_{PDR}(min).

- V_{DDA} = 1.62 V (ADC and COMP) / 1.8 V (DAC) / 2.4 V (VREFBUF) to 3.6 V

  V_{DDA} is the analog power supply for the A/D converter, D/A converter, voltage reference buffer and comparators. V_{DDA} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- V_{DDIO1} = V_{DD}

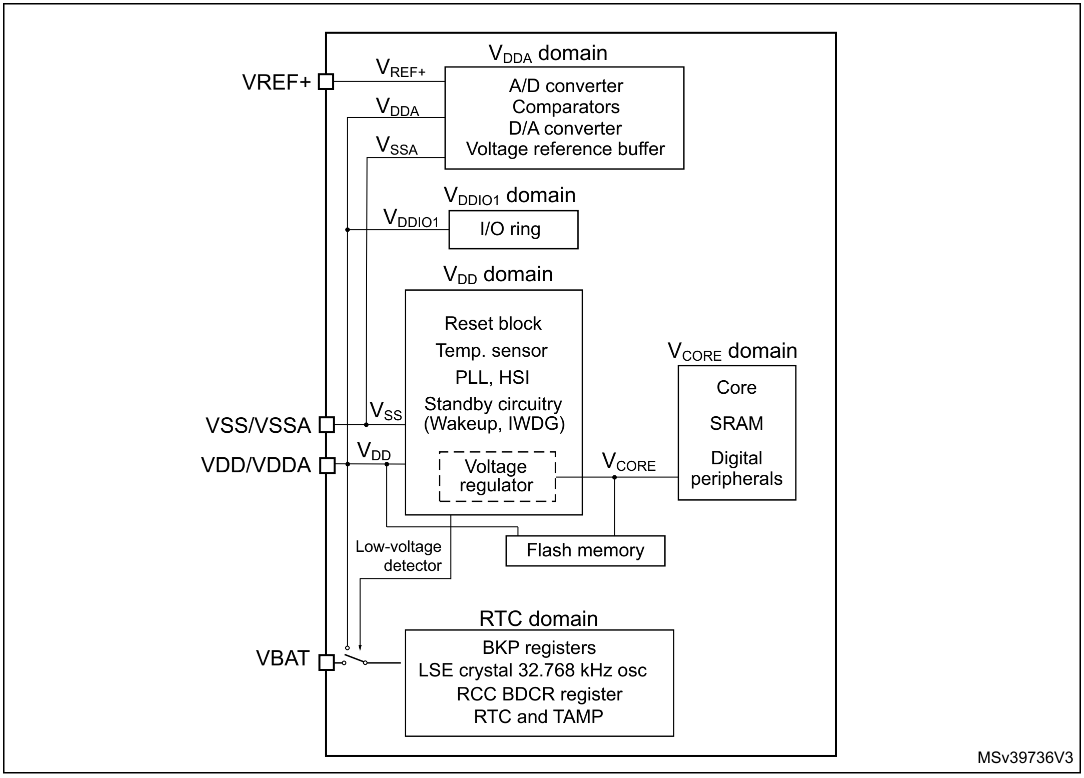
  V_{DDIO1} is the power supply for the I/Os. V_{DDIO1} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- V_{BAT} = 1.55 V to 3.6 V. V_{BAT} is the power supply (through a power switch) for RTC, TAMP, low-speed external 32.768 kHz oscillator and backup registers when V_{DD} is not present. V_{BAT} is provided externally through VBAT pin. When this pin is not available on the package, VBAT bonding pad is internally bonded to the VDD/VDDA pin.
- V_{REF+} is the analog peripheral input reference voltage, or the output of the internal voltage reference buffer (when enabled). When V_{DDA} < 2 V, V_{REF+} must be equal to V_{DDA}. When V_{DDA} ≥ 2 V, V_{REF+} must be between 2 V and V_{DDA}. It can be grounded when the analog peripherals using V_{REF+} are not active.

  The internal voltage reference buffer supports two output voltages, which is configured with VRS bit of the VREFBUF_CSR register:
  - V_{REF+} around 2.048 V (requiring V_{DDA} equal to or higher than 2.4 V)
  - V_{REF+} around 2.5 V (requiring V_{DDA} equal to or higher than 2.8 V)

  V_{REF+} is delivered through VREF+ pin. On packages without VREF+ pin, V_{REF+} is internally connected with V_{DD}, and the internal voltage reference buffer must be kept disabled (refer to datasheets for package pinout description).
- V_{CORE}

  An embedded linear voltage regulator is used to supply the V_{CORE} internal digital power. V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. The Flash memory is also supplied with V_{DD}.

Figure 2. Power supply overview



3.7.2 Power supply supervisor

The device has an integrated power-on/power-down (POR/PDR) reset active in all power modes except Shutdown and ensuring proper operation upon power-on and power-down. It maintains the device in reset when the supply voltage is below $V_{POR/PDR}$ threshold, without the need for an external reset circuit. Brownout reset (BOR) function allows extra flexibility. It can be enabled and configured through option bytes, by selecting one of four thresholds for rising V_{DD} and other four for falling V_{DD}.

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to V_{PVD} threshold. It allows generating an interrupt when V_{DD} level crosses the V_{PVD} threshold, selectively while falling, while rising, or while falling and rising. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.7.3 Voltage regulator

Two embedded linear voltage regulators, main regulator (MR) and low-power regulator (LPR), supply most of digital circuitry in the device.

The MR is used in Run and Sleep modes. The LPR is used in Low-power run, Low-power sleep and Stop modes.

In Standby and Shutdown modes, both regulators are powered down and their outputs set in high-impedance state, such as to bring their current consumption close to zero. However, SRAM data retention is possible in Standby mode, in which case the LPR remains active and it only supplies the SRAM.

3.7.4 Low-power modes

By default, the microcontroller is in Run mode after system or power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run** mode

  This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep** mode

  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low-power run mode.
- **Stop 0 and Stop 1** modes

  In Stop 0 and Stop 1 modes, the device achieves the lowest power consumption while retaining the SRAM and register contents. All clocks in the V_{CORE} domain are stopped. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are disabled. The LSE or LSI keep running. The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode, so as to get clock for processing the wakeup event. The main regulator remains active in Stop 0 mode while it is turned off in Stop 1 mode.
- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption, with POR/PDR always active in this mode. The main regulator is switched off to power down V_{CORE} domain. The low-power regulator is either switched off or kept active. In the latter case, it only supplies SRAM to ensure data retention. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are also powered down. The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  For each I/O, the software can determine whether a pull-up, a pull-down or no resistor shall be applied to that I/O during Standby mode.

  Upon entering Standby mode, register contents are lost except for registers in the RTC domain and standby circuitry. The SRAM contents can be retained through register setting.

  The device exits Standby mode upon external reset event (NRST pin), IWDG reset event, wakeup event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wakeup, timestamp, tamper), or when a failure is detected on LSE (CSS on LSE).
- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off to power down the V_{CORE} domain. The PLL, as well as the

HSI16 and LSI RC-oscillators and HSE crystal oscillator are also powered down. The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode. Therefore, switching to RTC domain is not supported.

SRAM and register contents are lost except for registers in the RTC domain.

The device exits Shutdown mode upon external reset event (NRST pin), IWDG reset event, wakeup event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wakeup, timestamp, tamper).

3.7.5 Reset mode

During and upon exiting reset, the schmitt triggers of I/Os are disabled so as to reduce power consumption. In addition, when the reset source is internal, the built-in pull-up resistor on NRST pin is deactivated.

3.7.6 VBAT operation

The V_{BAT} power domain, consuming very little energy, includes RTC, and LSE oscillator and backup registers.

In VBAT mode, the RTC domain is supplied from VBAT pin. The power source can be, for example, an external battery or an external supercapacitor. Two anti-tamper detection pins are available.

The RTC domain can also be supplied from VDD/VDDA pin.

By means of a built-in switch, an internal voltage supervisor allows automatic switching of RTC domain powering between V_{DD} and voltage from VBAT pin to ensure that the supply voltage of the RTC domain (V_{BAT}) remains within valid operating conditions. If both voltages are valid, the RTC domain is supplied from VDD/VDDA pin.

An internal circuit for charging the battery on VBAT pin can be activated if the V_{DD} voltage is within a valid range.

Note: External interrupts and RTC alarm/events cannot cause the microcontroller to exit the VBAT mode, as in that mode the V_{DD} *is not within a valid range.*

3.8 Interconnect of peripherals

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

Table 4. Interconnect of STM32G071x8/xB peripherals

Interconnect source	Interconnect destination	Interconnect action	Run Low-power run	Sleep Low-power sleep	Stop
TIMx	TIMx	Timer synchronization or chaining	Y	Y	-
	ADCx DACx	Conversion triggers	Y	Y	-
	DMA	Memory-to-memory transfer trigger	Y	Y	-
	COMPx	Comparator output blanking	Y	Y	-
COMPx	TIM1,2,3	Timer input channel, trigger, break from analog signals comparison	Y	Y	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y
ADCx	TIM1	Timer triggered by analog watchdog	Y	Y	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y
All clocks sources (internal and external)	TIM14,16,17	Clock source used as input channel for RC measurement and trimming	Y	Y	-
CSS RAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1,15,16,17	Timer break	Y	Y	-
CPU (hard fault)	TIM1,15,16,17	Timer break	Y	-	-
GPIO	TIMx	External trigger	Y	Y	-
	LPTIMERx	External trigger	Y	Y	Y
	ADC DACx	Conversion external trigger	Y	Y	-

3.9 Clocks and startup

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** three different sources can deliver SYSCLK system clock:
  - 4-48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). It can supply clock to system PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software. It can supply clock to system PLL.
  - System PLL with maximum output frequency of 64 MHz. It can be fed with HSE or HSI16 clocks.
- **Auxiliary clock source:** two ultra-low-power clock sources for the real-time clock (RTC):
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ±5% accuracy, also used to clock an independent watchdog.
- **Peripheral clock sources:** several peripherals (I2S, USARTs, I2Cs, LPTIMs, ADC) have their own clock independent of the system clock.
- **Clock security system (CSS):** in the event of HSE clock failure, the system clock is automatically switched to HSI16 and, if enabled, a software interrupt is generated. LSE clock failure can also be detected and generate an interrupt. The CCS feature can be enabled by software.
- Clock output:
  - **MCO (microcontroller clock output)** provides one of the internal clocks for external use by the application
  - **LSCO (low speed clock output)** provides LSI or LSE in all low-power modes (except in VBAT operation).

Several prescalers allow the application to configure AHB and APB domain clock frequencies, 64 MHz at maximum.

3.10 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function (AF). Most of the GPIO pins are shared with special digital or analog functions.

Through a specific sequence, this special function configuration of I/Os can be locked, such as to avoid spurious writing to I/O control registers.

3.11 Direct memory access controller (DMA)

The direct memory access (DMA) controller is a bus master and system peripheral with single-AHB architecture.

With 7 channels, it performs data transfers between memory-mapped peripherals and/or memories, to offload the CPU.

Each channel is dedicated to managing memory access requests from one or more peripherals. The unit includes an arbiter for handling the priority between DMA requests.

Main features of the DMA controller:

- Single-AHB master
- Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-to-peripheral data transfers
- Access, as source and destination, to on-chip memory-mapped devices such as Flash memory, SRAM, and AHB and APB peripherals
- All DMA channels independently configurable:
  - Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
  - Priority between the requests is programmable by software (four levels per channel: very high, high, medium, low) and by hardware in case of equality (such as request to channel 1 has priority over request to channel 2).
  - Transfer size of source and destination are independent (byte, half-word, word), emulating packing and unpacking. Source and destination addresses must be aligned on the data size.
  - Support of transfers from/to peripherals to/from memory with circular buffer management
  - Programmable number of data to be transferred: 0 to 2^{16} - 1
- Generation of an interrupt request per channel. Each interrupt request originates from any of the three DMA events: transfer complete, half transfer, or transfer error.

3.12 DMA request multiplexer (DMAMUX)

The DMAMUX request multiplexer enables routing a DMA request line between the peripherals and the DMA controller. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. DMAMUX may also be used as a DMA request generator from programmable events on its input trigger signals.

3.13 Interrupts and events

The device flexibly manages events causing interrupts of linear program execution, called exceptions. The Cortex-M0+ processor core, a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI) are the assets contributing to handling the exceptions. Exceptions include core-internal events such as, for example, a division by zero and, core-external events such as logical level changes on physical lines. Exceptions result in interrupting the program flow, executing an interrupt service routine (ISR) then resuming the original program flow.

The processor context (contents of program pointer and status registers) is stacked upon program interrupt and unstacked upon program resume, by hardware. This avoids context stacking and unstacking in the interrupt service routines (ISRs) by software, thus saving time, code and power. The ability to abandon and restart load-multiple and store-multiple operations significantly increases the device's responsiveness in processing exceptions.

3.13.1 Nested vectored interrupt controller (NVIC)

The configurable nested vectored interrupt controller is tightly coupled with the core. It handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupts, and Cortex-M0+ exceptions. It provides flexible priority management.

The tight coupling of the processor core with NVIC significantly reduces the latency between interrupt events and start of corresponding interrupt service routines (ISRs). The ISR vectors are listed in a vector table, stored in the NVIC at a base address. The vector address of an ISR to execute is hardware-built from the vector table base address and the ISR order number used as offset.

If a higher-priority interrupt event happens while a lower-priority interrupt event occurring just before is waiting for being served, the later-arriving higher-priority interrupt event is served first. Another optimization is called tail-chaining. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context unstacking and stacking is skipped. This reduces latency and contributes to power efficiency.

Features of the NVIC:

- Low-latency interrupt processing
- 4 priority levels
- Handling of a non-maskable interrupt (NMI)
- Handling of 32 maskable interrupt lines
- Handling of 10 Cortex-M0+ exceptions
- Later-arriving higher-priority interrupt processed first
- Tail-chaining
- Interrupt vector retrieval by hardware

3.13.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller adds flexibility in handling physical line events and allows identifying wake-up events at processor wakeup from Stop mode.

The EXTI controller has a number of channels, of which some with rising, falling or rising, and falling edge detector capability. Any GPIO and a few peripheral signals can be connected to these channels.

The channels can be independently masked.

The EXTI controller can capture pulses shorter than the internal clock period.

A register in the EXTI controller latches every event even in Stop mode, which allows the software to identify the origin of the processor's wake-up from Stop mode or, to identify the GPIO and the edge event having caused an interrupt.

3.14 Analog-to-digital converter (ADC)

A native 12-bit analog-to-digital converter is embedded into STM32G071x8/xB devices. It can be extended to 16-bit resolution through hardware oversampling. The ADC has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference, V_{BAT} monitoring). It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of ~2 MSps even with a low CPU speed. An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate in the whole V_{DD} supply range.

The ADC features a hardware oversampler up to 256 samples, improving the resolution to 16 bits (refer to AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions with timers.

3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to an ADC input to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor may vary from part to part due to process variation, the uncalibrated internal temperature sensor is suitable only for relative temperature measurements.

To improve the accuracy of the temperature sensor, each part is individually factory-calibrated by ST. The resulting calibration data are stored in the part’s engineering bytes, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.14.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to an ADC input. The V_{REFINT} voltage is individually precisely measured for each part by ST during production test and stored in the part's engineering bytes. It is accessible in read-only mode.

Table 6. Internal voltage reference calibration values

Calibration value name	Description	Memory address
V_{REFINT}	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.14.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using an internal ADC input. As the V_{BAT} voltage may be higher than V_{DDA} and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by three. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.15 Digital-to-analog converter (DAC)

The 2-channel 12-bit buffered DAC converts a digital value into an analog voltage available on the channel output. The architecture of either channel is based on integrated resistor string and an inverting amplifier. The digital circuitry is common for both channels.

Features of the DAC:

- Two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Independent or simultaneous conversion for DAC channels
- DMA capability for either DAC channel
- Triggering with timer events, synchronized with DMA
- Triggering with external events
- Sample-and-hold low-power mode, with internal or external capacitor

3.16 Voltage reference buffer (VREFBUF)

When enabled, an embedded buffer provides the internal reference voltage to analog blocks (for example ADC) and to VREF+ pin for external components.

The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is disabled.

On some packages, the VREF+ pad of the silicon die is double-bonded with supply pad to common VDD/VDDA pin and so the internal voltage reference buffer cannot be used.

3.17 Comparators (COMP)

Two embedded rail-to-rail analog comparators have programmable reference voltage (internal or external), hysteresis, speed (low for low-power) and output polarity.

The reference voltage can be one of the following:

- external, from an I/O
- internal, from DAC
- internal reference voltage (V_{REFINT}) or its submultiple (1/4, 1/2, 3/4)

The comparators can wake up the device from Stop mode, generate interrupts, breaks or triggers for the timers and can be also combined into a window comparator.

3.18 Timers and watchdogs

The device includes an advanced-control timer, six general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer. *Table 7* compares features of the advanced-control, general-purpose and basic timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Maximum operating frequency	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary outputs
Advanced-control	TIM1	16-bit	Up, down, up/down	128 MHz	Integer from 1 to 2^{16}	Yes	4	3

Table 7. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Maximum operating frequency	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary outputs
General-purpose	TIM2	32-bit	Up, down, up/down	64 MHz	Integer from 1 to 2^{16}	Yes	4	-
	TIM3	16-bit	Up, down, up/down	64 MHz	Integer from 1 to 2^{16}	Yes	4	-
	TIM14	16-bit	Up	64 MHz	Integer from 1 to 2^{16}	No	1	-
	TIM15	16-bit	Up	128 MHz	Integer from 1 to 2^{16}	Yes	2	1
	TIM16 TIM17	16-bit	Up	64 MHz	Integer from 1 to 2^{16}	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	64 MHz	Integer from 1 to 2^{16}	Yes	-	-
Low-power	LPTIM1 LPTIM2	16-bit	Up	64 MHz	2^n where n=0 to 7	No	N/A	-

3.18.1 Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM unit multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM output (edge or center-aligned modes) with full modulation capability (0-100%)
- one-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled, so as to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.18.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.18.2 General-purpose timers (TIM2, 3, 14, 15, 16, 17)

There are six synchronizable general-purpose timers embedded in the device (refer to *Table 7* for comparison). Each general-purpose timer can be used to generate PWM outputs or act as a simple timebase.

- TIM2, TIM3

  These are full-featured general-purpose timers:
  - TIM2 with 32-bit auto-reload up/downcounter and 16-bit prescaler
  - TIM3 with 16-bit auto-reload up/downcounter and 16-bit prescaler

  They have four independent channels for input capture/output compare, PWM or one-pulse mode output. They can operate together or in combination with other general-purpose timers via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request and support quadrature encoders. Their counters can be frozen in debug mode.
- TIM14

  This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. It has one channel for input capture/output compare, PWM output or one-pulse mode output. Its counter can be frozen in debug mode.
- TIM15, TIM16, TIM17

  These are general-purpose timers featuring:
  - 16-bit auto-reload upcounter and 16-bit prescaler
  - 2 channels and 1 complementary channel for TIM15
  - 1 channel and 1 complementary channel for TIM16 and TIM17

  All channels can be used for input capture/output compare, PWM or one-pulse mode output. The timers can operate together via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request. Their counters can be frozen in debug mode.

3.18.3 Basic timers (TIM6 and TIM7)

These timers are mainly used for triggering DAC conversions. They can also be used as generic 16-bit timebases.

3.18.4 Low-power timers (LPTIM1 and LPTIM2)

These timers have an independent clock. When fed with LSE, LSI or external clock, they keep running in Stop mode and they can wake up the system from it.

Features of LPTIM1 and LPTIM2:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output (pulse, PWM)
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Selectable clock source:
  - Internal: LSE, LSI, HSI16 or APB clocks
  - External: over LPTIM input (working even with no internal clock source running, used by pulse counter application)
- Programmable digital glitch filter
- Encoder mode

3.18.5 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 32 kHz internal RC (LSI). Independent of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. Its counter can be frozen in debug mode.

3.18.6 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked by the system clock. It has an early-warning interrupt capability. Its counter can be frozen in debug mode.

3.18.7 SysTick timer

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter.

Features of SysTick timer:

- 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.19 Real-time clock (RTC), tamper (TAMP) and backup registers

The device embeds an RTC and five 32-bit backup registers, located in the RTC domain of the silicon die.

The ways of powering the RTC domain are described in *Section 3.7.6*.

The RTC is an independent BCD timer/counter.

Features of the RTC:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Programmable alarm
- On-the-fly correction from 1 to 32767 RTC clock pulses, usable for synchronization with a master clock
- Reference clock detection - a more precise second-source clock (50 or 60 Hz) can be used to improve the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Two anti-tamper detection pins with programmable filter
- Timestamp feature to save a calendar snapshot, triggered by an event on the timestamp pin or a tamper event, or by switching to VBAT mode
- 17-bit auto-reload wakeup timer (WUT) for periodic events, with programmable resolution and period
- Multiple clock sources and references:
  - A 32.768 kHz external crystal (LSE)
  - An external resonator or oscillator (LSE)
  - The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
  - The high-speed external clock (HSE) divided by 32

When clocked by LSE, the RTC operates in VBAT mode and in all low-power modes. When clocked by LSI, the RTC does not operate in VBAT mode, but it does in low-power modes except for the Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wake the device up from the low-power modes.

The backup registers allow keeping 20 bytes of user application data in the event of V_{DD} failure, if a valid backup supply voltage is provided on VBAT pin. They are not affected by the system reset, power reset, and upon the device’s wakeup from Standby or Shutdown modes.

3.20 Inter-integrated circuit interface (I2C)

The device embeds two I2C peripherals. Refer to *Table 8* for the features.

The I^2C-bus interface handles communication between the microcontroller and the serial I^2C-bus. It controls all I^2C-bus-specific sequencing, protocol, arbitration and timing.

Features of the I2C peripheral:

- I^{2}C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and extra output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Clock stretching
- SMBus specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Command and data acknowledge control
  - Address resolution protocol (ARP) support
  - Host and Device support
  - SMBus alert
  - Timeouts and idle condition detection
- PMBus rev 1.3 standard compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent of the PCLK reprogramming
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 8. I^{2}C implementation

I^{2}C features[(1)]	I2C1	I2C2
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s) with extra output drive I/Os	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	-
Independent clock	X	-
Wakeup from Stop mode on address match	X	-

1. X: supported

3.21 Universal synchronous/asynchronous receiver transmitter (USART)

The device embeds universal synchronous/asynchronous receivers/transmitters (USART1, USART2, USART3, USART4) that communicate at speeds of up to 8 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. Some can also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and have a clock domain independent of the CPU clock, which allows them to wake up the MCU from Stop mode. The wakeup events from Stop mode are programmable and can be:

- start bit detection
- any received data frame
- a specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 9. USART implementation

USART modes/features[1]	USART1 USART2	USART3 USART4
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X: supported

3.22 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one LPUART. The peripheral supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent of the CPU clock, and can wakeup the system from Stop mode. The Stop mode wakeup events are programmable and can be:

- start bit detection
- any received data frame
- a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

3.23 Serial peripheral interface (SPI)

The device contains two SPIs running at up to 32 Mbits/s in master and slave modes. It supports half-duplex, full-duplex and simplex communications. A 3-bit prescaler gives eight master mode frequencies. The frame size is configurable from 4 bits to 16 bits. The SPI peripherals support NSS pulse mode, TI mode and hardware CRC calculation.

The SPI peripherals can be served by the DMA controller.

The I^{2}S interface mode of the SPI peripheral (if supported, see the following table) supports four different audio standards can operate as master or slave, in half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 10. SPI/I2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I^{2}S mode	X	-
TI mode	X	X

1. X = supported.

3.24 USB Type-C™ Power Delivery controller

The device embeds two controllers (UCPD1 and UCPD2) compliant with USB Type-C Rev. 1.2 and USB Power Delivery Rev. 3.0 specifications.

The controllers use specific I/Os supporting the USB Type-C and USB Power Delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- “Dead battery” support
- USB Power Delivery message transmission and reception
- FRS (fast role swap) support

The digital controller handles notably:

- USB Type-C level detection with de-bounce, generating interrupts
- FRS detection, generating an interrupt
- byte-level interface for USB Power Delivery payload, generating interrupts (DMA compatible)
- USB Power Delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode
- ordered sets (with a programmable ordered set mask at receive)
- frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages and FRS signaling.

3.25 Development support

3.25.1 Serial wire debug port (SW-DP)

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts, pin description and alternate functions

The devices housed in packages with 48 or more pins provide 2-port USB-C Power Delivery. The devices housed in 32-pin packages come in two variants - “GP” with a single-port limited USB-C Power Delivery and “PD” with 2-port USB-C Power Delivery.

Figure 3. STM32G071RxT LQFP64 pinout

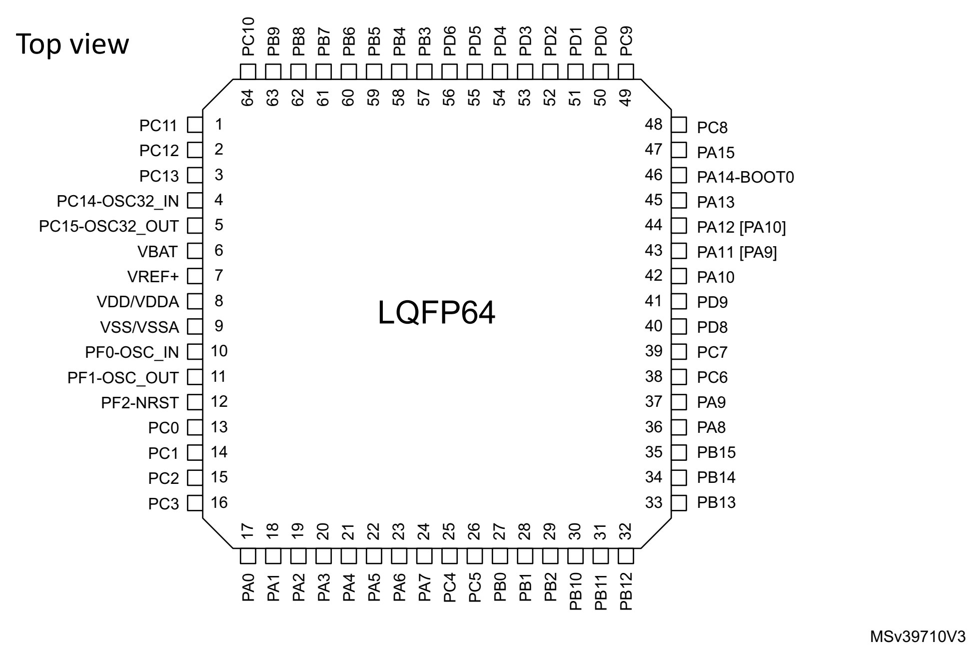
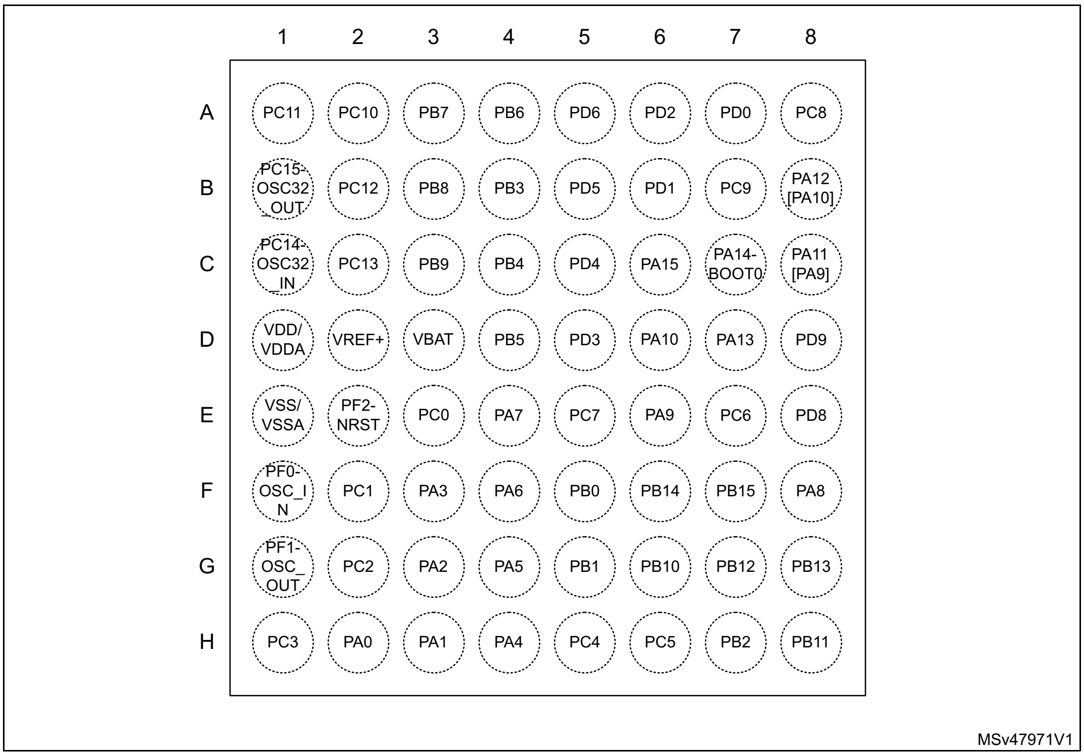


Figure 4. STM32G071RxI UFBGA64 pinout



	1	2	3	4	5	6	7	8
A	PC11	PC10	PB7	PB6	PD6	PD2	PD0	PC8
B	PC15-OSC32_OUT	PC12	PB8	PB3	PD5	PD1	PC9	PA12 [PA10]
C	PC14-OSC32_IN	PC13	PB9	PB4	PD4	PA15	PA14-BOOT0	PA11 [PA9]
D	VDD/ VDDA	VREF+	VBAT	PB5	PD3	PA10	PA13	PD9
E	VSS/ VSSA	PF2-NRST	PC0	PA7	PC7	PA9	PC6	PD8
F	PF0-OSC_IN	PC1	PA3	PA6	PB0	PB14	PB15	PA8
G	PF1-OSC_OUT	PC2	PA2	PA5	PB1	PB10	PB12	PB13
H	PC3	PA0	PA1	PA4	PC4	PC5	PB2	PB11

Figure 5. STM32G071CxT LQFP48 pinout

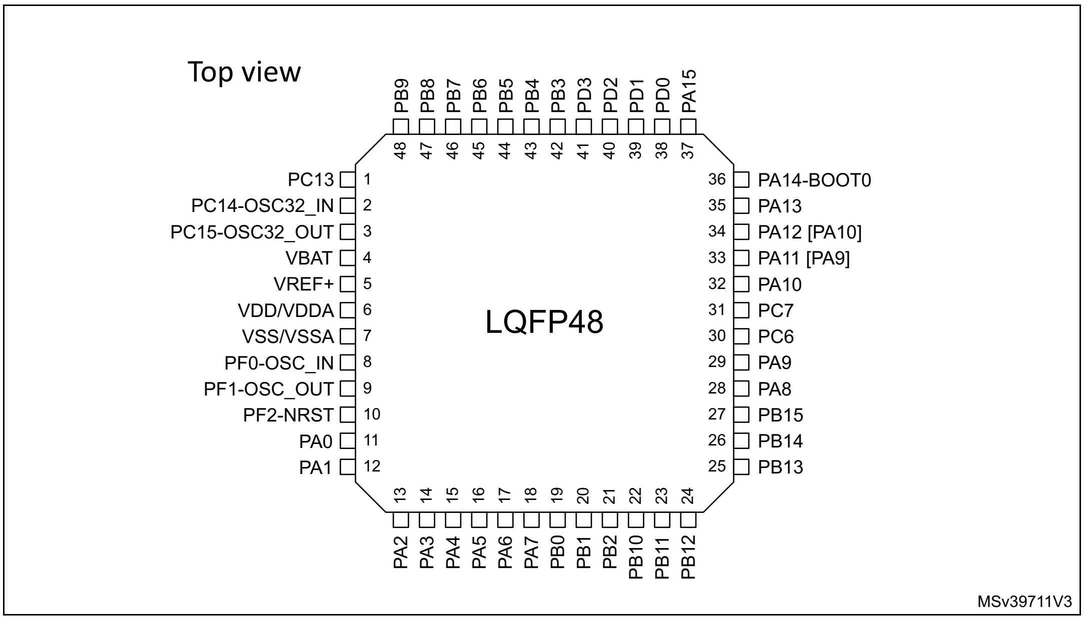


Figure 6. STM32G071CxU UFQFPN48 pinout

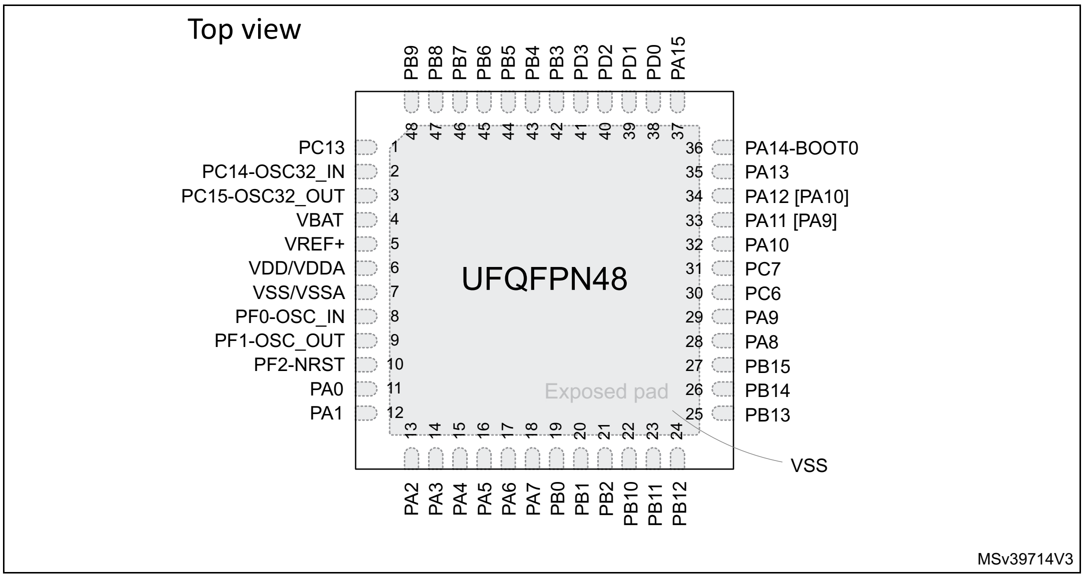


Figure 7. STM32G071KxT LQFP32 pinout

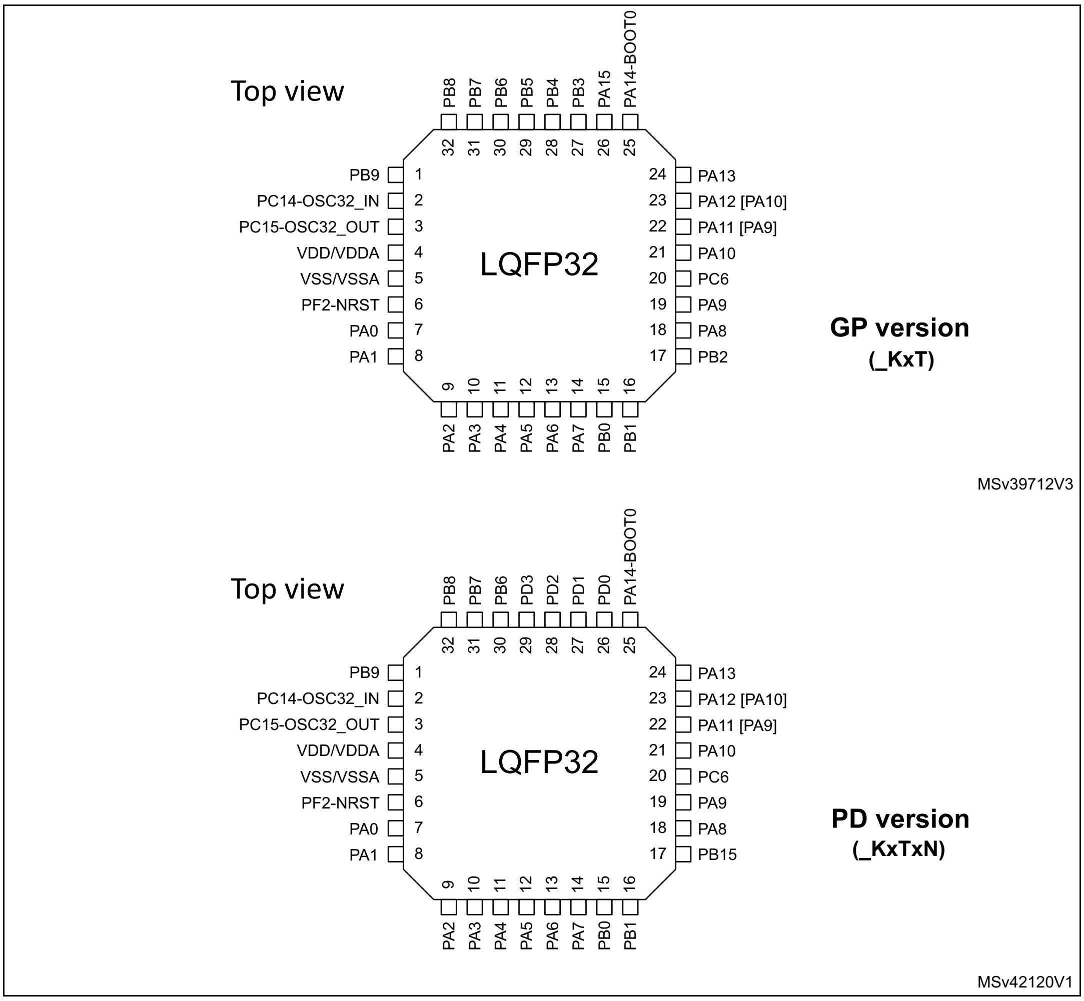


Figure 8. STM32G071KxU UFQFPN32 pinout

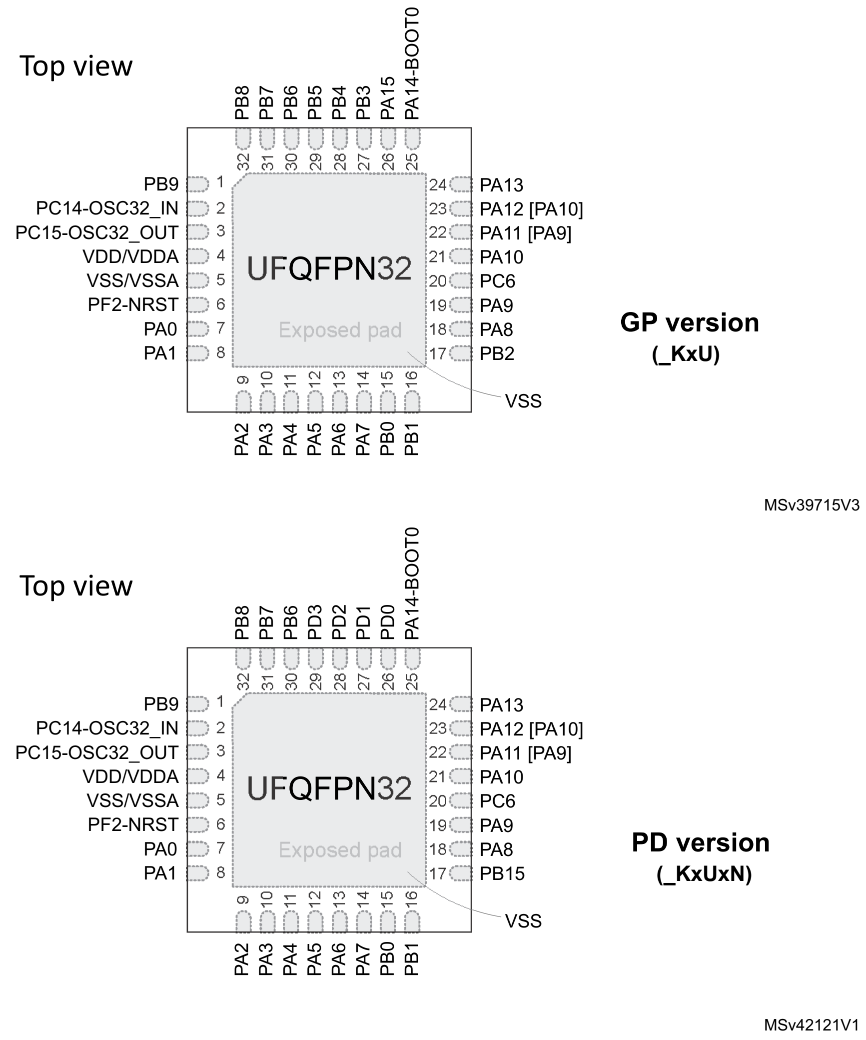


Figure 9. STM32G071GxU UFQFPN28 pinout

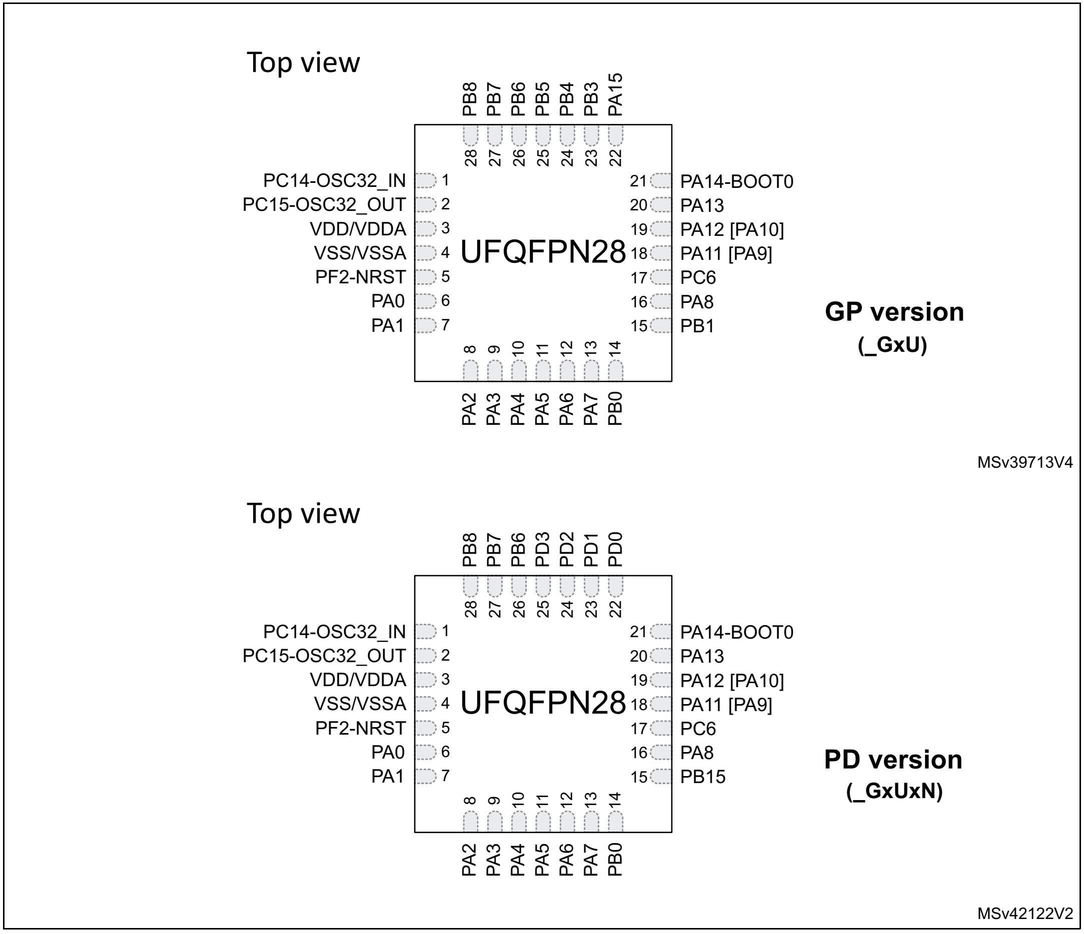
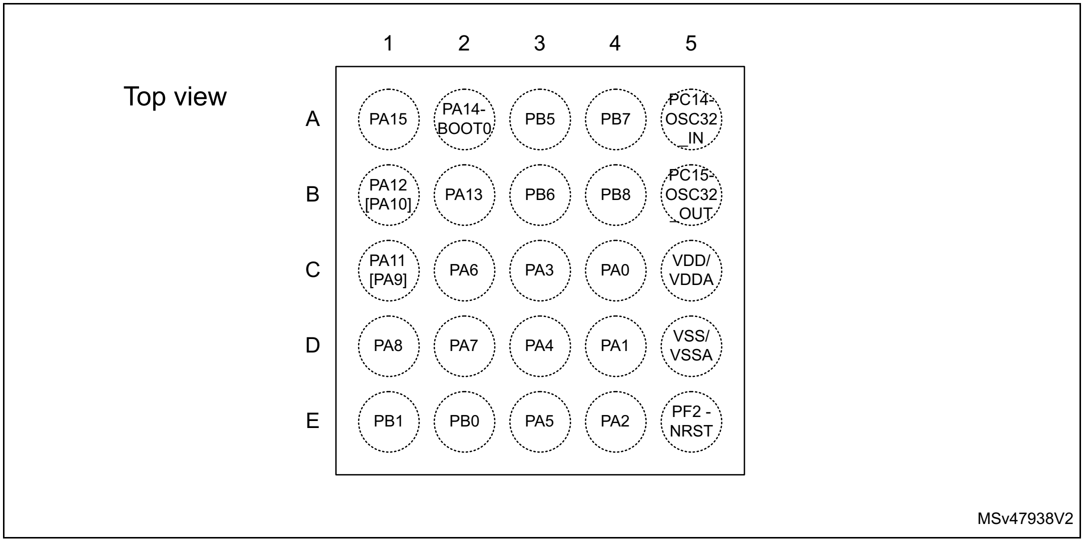


Figure 10. STM32G071Ex WLCSP25 pinout



	1	2	3	4	5
A	PA15	PA14-BOOT0	PB5	PB7	PC14-OSC32_IN
B	PA12 [PA10]	PA13	PB6	PB8	PC15-OSC32_OUT
C	PA11 [PA9]	PA6	PA3	PA0	VDD/VDDA
D	PA8	PA7	PA4	PA1	VSS/VSSA
E	PB1	PB0	PA5	PA2	PF2 - NRST

Table 11. Terms and symbols used in *Table 12*

Column		Symbol	Definition
Pin name		Terminal name corresponds to its by-default function at reset, unless otherwise specified in parenthesis under the pin name.	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Options for TT or FT I/Os	
		_f	I/O, Fm+ capable
		_a	I/O, with analog switch function
		_c	I/O, USB Type-C PD capable
		_d	I/O, USB Type-C PD Dead Battery function
Note		Upon reset, all I/Os are set as analog inputs, unless otherwise specified.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. Pin assignment and description

Pin Number								Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
WLCSP25	UFQFPN28 - GP	UFQFPN28 - PD	LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - PD	LQFP48 / UFQFPN48	UFBGA64	LQFP64						
-	-	-	-	-	-	A1	1	PC11	I/O	FT	-	USART3_RX, USART4_RX, TIM1_CH4	-
-	-	-	-	-	-	B2	2	PC12	I/O	FT	-	LPTIM1_IN1, UCPD1_FRSTX, TIM14_CH1	-
-	-	-	-	-	1	C2	3	PC13	I/O	FT	(1)(2)	TIM1_BKIN	TAMP_IN1,RTC_TS, RTC_OUT1,WKUP2

Table 12. Pin assignment and description (continued)

Pin Number								Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
WLCSP25	UFQFPN28 - GP	UFQFPN28 - PD	LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - PD	LQFP48 / UFQFPN48	UFBGA64	LQFP64						
-	-	-	-	-	2	C1	4	PC14-OSC32_IN (PC14)	I/O	FT	(1)(2)	TIM1_BKIN2	OSC32_IN
A5	1	1	2	2	-	-	-	PC14-OSC32_IN (PC14)	I/O	FT	(1)(2)	TIM1_BKIN2	OSC32_IN,OSC_IN
B5	2	2	3	3	3	B1	5	PC15-OSC32_OUT (PC15)	I/O	FT	(1)(2)	OSC32_EN, OSC_EN, TIM15_BKIN	OSC32_OUT
-	-	-	-	-	4	D3	6	VBAT	S	-	-	-	-
-	-	-	-	-	5	D2	7	VREF+	S	-	-	-	VREF_OUT
C5	3	3	4	4	6	D1	8	VDD/VDDA	S	-	-	-	-
D5	4	4	5	5	7	E1	9	VSS/VSSA	S	-	-	-	-
-	-	-	-	-	8	F1	10	PF0-OSC_IN (PF0)	I/O	FT	-	TIM14_CH1	OSC_IN
-	-	-	-	-	9	G1	11	PF1-OSC_OUT (PF1)	I/O	FT	-	OSC_EN, TIM15_CH1N	OSC_OUT
E5	5	5	6	6	10	E2	12	PF2 - NRST	I/O	FT	-	MCO	NRST
-	-	-	-	-	-	E3	13	PC0	I/O	FT	-	LPTIM1_IN1, LPUART1_RX, LPTIM2_IN1	-
-	-	-	-	-	-	F2	14	PC1	I/O	FT	-	LPTIM1_OUT, LPUART1_TX, TIM15_CH1	-
-	-	-	-	-	-	G2	15	PC2	I/O	FT	-	LPTIM1_IN2, SPI2_MISO, TIM15_CH2	-
-	-	-	-	-	-	H1	16	PC3	I/O	FT	-	LPTIM1_ETR, SPI2_MOSI, LPTIM2_ETR	-
C4	6	6	7	7	11	H2	17	PA0	I/O	FT_a	-	SPI2_SCK, USART2_CTS, TIM2_CH1_ETR, USART4_TX, LPTIM1_OUT, UCPD2_FRSTX, COMP1_OUT	COMP1_INM, ADC_IN0, TAMP_IN2,WKUP1

Table 12. Pin assignment and description (continued)

Pin Number								Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
WLCSP25	UFQFPN28 - GP	UFQFPN28 - PD	LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - PD	LQFP48 / UFQFPN48	UFBGA64	LQFP64						
D4	7	7	8	8	12	H3	18	PA1	I/O	FT_a	-	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM2_CH2, USART4_RX, TIM15_CH1N, I2C1_SMBA, EVENTOUT	COMP1_INP, ADC_IN1
E4	8	8	9	9	13	G3	19	PA2	I/O	FT_a	-	SPI1_MOSI/I2S1_SD, USART2_TX, TIM2_CH3, UCPD1_FRSTX, TIM15_CH1, LPUART1_TX, COMP2_OUT	COMP2_INM, ADC_IN2, WKUP4,LSCO
C3	9	9	10	10	14	F3	20	PA3	I/O	FT_a	-	SPI2_MISO, USART2_RX, TIM2_CH4, UCPD2_FRSTX, TIM15_CH2, LPUART1_RX, EVENTOUT	COMP2_INP, ADC_IN3
-	-	-	-	-	15	H4	21	PA4	I/O	TT_a	-	SPI1_NSS/I2S1_WS, SPI2_MOSI, TIM14_CH1, LPTIM2_OUT, UCPD2_FRSTX, EVENTOUT	ADC_IN4, DAC_OUT1, RTC_OUT2
D3	10	10	11	11	-	-	-	PA4	I/O	TT_a	-	SPI1_NSS/I2S1_WS, SPI2_MOSI, TIM14_CH1, LPTIM2_OUT, UCPD2_FRSTX, EVENTOUT	ADC_IN4, DAC_OUT1, TAMP_IN1,RTC_TS, RTC_OUT1,WKUP2
E3	11	11	12	12	16	G4	22	PA5	I/O	TT_a	-	SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, USART3_TX, LPTIM2_ETR, UCPD1_FRSTX, EVENTOUT	ADC_IN5, DAC_OUT2
C2	12	12	13	13	17	F4	23	PA6	I/O	FT_a	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, USART3_CTS, TIM16_CH1, LPUART1_CTS, COMP1_OUT	ADC_IN6
D2	13	13	14	14	18	E4	24	PA7	I/O	FT_a	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1, UCPD1_FRSTX, COMP2_OUT	ADC_IN7
-	-	-	-	-	-	H5	25	PC4	I/O	FT_a	-	USART3_TX, USART1_TX, TIM2_CH1_ETR	COMP1_INM, ADC_IN17

Table 12. Pin assignment and description (continued)

Pin Number								Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
WLCSP25	UFQFPN28 - GP	UFQFPN28 - PD	LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - PD	LQFP48 / UFQFPN48	UFBGA64	LQFP64						
-	-	-	-	-	-	H6	26	PC5	I/O	FT_a	-	USART3_RX, USART1_RX, TIM2_CH2	COMP1_INP, ADC_IN18, WKUP5
E2	14	-	15	15	19	F5	27	PB0	I/O	FT_a	-	SPI1_NSS/I2S1_WS, TIM3_CH3, TIM1_CH2N, USART3_RX, LPTIM1_OUT, UCPD1_FRSTX, COMP1_OUT	ADC_IN8
-	-	14	-	-	-	-	-	PB0	I/O	FT_da	(3)	SPI1_NSS/I2S1_WS, TIM3_CH3, TIM1_CH2N, USART3_RX, LPTIM1_OUT, UCPD1_FRSTX, COMP1_OUT	UCPD1_DBCC2, ADC_IN8
E1	15	-	16	16	20	G5	28	PB1	I/O	FT_a	-	TIM14_CH1, TIM3_CH4, TIM1_CH3N, USART3_RTS_DE_CK, LPTIM2_IN1, LPUART1_RTS_DE, EVENTOUT	COMP1_INM, ADC_IN9
-	-	-	17	-	21	H7	29	PB2	I/O	FT_a	-	SPI2_MISO, USART3_TX, LPTIM1_OUT, EVENTOUT	COMP1_INP, ADC_IN10
-	-	-	-	-	22	G6	30	PB10	I/O	FT_fa	-	CEC, LPUART1_RX, TIM2_CH3, USART3_TX, SPI2_SCK, I2C2_SCL, COMP1_OUT	ADC_IN11
-	-	-	-	-	23	H8	31	PB11	I/O	FT_fa	-	SPI2_MOSI, LPUART1_TX, TIM2_CH4, USART3_RX, I2C2_SDA, COMP2_OUT	ADC_IN15
-	-	-	-	-	24	G7	32	PB12	I/O	FT_a	-	SPI2_NSS, LPUART1_RTS_DE, TIM1_BKIN, TIM15_BKIN, UCPD2_FRSTX, EVENTOUT	ADC_IN16
-	-	-	-	-	25	G8	33	PB13	I/O	FT_f	-	SPI2_SCK, LPUART1_CTS, TIM1_CH1N, USART3_CTS, TIM15_CH1N, I2C2_SCL, EVENTOUT	-

Table 12. Pin assignment and description (continued)

Pin Number								Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
WLCSP25	UFQFPN28 - GP	UFQFPN28 - PD	LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - PD	LQFP48 / UFQFPN48	UFBGA64	LQFP64						
-	-	-	-	-	26	F6	34	PB14	I/O	FT_f	-	SPI2_MISO, UCPD1_FRSTX, TIM1_CH2N, USART3_RTS_DE_CK, TIM15_CH1, I2C2_SDA, EVENTOUT	-
-	-	15	-	17	27	F7	35	PB15	I/O	FT_c	(3)	SPI2_MOSI, TIM1_CH3N, TIM15_CH1N, TIM15_CH2, EVENTOUT	UCPD1_CC2, RTC_REFIN,
D1	16	16	18	18	28	F8	36	PA8	I/O	FT_c	(3)	MCO, SPI2_NSS, TIM1_CH1, LPTIM2_OUT, EVENTOUT	UCPD1_CC1
-	-	-	19	19	29	E6	37	PA9	I/O	FT_fd	(3)	MCO, USART1_TX, TIM1_CH2, SPI2_MISO, TIM15_BKIN, I2C1_SCL, EVENTOUT	UCPD1_DBCC1
-	17	-	20	20	30	E7	38	PC6	I/O	FT	-	UCPD1_FRSTX, TIM3_CH1, TIM2_CH3	-
-	-	17	-	-	-	-	-	PC6	I/O	FT_d	(3)	UCPD1_FRSTX, TIM3_CH1, TIM2_CH3	UCPD1_DBCC1
-	-	-	-	-	31	E5	39	PC7	I/O	FT	-	UCPD2_FRSTX, TIM3_CH2, TIM2_CH4	-
-	-	-	-	-	-	E8	40	PD8	I/O	FT	-	USART3_TX, SPI1_SCK/I2S1_CK, LPTIM1_OUT	-
-	-	-	-	-	-	D8	41	PD9	I/O	FT	-	USART3_RX, SPI1_NSS/I2S1_WS, TIM1_BKIN2	-
-	-	-	21	21	32	D6	42	PA10	I/O	FT_fd	(3)	SPI2_MOSI, USART1_RX, TIM1_CH3, TIM17_BKIN, I2C1_SDA, EVENTOUT	UCPD1_DBCC2
C1	18	18	22	22	33	C8	43	PA11 [PA9](4)	I/O	FT_f	-	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BKIN2, I2C2_SCL, COMP1_OUT	-
B1	19	19	23	23	34	B8	44	PA12 [PA10](4)	I/O	FT_f	-	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN, I2C2_SDA, COMP2_OUT	-

Table 12. Pin assignment and description (continued)

Pin Number								Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
WLCSP25	UFQFPN28 - GP	UFQFPN28 - PD	LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - PD	LQFP48 / UFQFPN48	UFBGA64	LQFP64						
B2	20	20	24	24	35	D7	45	PA13	I/O	FT	(5)	SWDIO, IR_OUT, EVENTOUT	-
A2	21	21	25	25	36	C7	46	PA14-BOOT0	I/O	FT	(5)	SWCLK, USART2_TX, EVENTOUT	BOOT0
A1	22	-	26	-	37	C6	47	PA15	I/O	FT	-	SPI1_NSS/I2S1_WS, USART2_RX, TIM2_CH1_ETR, USART4_RTS_DE_CK, USART3_RTS_DE_CK, EVENTOUT	-
-	-	-	-	-	-	A8	48	PC8	I/O	FT	-	UCPD2_FRSTX, TIM3_CH3, TIM1_CH1	-
-	-	-	-	-	-	B7	49	PC9	I/O	FT	-	I2S_CKIN, TIM3_CH4, TIM1_CH2	-
-	-	22	-	26	38	A7	50	PD0	I/O	FT_c	(3)	EVENTOUT, SPI2_NSS, TIM16_CH1	UCPD2_CC1
-	-	23	-	27	39	B6	51	PD1	I/O	FT_d	(3)	EVENTOUT, SPI2_SCK, TIM17_CH1	UCPD2_DBCC1
-	-	24	-	28	40	A6	52	PD2	I/O	FT_c	(3)	USART3_RTS_DE_CK, TIM3_ETR, TIM1_CH1N	UCPD2_CC2
-	-	25	-	29	41	D5	53	PD3	I/O	FT_d	(3)	USART2_CTS, SPI2_MISO, TIM1_CH2N	UCPD2_DBCC2
-	-	-	-	-	-	C5	54	PD4	I/O	FT	-	USART2_RTS_DE_CK, SPI2_MOSI, TIM1_CH3N	-
-	-	-	-	-	-	B5	55	PD5	I/O	FT	-	USART2_TX, SPI1_MISO/I2S1_MCK, TIM1_BKIN	-
-	-	-	-	-	-	A5	56	PD6	I/O	FT	-	USART2_RX, SPI1_MOSI/I2S1_SD, LPTIM2_OUT	-
-	23	-	27	-	42	B4	57	PB3	I/O	FT_a	-	SPI1_SCK/I2S1_CK, TIM1_CH2, TIM2_CH2, USART1_RTS_DE_CK, EVENTOUT	COMP2_INM
-	24	-	28	-	43	C4	58	PB4	I/O	FT_a	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, USART1_CTS, TIM17_BKIN, EVENTOUT	COMP2_INP

Table 12. Pin assignment and description (continued)

Pin Number								Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
WLCSP25	UFQFPN28 - GP	UFQFPN28 - PD	LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - PD	LQFP48 / UFQFPN48	UFBGA64	LQFP64						
A3	25	-	29	-	44	D4	59	PB5	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM16_BKIN, LPTIM1_IN1, I2C1_SMBA, COMP2_OUT	WKUP6
B3	26	26	30	30	45	A4	60	PB6	I/O	FT_fa	-	USART1_TX, TIM1_CH3, TIM16_CH1N, SPI2_MISO, LPTIM1_ETR, I2C1_SCL, EVENTOUT	COMP2_INP
A4	27	27	31	31	46	A3	61	PB7	I/O	FT_fa	-	USART1_RX, SPI2_MOSI, TIM17_CH1N, USART4_CTS, LPTIM1_IN2, I2C1_SDA, EVENTOUT	COMP2_INM, PVD_IN
B4	28	28	32	32	47	B3	62	PB8	I/O	FT_f	-	CEC, SPI2_SCK, TIM16_CH1, USART3_TX, TIM15_BKIN, I2C1_SCL, EVENTOUT	-
-	-	-	1	1	48	C3	63	PB9	I/O	FT_f	-	IR_OUT, UCPD2_FRSTX, TIM17_CH1, USART3_RX, SPI2_NSS, I2C1_SDA, EVENTOUT	-
-	-	-	-	-	-	A2	64	PC10	I/O	FT	-	USART3_TX, USART4_TX, TIM1_CH3	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After an RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers. The RTC registers are not reset upon system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the RM0444 reference manual.
3. Upon reset, a pull-down resistor might be present on PB15, PA8, PD0, or PD2, depending on the voltage level on PB0, PA9, PC6, PA10, PD1, and PD3. In order to disable this resistor, strobe the UCPDx_STROBE bit of the SYSCFG_CFGR1 register during start-up sequence.
4. Pins PA9/PA10 can be remapped in place of pins PA11/PA12 (default mapping), using SYSCFG_CFGR1 register.
5. Upon reset, these pins are configured as SW debug alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.

Table 13. Port A alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI2_SCK	USART2_CTS	TIM2_CH1_ETR	-	USART4_TX	LPTIM1_OUT	UCPD2_FRSTX	COMP1_OUT
PA1	SPI1_SCK/I2S1_CK	USART2_RTS_DE_CK	TIM2_CH2	-	USART4_RX	TIM15_CH1N	I2C1_SMBA	EVENTOUT
PA2	SPI1_MOSI/I2S1_SD	USART2_TX	TIM2_CH3	-	UCPD1_FRSTX	TIM15_CH1	LPUART1_TX	COMP2_OUT
PA3	SPI2_MISO	USART2_RX	TIM2_CH4	-	UCPD2_FRSTX	TIM15_CH2	LPUART1_RX	EVENTOUT
PA4	SPI1_NSS/I2S1_WS	SPI2_MOSI	-	-	TIM14_CH1	LPTIM2_OUT	UCPD2_FRSTX	EVENTOUT
PA5	SPI1_SCK/I2S1_CK	CEC	TIM2_CH1_ETR	-	USART3_TX	LPTIM2_ETR	UCPD1_FRSTX	EVENTOUT
PA6	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	USART3_CTS	TIM16_CH1	LPUART1_CTS	COMP1_OUT
PA7	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	UCPD1_FRSTX	COMP2_OUT
PA8	MCO	SPI2_NSS	TIM1_CH1	-	-	LPTIM2_OUT	-	EVENTOUT
PA9	MCO	USART1_TX	TIM1_CH2	-	SPI2_MISO	TIM15_BKIN	I2C1_SCL	EVENTOUT
PA10	SPI2_MOSI	USART1_RX	TIM1_CH3	-	-	TIM17_BKIN	I2C1_SDA	EVENTOUT
PA11	SPI1_MISO/I2S1_MCK	USART1_CTS	TIM1_CH4	-	-	TIM1_BKIN2	I2C2_SCL	COMP1_OUT
PA12	SPI1_MOSI/I2S1_SD	USART1_RTS_DE_CK	TIM1_ETR	-	-	I2S_CKIN	I2C2_SDA	COMP2_OUT
PA13	SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT
PA14	SWCLK	USART2_TX	-	-	-	-	-	EVENTOUT
PA15	SPI1_NSS/I2S1_WS	USART2_RX	TIM2_CH1_ETR	-	USART4_RTS_DE_CK	USART3_RTS_DE_CK	-	EVENTOUT

Table 14. Port B alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI1_NSS/I2S1_WS	TIM3_CH3	TIM1_CH2N	-	USART3_RX	LPTIM1_OUT	UCPD1_FRSTX	COMP1_OUT
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	USART3_RTS_DE_CK	LPTIM2_IN1	LPUART1_RTS_DE	EVENTOUT
PB2	-	SPI2_MISO	-	-	USART3_TX	LPTIM1_OUT	-	EVENTOUT
PB3	SPI1_SCK/I2S1_CK	TIM1_CH2	TIM2_CH2	-	USART1_RTS_DE_CK	-	-	EVENTOUT
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	-	USART1_CTS	TIM17_BKIN	-	EVENTOUT
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN	-	-	LPTIM1_IN1	I2C1_SMBA	COMP2_OUT
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	-	SPI2_MISO	LPTIM1_ETR	I2C1_SCL	EVENTOUT
PB7	USART1_RX	SPI2_MOSI	TIM17_CH1N	-	USART4_CTS	LPTIM1_IN2	I2C1_SDA	EVENTOUT
PB8	CEC	SPI2_SCK	TIM16_CH1	-	USART3_TX	TIM15_BKIN	I2C1_SCL	EVENTOUT
PB9	IR_OUT	UCPD2_FRSTX	TIM17_CH1	-	USART3_RX	SPI2_NSS	I2C1_SDA	EVENTOUT
PB10	CEC	LPUART1_RX	TIM2_CH3	-	USART3_TX	SPI2_SCK	I2C2_SCL	COMP1_OUT
PB11	SPI2_MOSI	LPUART1_TX	TIM2_CH4	-	USART3_RX	-	I2C2_SDA	COMP2_OUT
PB12	SPI2_NSS	LPUART1_RTS_DE	TIM1_BKIN	-	-	TIM15_BKIN	UCPD2_FRSTX	EVENTOUT
PB13	SPI2_SCK	LPUART1_CTS	TIM1_CH1N	-	USART3_CTS	TIM15_CH1N	I2C2_SCL	EVENTOUT
PB14	SPI2_MISO	UCPD1_FRSTX	TIM1_CH2N	-	USART3_RTS_DE_CK	TIM15_CH1	I2C2_SDA	EVENTOUT
PB15	SPI2_MOSI	-	TIM1_CH3N	-	TIM15_CH1N	TIM15_CH2	-	EVENTOUT

Table 15. Port C alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	LPTIM1_IN1	LPUART1_RX	LPTIM2_IN1	-	-	-	-	-
PC1	LPTIM1_OUT	LPUART1_TX	TIM15_CH1	-	-	-	-	-
PC2	LPTIM1_IN2	SPI2_MISO	TIM15_CH2	-	-	-	-	-
PC3	LPTIM1_ETR	SPI2_MOSI	LPTIM2_ETR	-	-	-	-	-
PC4	USART3_TX	USART1_TX	TIM2_CH1_ETR	-	-	-	-	-
PC5	USART3_RX	USART1_RX	TIM2_CH2	-	-	-	-	-
PC6	UCPD1_FRSTX	TIM3_CH1	TIM2_CH3	-	-	-	-	-
PC7	UCPD2_FRSTX	TIM3_CH2	TIM2_CH4	-	-	-	-	-
PC8	UCPD2_FRSTX	TIM3_CH3	TIM1_CH1	-	-	-	-	-
PC9	I2S_CKIN	TIM3_CH4	TIM1_CH2	-	-	-	-	-
PC10	USART3_TX	USART4_TX	TIM1_CH3	-	-	-	-	-
PC11	USART3_RX	USART4_RX	TIM1_CH4	-	-	-	-	-
PC12	LPTIM1_IN1	UCPD1_FRSTX	TIM14_CH1	-	-	-	-	-
PC13	-	-	TIM1_BKIN	-	-	-	-	-
PC14	-	-	TIM1_BKIN2	-	-	-	-	-
PC15	OSC32_EN	OSC_EN	TIM15_BKIN	-	-	-	-	-

Table 16. Port D alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	EVENTOUT	SPI2_NSS	TIM16_CH1	-	-	-	-	-
PD1	EVENTOUT	SPI2_SCK	TIM17_CH1	-	-	-	-	-
PD2	USART3_RTS_DE_CK	TIM3_ETR	TIM1_CH1N	-	-	-	-	-
PD3	USART2_CTS	SPI2_MISO	TIM1_CH2N	-	-	-	-	-
PD4	USART2_RTS_DE_CK	SPI2_MOSI	TIM1_CH3N	-	-	-	-	-
PD5	USART2_TX	SPI1_MISO/I2S1_MCK	TIM1_BKIN	-	-	-	-	-
PD6	USART2_RX	SPI1_MOSI/I2S1_SD	LPTIM2_OUT	-	-	-	-	-
PD8	USART3_TX	SPI1_SCK/I2S1_CK	LPTIM1_OUT	-	-	-	-	-
PD9	USART3_RX	SPI1_NSS/I2S1_WS	TIM1_BKIN2	-	-	-	-	-

Table 17. Port F alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	TIM14_CH1	-	-	-	-	-
PF1	OSC_EN	-	TIM15_CH1N	-	-	-	-	-
PF2	MCO	-	-	-	-	-	-	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

Parameter values defined at temperatures or in temperature ranges out of the ordering information scope are to be ignored.

Packages used for characterizing certain electrical parameters may differ from the commercial packages as per the ordering information.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A(max) (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

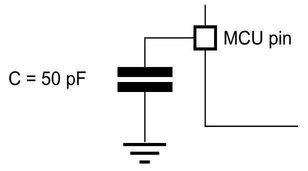
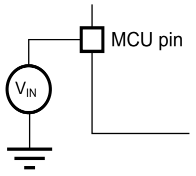
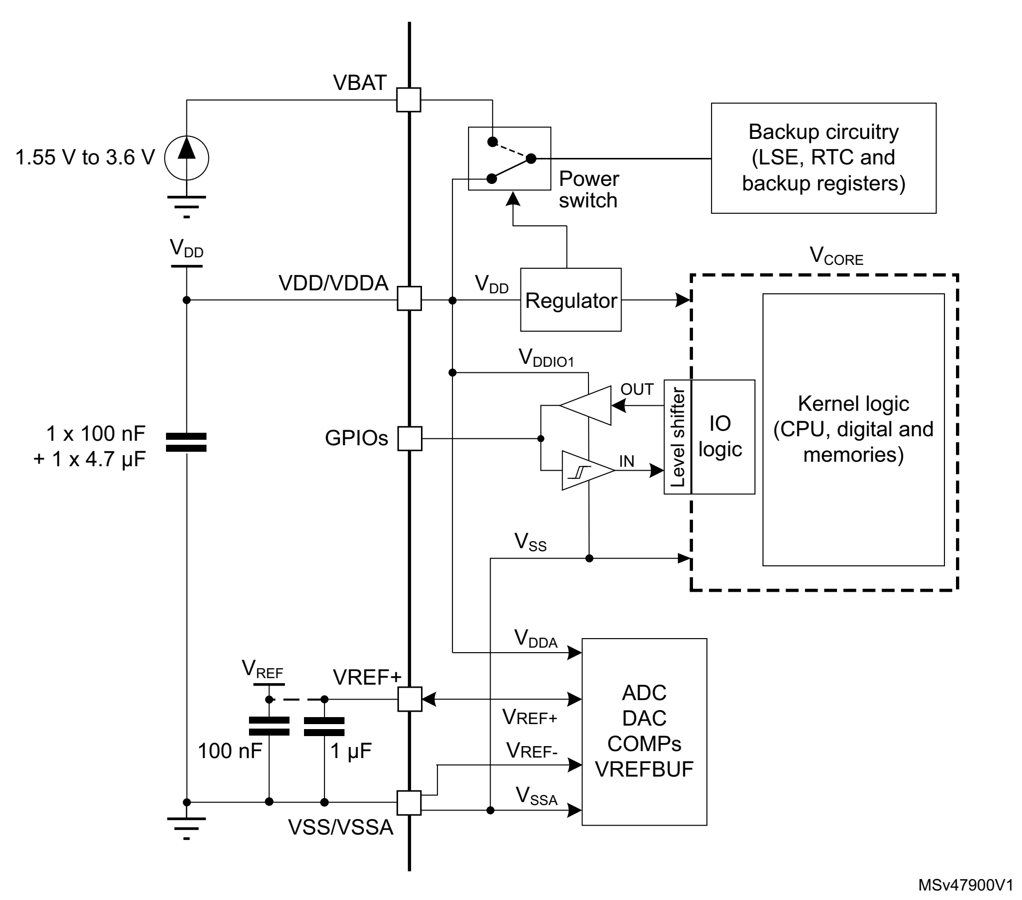


Figure 12. Pin input voltage



5.1.6 Power supply scheme

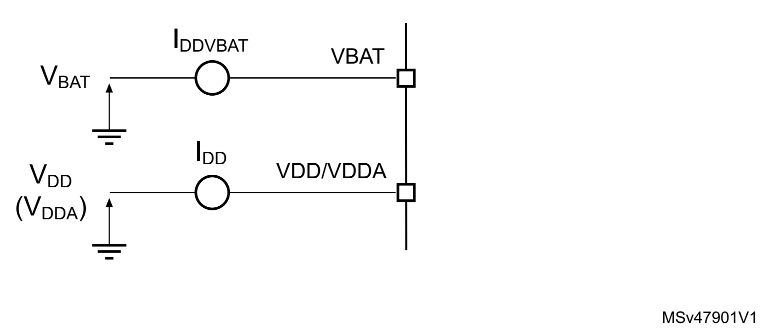
Figure 13. Power supply scheme



Caution: Power supply pin pair (VDD/VDDA and VSS/VSSA) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

5.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18*, *Table 19* and *Table 20* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

All voltages are defined with respect to V_{SS}.

Table 18. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}	External supply voltage	- 0.3	4.0	V
V_{BAT}	External supply voltage on VBAT pin	- 0.3	4.0	
V_{REF+}	External voltage on VREF+ pin	- 0.3	Min(V_{DD} + 0.4, 4.0)	
V_{IN}(1)	Input voltage on FT_xx pins except FT_c	- 0.3	V_{DD} + 4.0(2)	
	Input voltage on FT_c pins	- 0.3	5.5	
	Input voltage on any other pin	- 0.3	4.0	

1. Refer to *Table 19* for the maximum allowed injected current values.
2. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.

Table 19. Current characteristics

Symbol	Ratings	Max	Unit
$I_{VDD/VDDA}$	Current into VDD/VDDA power pin (source)(1)	100	mA
$I_{VSS/VSSA}$	Current out of VSS/VSSA ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	15	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	15	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins	80	
	Total output current sourced by sum of all I/Os and control pins	80	
$I_{INJ(PIN)}$(2)	Injected current on a FT_xx pin	-5 / NA(3)	
	Injected current on a TT_a pin(4)	-5 / 0	
$\Sigma\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(5)	25	

1. All main power (VDD/VDDA, VBAT) and ground (VSS/VSSA) pins must always be connected to the external power supplies, in the permitted range.
2. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 18: Voltage characteristics* for the maximum allowed input voltage values.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. On these I/Os, any current injection disturbs the analog performances of the device.
5. When several inputs are submitted to a current injection, the maximum $\Sigma|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz
f_{PCLK}	Internal APB clock frequency	-	0	64	
V_{DD}	Standard operating voltage	-	1.7(1)	3.6	V
V_{DDA}	Analog supply voltage	For ADC and COMP operation	1.62	3.6	V
		For DAC operation	1.8	3.6	
		For VREFBUF operation	2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.55	3.6	V
V_{IN}	I/O input voltage	All except TT_xx and FT_c	-0.3	Min(V_{DD} + 3.6, 5.5)(2)	V
		TT_xx	-0.3	V_{DD} + 0.3	
		FT_c	-0.3	5.0(2)	
T_A	Ambient temperature(3)	Suffix 6(4)	-40	85	°C
		Suffix 7(4)	-40	105	
		Suffix 3(4)	-40	125	
T_J	Junction temperature	Suffix 6(4)	-40	105	°C
		Suffix 7(4)	-40	125	
		Suffix 3(4)	-40	130	

1. When RESET is released functionality is guaranteed down to V_{PDR} min.
2. For operation with voltage higher than V_{DD} +0.3 V, the internal pull-up and pull-down resistors must be disabled.
3. The T_A(max) applies to P_D(max). At $P_D < P_D$(max) the ambient temperature is allowed to go higher than T_A(max) provided that the junction temperature T_J does not exceed T_J(max). Refer to *Section 6.9: Thermal characteristics*.
4. Temperature range digit in the order code. See *Section 7: Ordering information*.

5.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} slew rate	V_{DD} rising	-	∞	µs/V
		V_{DD} falling; ULPEN = 0	10	∞	
		V_{DD} falling; ULPEN = 1	100	∞	ms/V

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	POR temporization when V_{DD} crosses V_{POR}	V_{DD} rising	-	250	400	µs
V_{POR}(2)	Power-on reset threshold	-	1.62	1.66	1.70	V
V_{PDR}(2)	Power-down reset threshold	-	1.60	1.64	1.69	V
V_{BOR1}	Brownout reset threshold 1	V_{DD} rising	2.05	2.10	2.18	V
		V_{DD} falling	1.95	2.00	2.08	
V_{BOR2}	Brownout reset threshold 2	V_{DD} rising	2.20	2.31	2.38	V
		V_{DD} falling	2.10	2.21	2.28	
V_{BOR3}	Brownout reset threshold 3	V_{DD} rising	2.50	2.62	2.68	V
		V_{DD} falling	2.40	2.52	2.58	
V_{BOR4}	Brownout reset threshold 4	V_{DD} rising	2.80	2.91	3.00	V
		V_{DD} falling	2.70	2.81	2.90	
V_{PVD0}	Programmable voltage detector threshold 0	V_{DD} rising	2.05	2.15	2.22	V
		V_{DD} falling	1.95	2.05	2.12	
V_{PVD1}	PVD threshold 1	V_{DD} rising	2.20	2.30	2.37	V
		V_{DD} falling	2.10	2.20	2.27	
V_{PVD2}	PVD threshold 2	V_{DD} rising	2.35	2.46	2.54	V
		V_{DD} falling	2.25	2.36	2.44	
V_{PVD3}	PVD threshold 3	V_{DD} rising	2.50	2.62	2.70	V
		V_{DD} falling	2.40	2.52	2.60	
V_{PVD4}	PVD threshold 4	V_{DD} rising	2.65	2.74	2.87	V
		V_{DD} falling	2.55	2.64	2.77	

Table 23. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
V_{PVD5}	PVD threshold 5	V_{DD} rising	2.80	2.91	3.03	V
		V_{DD} falling	2.70	2.81	2.93	
V_{PVD6}	PVD threshold 6	V_{DD} rising	2.90	3.01	3.14	V
		V_{DD} falling	2.80	2.91	3.04	
$V_{hyst\_POR\_PDR}$	Hysteresis of V_{POR} and V_{PDR}	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis of V_{BORx} and V_{PVDx}	-	-	100	-	mV
$I_{DD(BOR\_PVD)}$(2)	BOR and PVD consumption	-	-	1.1	1.6	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.

5.3.4 Embedded voltage reference

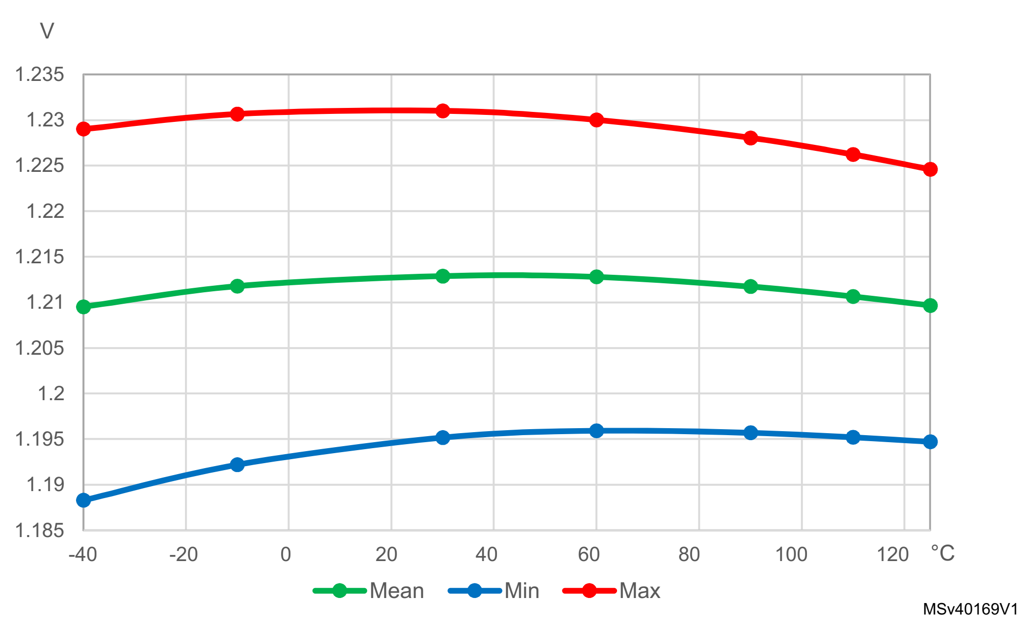
The parameters given in *Table 24* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 24. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40°C < T_J < 130°C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD(VREFINTBUF)}$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
$T_{Coeff\_vrefint}$	Temperature coefficient	-	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25 °C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 15. V_{REFINT} vs. temperature



5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0444 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- For Flash memory and shared peripherals $f_{PCLK} = f_{HCLK} = f_{HCLKS}$

Unless otherwise stated, values given in *Table 25* through *Table 33* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 25. Current consumption in Run and Low-power run modes at different die temperatures

Symbol	Parameter	Conditions			Typ			Max(1)			Unit
		General	f_{HCLK}	Fetch from(2)	25° C	85° C	125° C	25° C	85° C	130° C	
$I_{DD(Run)}$	Supply current in Run mode	Range 1; PLL enabled; $f_{HCLK} = f_{HSE\_bypass}$ (≤16 MHz), $f_{HCLK} = f_{PLLRCLK}$ (>16 MHz); (3)	64 MHz	Flash memory	6.3	6.4	6.8	6.7	7.0	7.7	mA
			56 MHz		5.5	5.7	5.9	5.9	6.3	6.8	
			48 MHz		5.0	5.1	5.4	5.2	5.7	6.3	
			32 MHz		3.5	3.6	3.8	4.0	4.3	4.7	
			24 MHz		2.8	2.9	3.1	3.1	3.6	4.0	
			16 MHz		1.8	1.9	2.1	2.1	2.5	3.0	
			64 MHz	SRAM	6.0	6.2	6.4	6.3	6.6	7.0	
			56 MHz		5.3	5.5	5.7	5.6	5.8	6.2	
			48 MHz		4.7	4.8	5.0	5.0	5.2	5.6	
			32 MHz		3.3	3.4	3.5	3.5	3.8	4.1	
			24 MHz		2.6	2.7	2.9	2.8	3.1	3.4	
			16 MHz		1.7	1.7	1.9	1.9	2.1	2.7	
		Range 2; PLL enabled; $f_{HCLK} = f_{HSE\_bypass}$ (≤16 MHz), $f_{HCLK} = f_{PLLRCLK}$ (>16 MHz); (3)	16 MHz	Flash memory	1.4	1.5	1.7	1.7	2.0	2.6	
			8 MHz		0.8	0.9	1.0	1.2	1.3	1.8	
			2 MHz		0.3	0.3	0.5	0.5	0.8	1.4	
			16 MHz	SRAM	1.4	1.4	1.6	1.6	1.8	2.2	
			8 MHz		0.7	0.8	1.0	1.1	1.2	1.6	
			4 MHz		0.4	0.5	0.6	0.7	0.9	1.5	
			2 MHz		0.3	0.3	0.5	0.5	0.8	1.2	
$I_{DD(LPRun)}$	Supply current in Low-power run mode	PLL disabled; $f_{HCLK} = f_{HSE}$ bypass (> 32 kHz), $f_{HCLK} = f_{LSE}$ bypass (= 32 kHz); (3)	2 MHz	Flash memory	220	255	420	530	795	1255	µA
			1 MHz		105	155	320	505	770	1200	
			500 kHz		67	105	265	465	700	1110	
			125 kHz		26	66	230	450	520	1045	
			32 kHz		17	56	220	375	475	1035	
			2 MHz	SRAM	199	231	380	485	700	1220	
			1 MHz		95	140	290	430	660	1140	
			500 kHz		61	95	240	365	625	1100	
			125 kHz		24	59	225	335	440	970	
			32 kHz		15	55	220	325	355	940	

1. Based on characterization results, not tested in production.
2. Prefetch and cache enabled when fetching from Flash. Code compiled with high optimization for space in SRAM.
3. V_{DD} = 3.0 V for values in Typ columns and 3.6 V for values in Max columns, all peripherals disabled, cache enabled, prefetch disabled for code and data fetch from Flash and enabled from SRAM

Table 26. Typical current consumption in Run and Low-power run modes, depending on code executed

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		General	Code	Fetch from(1)	25 °C		25 °C	
$I_{DD(Run)}$	Supply current in Run mode	Range 1; $f_{HCLK} = f_{PLLRCLK}$ = 64 MHz; (2)	Reduced code(3)	Flash memory	6.4	mA	100	uA/MHz
			Coremark		6.2		97	
			Dhrystone 2.1		5.9		92	
			Fibonacci		4.6		71	
			While(1) loop		4.6		71	
			Reduced code(3)	SRAM	6.2		96	
			Coremark		6.2		97	
			Dhrystone 2.1		6.0		93	
			Fibonacci		6.2		96	
			While(1) loop		4.8		75	
		Range 2; $f_{HCLK} = f_{HSI16}$ = 16 MHz, PLL disabled, (2)	Reduced code(3)	Flash memory	1.5		94	
			Coremark		1.5		94	
			Dhrystone 2.1		1.5		91	
			Fibonacci		1.1		69	
			While(1) loop		1.1		69	
			Reduced code(3)	SRAM	1.5		91	
			Coremark		1.4		88	
			Dhrystone 2.1		1.4		84	
			Fibonacci		1.5		91	
			While(1) loop		1.1		69	
$I_{DD(LPRun)}$	Supply current in Low-power run mode	$f_{HCLK} = f_{HSI16}/8$ = 2 MHz; PLL disabled, (2)	Reduced code(3)	Flash memory	380	uA	190	uA/MHz
			Coremark		395		198	
			Dhrystone 2.1		405		203	
			Fibonacci		385		193	
			While(1) loop		400		200	
			Reduced code(3)	SRAM	250		125	
			Coremark		245		123	
			Dhrystone 2.1		240		120	
			Fibonacci		250		125	
			While(1) loop		230		115	

1. Prefetch and cache enabled when fetching from Flash. Code compiled with high optimization for space in SRAM.
2. V_{DD} = 3.3 V, all peripherals disabled, cache enabled, prefetch disabled for execution in Flash and enabled in SRAM
3. Reduced code used for characterization results provided in *Table 25*.

Table 27. Current consumption in Sleep and Low-power sleep modes

Symbol	Parameter	Conditions			Typ			Max[1]			Unit
		General	Voltage scaling	f_{HCLK}	25° C	85° C	125° C	25° C	85° C	130° C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	Flash memory enabled; $f_{HCLK} = f_{HSE}$ bypass (≤16 MHz; PLL disabled), $f_{HCLK} = f_{PLLRCLK}$ (>16 MHz; PLL enabled); All peripherals disabled	Range 1	64 MHz	1.8	1.9	2.1	1.8	2.1	2.9	mA
				56 MHz	1.6	1.7	1.9	1.7	1.9	2.8	
				48 MHz	1.4	1.5	1.7	1.6	1.7	2.7	
				32 MHz	1.0	1.1	1.3	1.2	1.3	2.3	
				24 MHz	0.8	0.9	1.1	1.0	1.1	1.9	
				16 MHz	0.5	0.6	0.8	0.6	0.7	1.7	
			Range 2	16 MHz	0.4	0.5	0.7	0.5	0.6	1.4	
				8 MHz	0.3	0.3	0.5	0.3	0.5	1.2	
				2 MHz	0.1	0.2	0.4	0.2	0.4	1.1	
$I_{DD(LPSleep)}$	Supply current in Low-power sleep mode	Flash memory disabled; PLL disabled; $f_{HCLK} = f_{HSE}$ bypass (> 32 kHz), $f_{HCLK} = f_{LSE}$ bypass (= 32 kHz); All peripherals disabled		2 MHz	60	99	265	150	360	1110	µA
				1 MHz	33	75	240	130	330	1010	
				500 kHz	25	64	230	125	250	870	
				125 kHz	16	55	220	110	235	715	
				32 kHz	14	53	215	110	225	645	

1. Based on characterization results, not tested in production.

Table 28. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		Typ			Max[1]			Unit
		HSI kernel	V_{DD}	25°C	85°C	125°C	25°C	85°C	130°C	
$I_{DD(Stop\ 0)}$	Supply current in Stop 0 mode	Enabled	1.8 V	275	305	430	330	425	750	µA
			2.4 V	280	310	435	330	450	850	
			3 V	280	315	435	350	490	950	
			3.6 V	285	315	440	375	500	1020	
		Disabled	1.8 V	95	140	270	120	180	490	
			2.4 V	100	145	275	125	220	610	
			3 V	100	145	280	125	240	720	
			3.6 V	105	150	285	130	250	840	

1. Based on characterization results, not tested in production.

Table 29. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			Typ			Max[1]			Unit
		Flash memory	RTC[2]	V_{DD}	25°C	85°C	125°C	25°C	85°C	130°C	
$I_{DD(Stop\ 1)}$	Supply current in Stop 1 mode	Not powered	Disabled	1.8 V	3.2	32	150	8	100	480	µA
				2.4 V	3.3	32	150	10	120	535	
				3 V	3.4	33	155	15	135	620	
				3.6 V	3.8	33	155	18	140	705	
			Enabled	1.8 V	3.4	32	150	9	100	480	
				2.4 V	3.7	32	155	11	120	540	
				3 V	4.0	33	155	16	140	630	
				3.6 V	4.4	34	160	20	145	720	
		Powered	Disabled	1.8 V	6.9	36	155	12	100	575	
				2.4 V	7.3	36	160	14	110	600	
				3 V	7.3	37	160	18	120	645	
				3.6 V	7.8	38	160	23	135	665	

1. Based on characterization results, not tested in production.
2. Clocked by LSI

Table 30. Current consumption in Standby mode

Symbol	Parameter	Conditions		Typ			Max[1]			Unit
		General	V_{DD}	25°C	85°C	125°C	25°C	85°C	130°C	
$I_{DD(Standby)}$	Supply current in Standby mode[2]	RTC disabled	1.8 V	0.07	1.7	6.7	0.7	9	34	µA
			2.4 V	0.13	2.1	8.1	0.8	12	38	
			3.0 V	0.20	2.5	10.0	0.9	14	46	
			3.6 V	0.34	3.0	12.0	1.0	16	55	
		RTC enabled, clocked by LSI;	1.8 V	0.35	2.0	7.0	0.8	10	35	
			2.4 V	0.49	2.4	8.4	1.0	12	40	
			3.0 V	0.66	2.9	10.5	1.3	15	47	
			3.6 V	0.90	3.5	12.5	2.2	18	56	
		IWDG enabled, clocked by LSI	1.8 V	0.26	1.9	6.8	0.8	10	34	
			2.4 V	0.37	2.3	8.3	1.0	12	39	
			3.0 V	0.49	2.7	10.3	1.4	15	45	
			3.6 V	0.69	3.3	12.3	2.1	18	52	
		ULPEN = 0	1.8 V	0.70	1.6	6.6	-	-	-	
			2.4 V	0.89	2.0	8.0	-	-	-	
			3.0 V	1.10	2.4	9.8	-	-	-	
			3.6 V	1.30	2.9	11.8	-	-	-	

Table 30. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		Typ			Max(1)			Unit
		General	V_{DD}	25°C	85°C	125°C	25°C	85°C	130°C	
$\Delta I_{DD(SRAM)}$	Extra supply current to retain SRAM content(3)	SRAM retention enabled	1.8 V	0.49	3.0	14.8	0.6	16	58	µA
			2.4 V	0.57	3.1	14.9	1.1	17	63	
			3.0 V	0.67	3.2	15.0	1.5	17	67	
			3.6 V	0.77	3.3	15.0	1.9	18	71	

1. Based on characterization results, not tested in production.
2. Without SRAM retention and with ULPEN bit set
3. To be added to $I_{DD(Standby)}$ as appropriate

Table 31. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		Typ			Max(1)			Unit
		RTC	V_{DD}	25 °C	85 °C	125 °C	25 °C	85 °C	130 °C	
$I_{DD(Shutdown)}$	Supply current in Shutdown mode	Disabled	1.8 V	17	515	4500	250	3000	32600	nA
			2.4 V	23	600	5150	450	3500	33600	
			3.0 V	33	730	6450	1075	4250	37400	
			3.6 V	53	940	7700	1250	5300	43600	
		Enabled, clocked by LSE bypass at 32.768 kHz	1.8 V	205	710	4700	900	4500	27300	
			2.4 V	300	890	5500	1550	5500	34800	
			3.0 V	420	1150	6800	2475	6000	40900	
			3.6 V	565	1450	8100	3250	7000	48500	

1. Based on characterization results, not tested in production.

Table 32. Current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ			Unit
		RTC	V_{DD}	25°C	85°C	125°C	
$I_{DD(VBAT)}$	Supply current in VBAT mode	Enabled, clocked by LSE bypass at 32.768 kHz	1.8 V	165	170	620	nA
			2.4 V	260	355	970	
			3.0 V	365	475	1200	
			3.6 V	505	655	2070	
		Enabled, clocked by LSE crystal at 32.768 kHz	1.8 V	290	390	960	
			2.4 V	370	480	1150	
			3.0 V	470	600	1650	
			3.6 V	600	815	2250	
		Disabled	1.8 V	1	80	660	
			2.4 V	2	90	750	
			3.0 V	2	105	1200	
			3.6 V	6	200	1700	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 51: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 33: Current consumption of peripherals*, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIO1} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
V_{DDIO1} is the I/O supply voltage
f_{SW} is the I/O switching frequency
C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$
C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 18: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 33. Current consumption of peripherals

Peripheral	Bus	Consumption in µA/MHz		
		Range 1	Range 2	Low-power run and sleep
IOPORT Bus	IOPORT	1.0	0.7	0.5
GPIOA	IOPORT	3.4	2.8	3.0
GPIOB	IOPORT	3.1	2.6	2.5
GPIOC	IOPORT	2.9	2.5	3.0
GPIOD	IOPORT	1.8	1.5	1.5
GPIOF	IOPORT	0.7	0.6	1.0
Bus matrix	AHB	3.2	2.2	2.8
All AHB Peripherals	AHB	15.0	12.5	14.0
DMA1/DMAMUX	AHB	4.7	3.8	4.5
CRC	AHB	0.5	0.4	0.5
FLASH	AHB	4.1	3.5	4.0
All APB peripherals	APB	46.5	47.5	48.0
AHB to APB bridge(1)	APB	0.2	0.2	0.1
PWR	APB	0.4	0.3	0.5
SYSCFG/VREFBUF/COMP	APB	0.4	0.4	0.3
WWDG	APB	0.4	0.3	0.5
TIM1	APB	7.3	6.1	6.5
TIM2	APB	4.7	3.8	5.0
TIM3	APB	3.6	3.0	2.5
TIM6	APB	0.7	0.6	0.5
TIM7	APB	0.7	0.7	1.0
TIM14	APB	1.5	1.2	1.5
TIM15	APB	4.0	3.3	3.0
TIM16	APB	2.3	2.0	2.0

Table 33. Current consumption of peripherals (continued)

Peripheral	Bus	Consumption in µA/MHz		
		Range 1	Range 2	Low-power run and sleep
TIM17	APB	0.7	0.7	0.5
LPTIM1	APB	3.2	2.7	3.0
LPTIM2	APB	3.1	2.5	3.0
I2C1	APB	3.8	3.1	3.5
I2C2	APB	0.7	0.6	1.0
SPI2	APB	1.5	1.2	1.0
USART1	APB	7.2	6.0	6.5
USART2	APB	7.2	6.0	6.0
USART3	APB	2.0	1.7	2.0
USART4	APB	2.0	1.7	2.0
LPUART1	APB	4.3	3.5	4.0
CEC	APB	0.4	0.3	0.5
UCPD1	APB	4.0	7.7	NA(2)
UCPD2	APB	4.0	7.7	NA(2)
ADC	APB	2.0	1.7	2.0
DAC	APB	2.2	1.8	2.0

1. The AHB to APB Bridge is automatically active when at least one peripheral is ON on the APB.
2. UCPDx are always clocked by HSI16.

5.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 34* are the latency between the event and the execution of the first user instruction.

Table 34. Low-power mode wakeup times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep to Run mode	-	11	11	CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode	Transiting to Low-power-run-mode execution in Flash memory not powered in Low-power sleep mode; HCLK = HSI16 / 8 = 2 MHz	11	14	

Table 34. Low-power mode wakeup times[1] (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSTOP0}$	Wakeup time from Stop 0	Transiting to Run-mode execution in Flash memory not powered in Stop 0 mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1 or Range 2	5.6	6	µs
		Transiting to Run-mode execution in SRAM or in Flash memory powered in Stop 0 mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1 or Range 2	2	2.4	
$t_{WUSTOP1}$	Wakeup time from Stop 1	Transiting to Run-mode execution in Flash memory not powered in Stop 1 mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1 or Range 2	9.0	11.2	µs
		Transiting to Run-mode execution in SRAM or in Flash memory powered in Stop 1 mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1 or Range 2	5	7.5	
		Transiting to Low-power-run-mode execution in Flash memory not powered in Stop 1 mode; HCLK = HSI16/8 = 2 MHz; Regulator in low-power mode (LPR = 1 in PWR_CR1)	22	25.3	
		Transiting to Low-power-run-mode execution in SRAM or in Flash memory powered in Stop 1 mode; HCLK = HSI16 / 8 = 2 MHz; Regulator in low-power mode (LPR = 1 in PWR_CR1)	18	23.5	
t_{WUSTBY}	Wakeup time from Standby mode	Transiting to Run mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1	14.5	30	µs
t_{WUSHDN}	Wakeup time from Shutdown mode	Transiting to Run mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1	258	340	µs
$t_{WULPRUN}$	Wakeup time from Low-power run mode[2]	Transiting to Run mode; HSISYS = HSI16/8 = 2 MHz	5	7	µs

1. Based on characterization results, not tested in production.
2. Time until REGLPF flag is cleared in PWR_SR2.

Table 35. Regulator mode transition times[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{VOST}	Transition times between regulator Range 1 and Range 2[2]	HSISYS = HSI16	20	40	µs

1. Based on characterization results, not tested in production.
2. Time until VOSF flag is cleared in PWR_SR2.

Table 36. Wakeup time using LPUART[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPUART}$	Wakeup time needed to calculate the maximum LPUART baud rate allowing to wakeup up from Stop mode when LPUART clock source is HSI16	Stop mode 0	-	1.7	µs
		Stop mode 1	-	8.5	

1. Guaranteed by design.

5.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

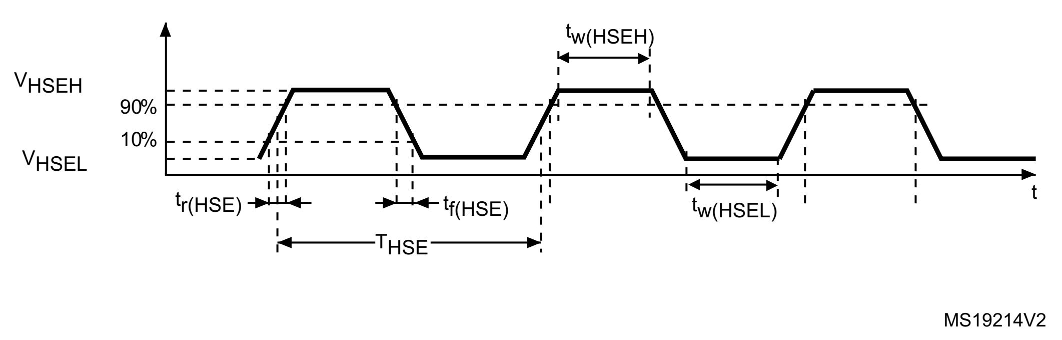
The external clock signal has to respect the I/O characteristics in *Section 5.3.14*. See *Figure 16* for recommended clock input waveform.

Table 37. High-speed external user clock characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIO1}	-	V_{DDIO1}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIO1}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 16. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

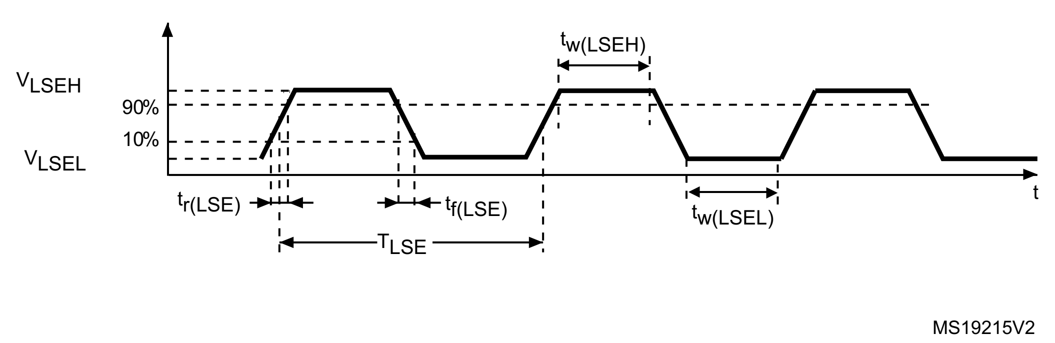
The external clock signal has to respect the I/O characteristics in *Section 5.3.14*. See *Figure 17* for recommended clock input waveform.

Table 38. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIO1}	-	V_{DDIO1}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIO1}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 17. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 39. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ

Table 39. HSE oscillator characteristics[1] (continued)

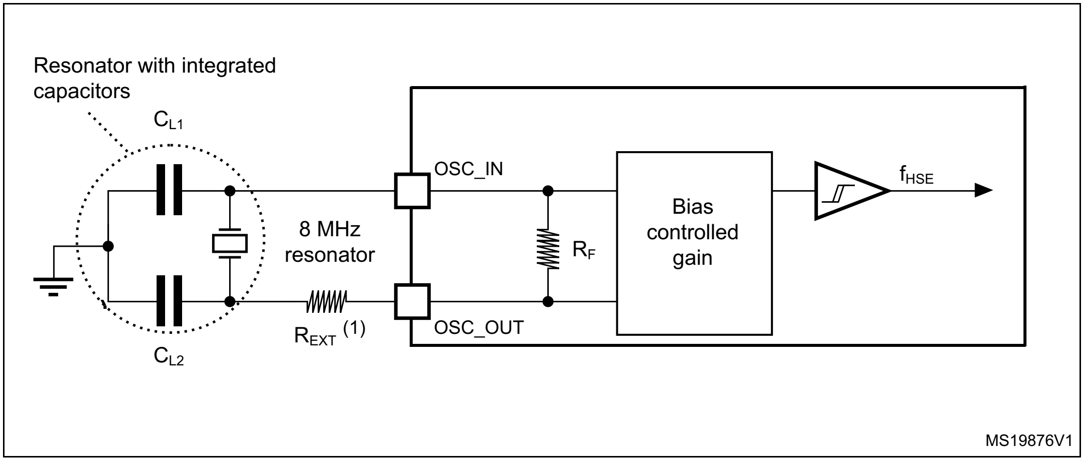
Symbol	Parameter	Conditions[2]	Min	Typ	Max	Unit
$I_{DD(HSE)}$	HSE current consumption	During startup[3]	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 18*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 18. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

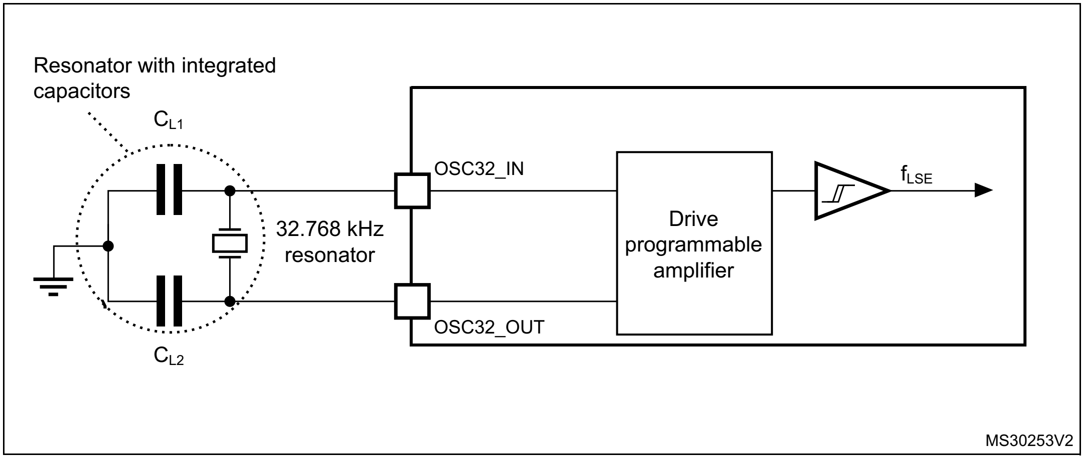
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.

3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 19. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

5.3.8 Internal clock source characteristics

The parameters given in *Table 41* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 41. HSI16 oscillator characteristics[1]

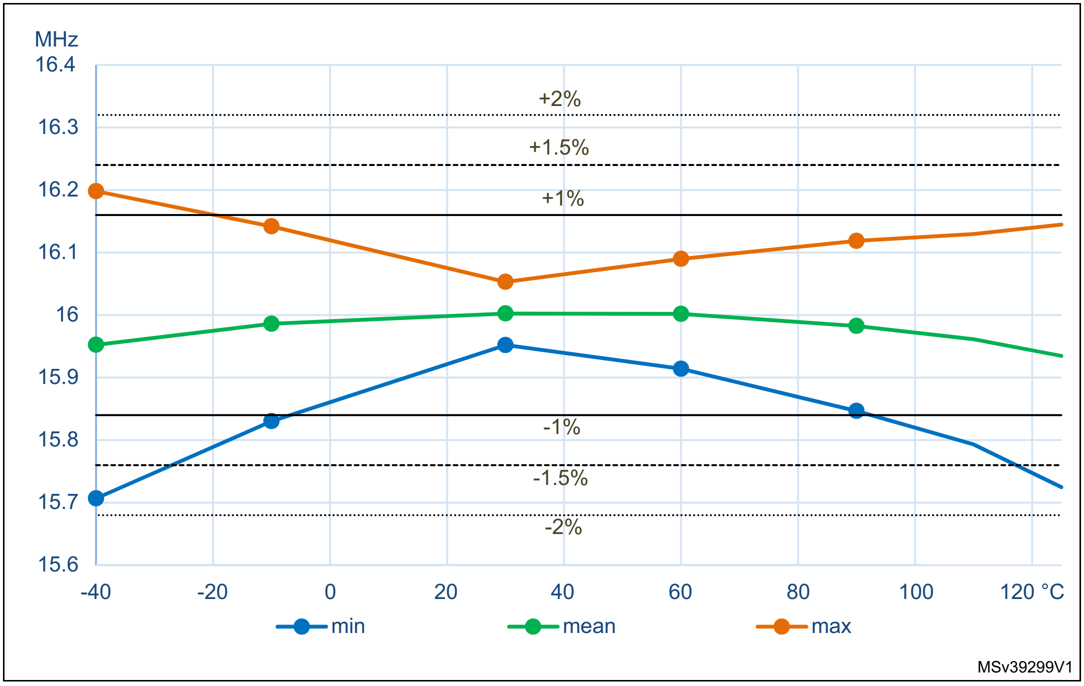
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
$\Delta_{Temp(HSI16)}$	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
$\Delta_{VDD(HSI16)}$	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
TRIM	HSI16 frequency user trimming step	From code 127 to 128	-8	-6	-4	%
		From code 63 to 64 From code 191 to 192	-5.8	-3.8	-1.8	
		For all other code increments	0.2	0.3	0.4	
D_{HSI16}[2]	Duty Cycle	-	45	-	55	%
$t_{su(HSI16)}$[2]	HSI16 oscillator start-up time	-	-	0.8	1.2	µs

Table 41. HSI16 oscillator characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{stab(HSI16)}$[2]	HSI16 oscillator stabilization time	-	-	3	5	µs
$I_{DD(HSI16)}$[2]	HSI16 oscillator power consumption	-	-	155	190	µA

1. Based on characterization results, not tested in production.
2. Guaranteed by design.

Figure 20. HSI16 frequency vs. temperature



Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 V to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
$t_{SU(LSI)}$[2]	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB(LSI)}$[2]	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD(LSI)}$[2]	LSI oscillator power consumption	-	-	110	180	nA

1. Based on characterization results, not tested in production.
2. Guaranteed by design.

5.3.9 PLL characteristics

The parameters given in *Table 43* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 43. PLL characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock frequency[2]	-	2.66	-	16	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	3.09	-	122	MHz
		Voltage scaling Range 2	3.09	-	40	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	12	-	128	MHz
		Voltage scaling Range 2	12	-	33	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	12	-	64	MHz
		Voltage scaling Range 2	12	-	16	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	MHz
		Voltage scaling Range 2	96	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 56 MHz	-	50	-	±ps
	RMS period jitter		-	40	-	
$I_{DD(PLL)}$	PLL power consumption on V_{DD}[1]	VCO freq = 96 MHz	-	200	260	µA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the two PLLs.

5.3.10 Flash memory characteristics

Table 44. Flash memory characteristics[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	85	125	µs
t_{prog_row}	Row (32 double word) programming time	Normal programming	2.7	4.6	ms
		Fast programming	1.7	2.8	
t_{prog_page}	Page (2 Kbyte) programming time	Normal programming	21.8	36.6	
		Fast programming	13.7	22.4	
t_{ERASE}	Page (2 Kbyte) erase time	-	22.0	40.0	
t_{prog_bank}	Bank (128 Kbyte[2]) programming time	Normal programming	1.4	2.4	s
		Fast programming	0.9	1.4	
t_{ME}	Mass erase time	-	22.1	40.1	ms

Table 44. Flash memory characteristics[1] (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(FlashA)}$	Average consumption from V_{DD}	Programming	3	-	mA
		Page erase	3	-	
		Mass erase	3	-	
$I_{DD(FlashP)}$	Maximum current (peak)	Programming, 2 µs peak duration	7	-	mA
		Erase, 41 µs peak duration	7	-	

1. Guaranteed by design.
2. Values provided also apply to devices with less Flash memory than one 128 Kbyte bank

Table 45. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min[1]	Unit
N_{END}	Endurance	T_A = -40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Years
		1 kcycle[2] at T_A = 105 °C	15	
		1 kcycle[2] at T_A = 125 °C	7	
		10 kcycles[2] at T_A = 55 °C	30	
		10 kcycles[2] at T_A = 85 °C	15	
		10 kcycles[2] at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 46*. They are based on the EMS levels and classes defined in application note AN1709.

Table 46. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, LQFP64, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, LQFP64, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- corrupted program counter
- unexpected reset
- critical data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 47. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8 MHz / 64 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	7	dBμV
			30 MHz to 130 MHz	-1	
			130 MHz to 1 GHz	8	
			1 GHz to 2 GHz	7	
			EMI level	2.5	-

5.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 48. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-002	C2a	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current is injected to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 49. Electrical sensitivity

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78	II Level A

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIO1} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter: ADC error above a certain limit (higher than 5 LSB TUE), induced leakage current on adjacent pins out of conventional limits (-5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 50. I/O current injection susceptibility(1)

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}	Injected current on pin	All except PA4, PA5, PA6, PB0, PB3, and PC0	-5	N/A	mA
		PA4, PA5	-5	0	mA
		PA6, PB0, PB3, and PC0	0	N/A	mA

1. Based on characterization results, not tested in production.

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under the conditions summarized in *Table 21: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Table 51. I/O static characteristics

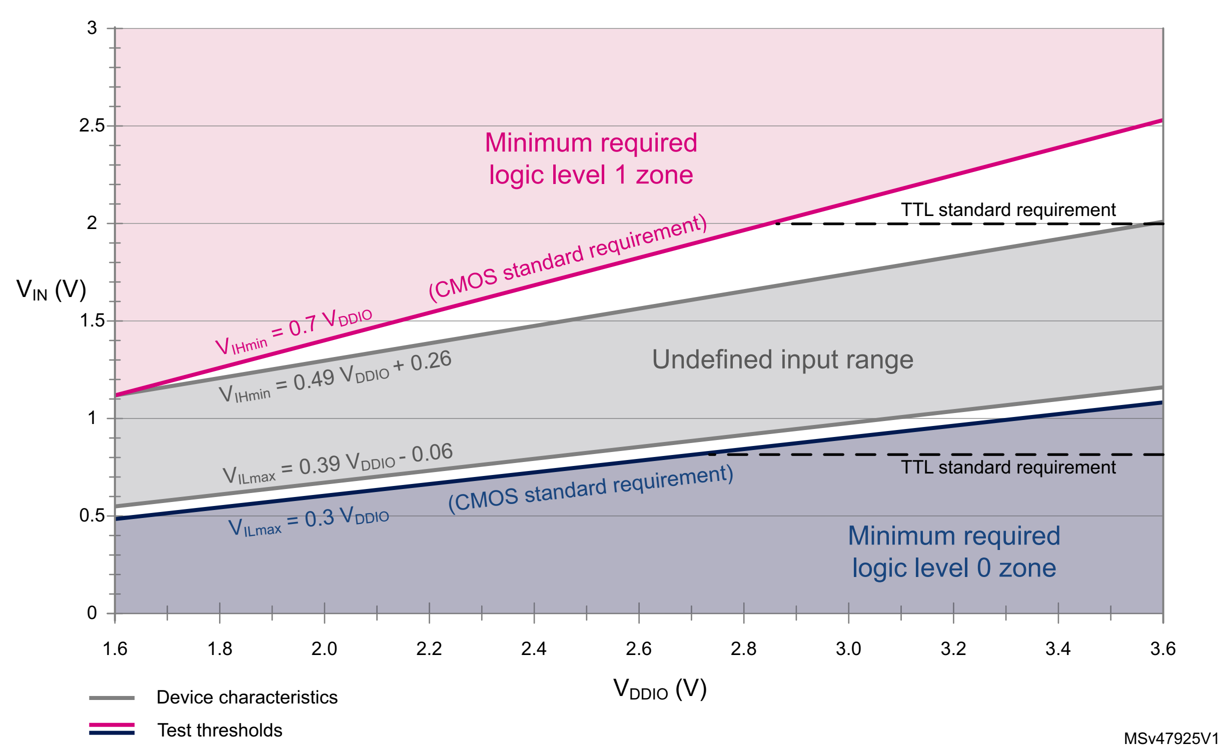
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	All except FT_c	$1.62\ V < V_{DDIO1} < 3.6\ V$	-	-	$0.3 \times V_{DDIO1}$(2)	V
						$0.39 \times V_{DDIO1} - 0.06$(3)	
		FT_c	$2\ V < V_{DDIO1} < 2.7\ V$	-	-	$0.3 \times V_{DDIO1}$	
			$1.62\ V < V_{DDIO1} < 2.7\ V$	-	-	$0.25 \times V_{DDIO1}$	
V_{IH}(1)	I/O input high level voltage	All except FT_c	$1.62\ V < V_{DDIO1} < 3.6\ V$	$0.7 \times V_{DDIO1}$(2)	-	-	V
				$0.49 \times V_{DDIO1} + 0.26$(3)	-	-	
		FT_c	$1.62\ V < V_{DDIO1} < 3.6\ V$	$0.7 \times V_{DDIO1}$	-	5	
V_{hys}(3)	I/O input hysteresis	TT_xx, FT_xx, NRST	$1.62\ V < V_{DDIO1} < 3.6\ V$	-	200	-	mV
I_{lkg}	Input leakage current(3)	FT_xx except FT_c and FT_d	$0 < V_{IN} \leq V_{DDIO1}$	-	-	±70	nA
			$V_{DDIO1} \leq V_{IN} \leq V_{DDIO1}+1\ V$	-	-	600(4)	
			$V_{DDIO1} +1\ V < V_{IN} \leq 5.5\ V$(3)	-	-	150(4)	
		FT_c	$0 < V_{IN} \leq V_{DDIO1}$	-	-	2000	
			$V_{DDIO1} < V_{IN} \leq 5\ V$	-	-	3000(4)	
		FT_d	$0 < V_{IN} \leq V_{DDIO1}$	-	-	4500	
			$V_{DDIO1} < V_{IN} \leq 5.5\ V$	-	-	9000(4)	
		TT_a	$0 < V_{IN} \leq V_{DDIO1}$	-	-	±150	
			$V_{DDIO1} < V_{IN} \leq V_{DDIO1} + 0.3\ V$	-	-	2000(4)	
R_{PU}	Weak pull-up equivalent resistor (5)	$V_{IN} = V_{SS}$		25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DDIO1}$		25	40	55	kΩ
C_{IO}	I/O pin capacitance	-		-	5	-	pF

1. Refer to *Figure 21: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.

4. This value represents the pad leakage of the I/O itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x I_{lkg}(Max).
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters, as shown in *Figure 21*.

Figure 21. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±6 mA, and up to ±15 mA with relaxed V_{OL}/V_{OH}.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIO1,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 18: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 18: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in

Table 21: General operating conditions. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 52. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\lvert I_{IO}\rvert$ = 2 mA for FT_c I/Os = 6 mA for other I/Os V_{DDIO1} ≥ 2.7 V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIO1} - 0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\lvert I_{IO}\rvert$ = 2 mA for FT_c I/Os = 6 mA for other I/Os V_{DDIO1} ≥ 2.7 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	All I/Os except FT_c $\lvert I_{IO}\rvert$ = 15 mA V_{DDIO1} ≥ 2.7 V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIO1} - 1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 1 mA for FT_c I/Os = 3 mA for other I/Os V_{DDIO1} ≥ 1.62 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIO1} - 0.45	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with _f option)	$\lvert I_{IO}\rvert$ = 20 mA V_{DDIO1} ≥ 2.7 V	-	0.4	
		$\lvert I_{IO}\rvert$ = 9 mA V_{DDIO1} ≥ 1.62 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 18: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 22* and *Table 53*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 53. I/O AC characteristics(1)(2)

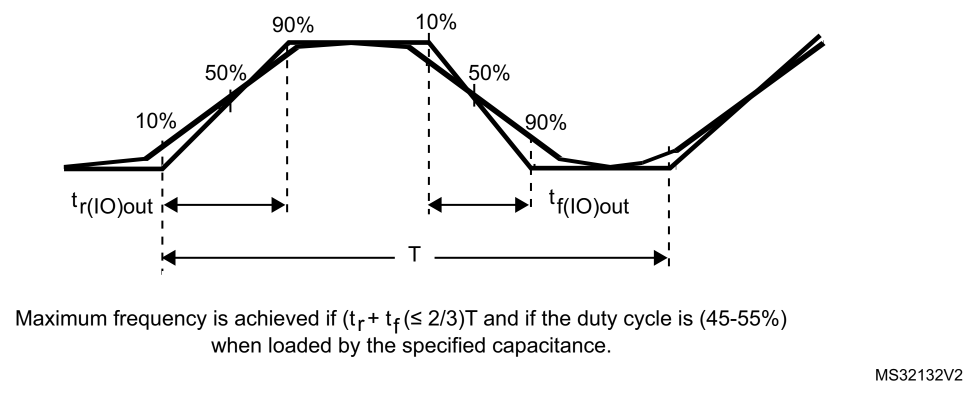
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	2	MHz
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	0.35	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	3	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	0.45	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	100	ns
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	225	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	75	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	150	

Table 53. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	10	MHz
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	2	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	15	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	2.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	30	ns
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	60	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	15	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	30	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	30	MHz
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	15	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	60	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	30	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	11	ns
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	22	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	4	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	8	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	60	MHz
			C=30 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	30	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	80(3)	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	40	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	5.5	ns
			C=30 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	11	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	2.5	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	5	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0444 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 64 MHz.
4. The fall time is defined between 70% and 30% of the output waveform, according to I^2C specification.

Figure 22. I/O AC characteristics definition[1]



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

1. Refer to *Table 53: I/O AC characteristics*.

5.3.15 NRST input characteristics

The NRST input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

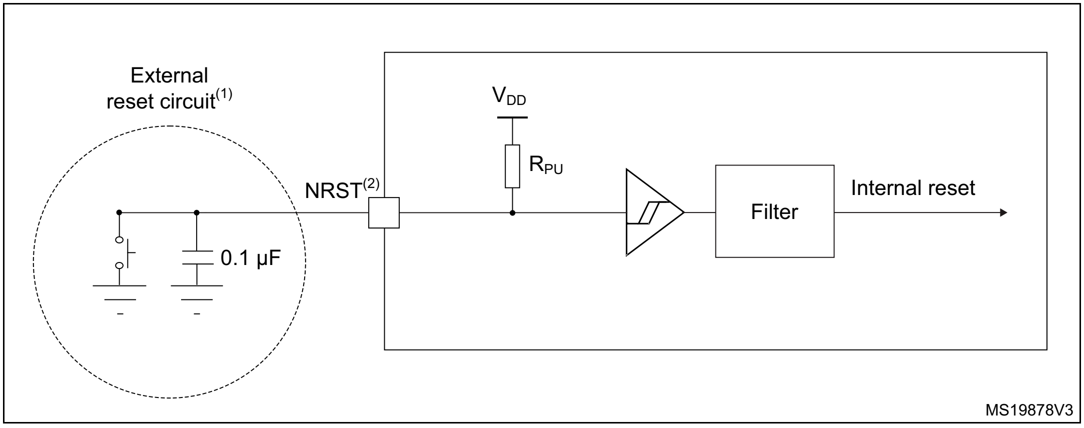
Table 54. NRST pin characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 x V_{DDIO1}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7 x V_{DDIO1}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor[2]	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.7 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 23. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 54: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.16 Analog switch booster

Table 55. Analog switch booster characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62 V	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for $1.62 V \le V_{DD} \le 2.0 V$	-	-	250	µA
	Booster consumption for $2.0 V \le V_{DD} \le 2.7 V$	-	-	500	
	Booster consumption for $2.7 V \le V_{DD} \le 3.6 V$	-	-	900	

1. Guaranteed by design.

5.3.17 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 56* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 21: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 56. ADC characteristics[1]

Symbol	Parameter	Conditions[2]	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \ge 2 V$	2	-	V_{DDA}	V
		$V_{DDA} < 2 V$	V_{DDA}			

Table 56. ADC characteristics[1] (continued)

Symbol	Parameter	Conditions[2]	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	Range 1	0.14	-	35	MHz
		Range 2	0.14	-	16	
f_S	Sampling rate	12 bits	-	-	2.50	MSps
		10 bits	-	-	2.92	
		8 bits	-	-	3.50	
		6 bits	-	-	4.38	
f_{TRIG}	External trigger frequency	f_{ADC} = 35 MHz; 12 bits	-	-	2.33	MHz
		12 bits	-	-	$f_{ADC}/15$	
V_{AIN} [3]	Conversion voltage range	-	V_{SSA}	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	ADC power-up time	-	2			Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 35 MHz	2.35			µs
		-	82			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency	CKMODE = 00	2	-	3	$1/f_{ADC}$
		CKMODE = 01	6.5			$1/f_{PCLK}$
		CKMODE = 10	12.5			
		CKMODE = 11	3.5			
t_S	Sampling time	f_{ADC} = 35 MHz; V_{DDA} > 2V	0.043	-	4.59	µs
			1.5	-	160.5	$1/f_{ADC}$
		f_{ADC} = 35 MHz; V_{DDA} < 2V	0.1	-	4.59	µs
			3.5		160.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 35 MHz Resolution = 12 bits	0.40	-	4.95	µs
		Resolution = 12 bits	t_S + 12.5 cycles for successive approximation = 14 to 173			$1/f_{ADC}$
t_{IDLE}	Laps of time allowed between two conversions without rearm	-	-	-	100	µs

Table 56. ADC characteristics[1] (continued)

Symbol	Parameter	Conditions[2]	Min	Typ	Max	Unit
$I_{DDA(ADC)}$	ADC consumption from V_{DDA}	f_S = 2.5 MSps	-	410	-	µA
		f_S = 1 MSps	-	164	-	
		f_S = 10 kSps	-	17	-	
$I_{DDV(ADC)}$	ADC consumption from V_{REF+}	f_S = 2.5 MSps	-	65	-	µA
		f_S = 1 MSps	-	26	-	
		f_S = 10 kSps	-	0.26	-	

1. Guaranteed by design
2. I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when V_{DDA} ≥ 2.4 V.
3. V_{REF+} is internally connected to V_{DDA} on some packages.Refer to *Section 4: Pinouts, pin description and alternate functions* for further details.

Table 57. Maximum ADC R_{AIN}

Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN}[1][2] (Ω)
12 bits	1.5[3]	43	50
	3.5	100	680
	7.5	214	2200
	12.5	357	4700
	19.5	557	8200
	39.5	1129	15000
	79.5	2271	33000
	160.5	4586	50000
10 bits	1.5[3]	43	68
	3.5	100	820
	7.5	214	3300
	12.5	357	5600
	19.5	557	10000
	39.5	1129	22000
	79.5	2271	39000
	160.5	4586	50000

Table 57. Maximum ADC R_{AIN} (continued)

Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN}(1)(2) (Ω)
8 bits	1.5(3)	43	82
	3.5	100	1500
	7.5	214	3900
	12.5	357	6800
	19.5	557	12000
	39.5	1129	27000
	79.5	2271	50000
	160.5	4586	50000
6 bits	1.5(3)	43	390
	3.5	100	2200
	7.5	214	5600
	12.5	357	10000
	19.5	557	15000
	39.5	1129	33000
	79.5	2271	50000
	160.5	4586	50000

1. Guaranteed by design.
2. I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when $V_{DDA} < 2.4$ V and disabled when $V_{DDA} \geq 2.4$ V.
3. Only allowed with $V_{DDA} > 2$ V

Table 58. ADC accuracy(1)(2)(3)

Symbol	Parameter	Conditions(4)	Min	Typ	Max	Unit
ET	Total unadjusted error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; $T_A = 25$ °C	-	3	4	LSB
		2 V < $V_{DDA}=V_{REF+}$ < 3.6 V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; T_A = entire range	-	3	6.5	
		1.65 V < $V_{DDA}=V_{REF+}$ < 3.6 V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \leq 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \leq 1.1$ MSps;	-	3	7.5	

Table 58. ADC accuracy(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)	Min	Typ	Max	Unit
EO	Offset error	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	-	1.5	2	LSB
		2 V < V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	1.5	4.5	
		1.65 V < V_{DDA}=V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	-	1.5	5.5	
EG	Gain error	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	-	3	3.5	LSB
		2 V < V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	3	5	
		1.65 V < V_{DDA}=V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	-	3	6.5	
ED	Differential linearity error	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	-	1.2	1.5	LSB
		2 V < V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	1.2	1.5	
		1.65 V < V_{DDA}=V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	-	1.2	1.5	
EL	Integral linearity error	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	-	2.5	3	LSB
		2 V < V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	2.5	3	
		1.65 V < V_{DDA}=V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	-	2.5	3.5	

Table 58. ADC accuracy[1][2][3] (continued)

Symbol	Parameter	Conditions[4]	Min	Typ	Max	Unit
ENOB	Effective number of bits	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; $T_A = 25$ °C	10.1	10.2	-	bit
		$2 \text{ V} < V_{DDA}=V_{REF+} < 3.6$ V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; T_A = entire range	9.6	10.2	-	
		$1.65 \text{ V} < V_{DDA}=V_{REF+} < 3.6$ V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \leq 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \leq 1.1$ MSps;	9.5	10.2	-	
SINAD	Signal-to-noise and distortion ratio	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; $T_A = 25$ °C	62.5	63	-	dB
		$2 \text{ V} < V_{DDA}=V_{REF+} < 3.6$ V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; T_A = entire range	59.5	63	-	
		$1.65 \text{ V} < V_{DDA}=V_{REF+} < 3.6$ V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \leq 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \leq 1.1$ MSps;	59	63	-	
SNR	Signal-to-noise ratio	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; $T_A = 25$ °C	63	64	-	dB
		$2 \text{ V} < V_{DDA}=V_{REF+} < 3.6$ V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; T_A = entire range	60	64	-	
		$1.65 \text{ V} < V_{DDA}=V_{REF+} < 3.6$ V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \leq 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \leq 1.1$ MSps;	60	64	-	
THD	Total harmonic distortion	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; $T_A = 25$ °C	-	-74	-73	dB
		$2 \text{ V} < V_{DDA}=V_{REF+} < 3.6$ V; $f_{ADC} = 35$ MHz; $f_s \leq 2.5$ MSps; T_A = entire range	-	-74	-70	
		$1.65 \text{ V} < V_{DDA}=V_{REF+} < 3.6$ V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \leq 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \leq 1.1$ MSps;	-	-74	-70	

1. Based on characterization results, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. Injecting negative current on any analog input pin significantly reduces the accuracy of A-to-D conversion of signal on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins susceptible to receive negative current.
4. I/O analog switch voltage booster enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when $V_{DDA} < 2.4$ V and disabled when $V_{DDA} \geq 2.4$ V.

Figure 24. ADC accuracy characteristics

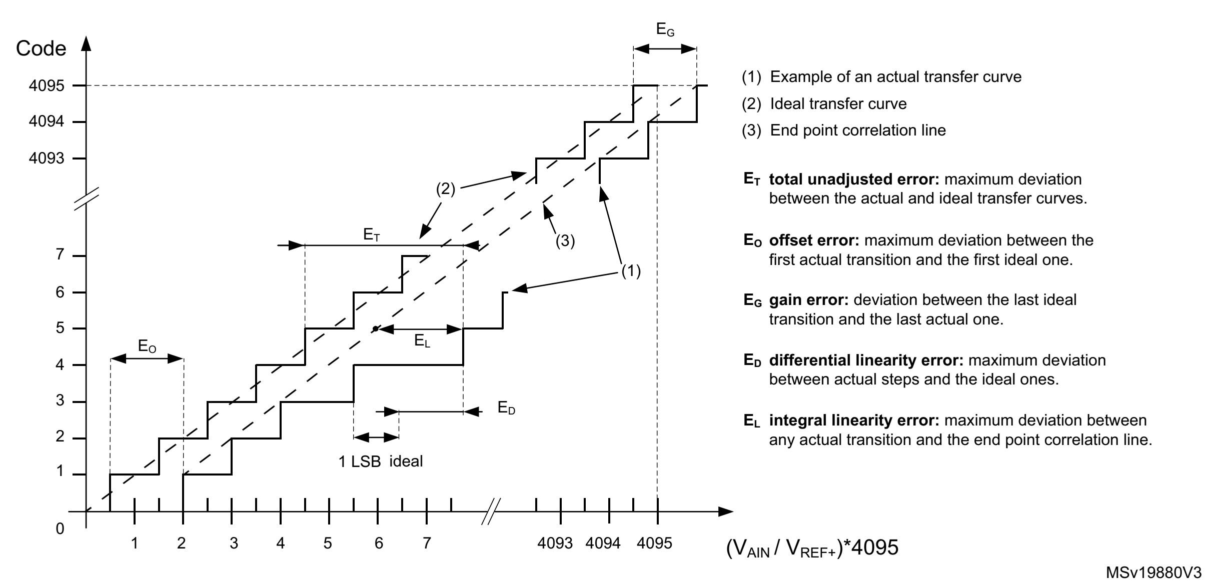
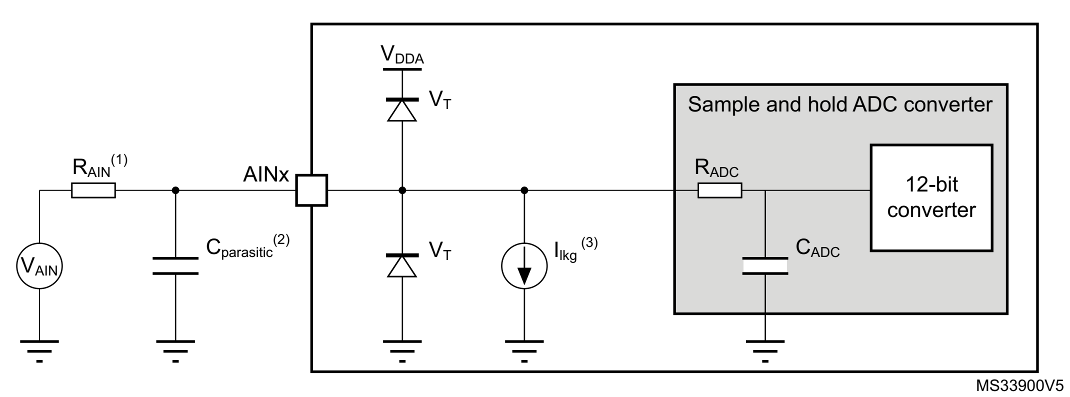


Figure 25. Typical connection diagram using the ADC



1. Refer to *Table 56: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 51: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 51: I/O static characteristics* for the values of Ilkg.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 13: Power supply scheme*. The 100 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

5.3.18 Digital-to-analog converter characteristics

Table 59. DAC characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	V_{DDA}	V
		Other modes		1.80	-		
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	$V_{DD} = 2.7$ V		-	-	2	kΩ
		$V_{DD} = 2.0$ V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	$V_{DD} = 2.7$ V		-	-	16.5	kΩ
		$V_{DD} = 2.0$ V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	$V_{REF+} - 0.2$	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}[2]	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 59. DAC characteristics[1] (continued)

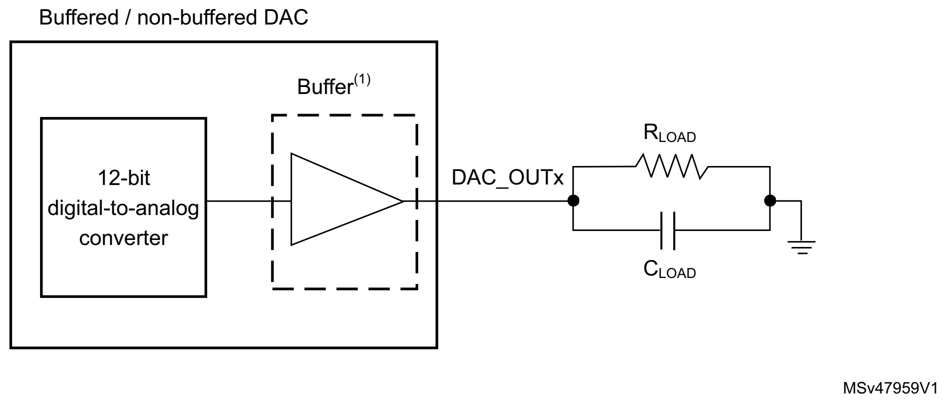
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimum time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB)	DAC_MCR:MODEx[2:0] = 000 or 001 CL ≤ 50 pF; RL ≥ 5 kΩ		1	-	-	µs
		DAC_MCR:MODEx[2:0] = 010 or 011 CL ≤ 10 pF		1.4	-	-	
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-[3]	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
$I_{DDA(DAC)}$	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x $T_{on}/(T_{on}+T_{off})$[4]	670 x $T_{on}/(T_{on}+T_{off})$[4]	

Table 59. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDV(DAC)}$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x $T_{on}/(T_{on}+T_{off})$(4)	400 x $T_{on}/(T_{on}+T_{off})$(4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x $T_{on}/(T_{on}+T_{off})$(4)	205 x $T_{on}/(T_{on}+T_{off})$(4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 51: I/O static characteristics*.
4. T_{on} is the Refresh phase duration. T_{off} is the Hold phase duration. Refer to RM0444 reference manual for more details.

Figure 26. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 60. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	

Table 60. DAC accuracy[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

5.3.19 Voltage reference buffer characteristics

Table 61. VREFBUF characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	$V_{RS} = 0$	2.4	-	3.6	V
			$V_{RS} = 1$	2.8	-	3.6	
		Degraded mode[2]	$V_{RS} = 0$	1.65	-	2.4	
			$V_{RS} = 1$	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	$V_{RS} = 0$	2.046[3]	2.048	2.049[3]	
			$V_{RS} = 1$	2.498[3]	2.5	2.502[3]	
		Degraded mode[2]	$V_{RS} = 0$	V_{DDA}-150 mV	-	V_{DDA}	
			$V_{RS} = 1$	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of C_{load}	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA

Table 61. VREFBUF characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{Coeff\_vrefbuf}$	Temperature coefficient of VREFBUF[4]	-40 °C < T_J < +125 °C	-	-	50	ppm/ °C
PSRR	Power supply rejection	DC	40	60	-	dB
		100 kHz	25	40	-	
t_{START}	Start-up time	CL = 0.5 µF[5]	-	300	350	µs
		CL = 1.1 µF[5]	-	500	650	
		CL = 1.5 µF[5]	-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (6)	-	-	8	-	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The temperature coefficient at VREF+ output is the sum of $T_{Coeff\_vrefint}$ and $T_{Coeff\_vrefbuf}$.
5. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
6. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

5.3.20 Comparator characteristics

Table 62. COMP characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	V
V_{BG}[2]	Scaler input voltage	-	V_{REFINT}			V
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)	-	200	300	nA
		BRG_EN=1 (bridge enable)	-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-	-	100	200	µs

Table 62. COMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode		-	-	5	µs
		Medium-speed mode		-	-	15	
t_D	Propagation delay	200 mV step; 100 mV overdrive	High-speed mode	-	30	50	ns
			Medium-speed mode	-	0.3	0.6	µs
		>200 mV step; 100 mV overdrive	High-speed mode	-	-	70	ns
			Medium-speed mode	-	-	1.2	µs
V_{offset}	Comparator offset error	Full common mode range		-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	10	-	
		Medium hysteresis		-	20	-	
		High hysteresis		-	30	-	
$I_{DDA(COMP)}$	Comparator consumption from V_{DDA}	Medium-speed mode; No deglitcher	Static	-	5	7.5	µA
			With 50 kHz and ±100 mV overdrive square signal	-	6	-	
		Medium-speed mode; With deglitcher	Static	-	7	10	
			With 50 kHz and ±100 mV overdrive square signal	-	8	-	
		High-speed mode	Static	-	250	400	
			With 50 kHz and ±100 mV overdrive square signal	-	250	-	

1. Guaranteed by design.
2. Refer to *Table 24: Embedded internal voltage reference*.

5.3.21 Temperature sensor characteristics

Table 63. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	0.742	0.76	0.785	V
$t_{START(TS\_BUF)}$(1)	Sensor Buffer Start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs

Table 63. TS characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
t_{S_temp}[1]	ADC sampling time when reading the temperature	5	-	-	µs
$I_{DD(TS)}$[1]	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Based on characterization results, not tested in production.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

5.3.22 V_{BAT} monitoring characteristics

Table 64. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er[1]	Error on Q	-10	-	10	%
t_{S_vbat}[1]	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 65. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

5.3.23 Timer characteristics

The parameters given in the following tables are guaranteed by design. Refer to *Section 5.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 66. TIMx[1] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	15.625	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 64 MHz	0	40	
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	

Table 66. TIMx(1) characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	0.015625	1024	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	-	67.10	s

1. TIMx, is used as a general term in which x stands for 1, 2, 3, 4, 5, 6, 7, 8, 15, 16 or 17.

Table 67. IWDG min/max timeout period at 32 kHz LSI clock(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings further depend on the phase of the APB interface clock versus the LSI clock, which causes an uncertainty of one RC period.

5.3.24 Characteristics of communication interfaces

I^{2}C-bus interface characteristics

The I^{2}C-bus interface meets timing requirements of the I^{2}C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The timings are guaranteed by design as long as the I2C peripheral is properly configured (refer to the reference manual RM0444) and when the I2CCLK frequency is greater than the minimum shown in the following table.

Table 68. Minimum I2CCLK frequency

Symbol	Parameter	Condition		Typ	Unit
$f_{I2CCLK(min)}$	Minimum I2CCLK frequency for correct operation of I2C peripheral	Standard-mode		2	MHz
		Fast-mode	Analog filter enabled DNF = 0	9	
			Analog filter disabled DNF = 1	9	
		Fast-mode Plus	Analog filter enabled DNF = 0	18	
			Analog filter disabled DNF = 1	16	

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIO1} is disabled, but is still present. Only FT_f I/O pins support Fm+ low-level output current maximum requirement. Refer to *Section 5.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the following table for its characteristics:

Table 69. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter(2)	50	260	ns

1. Based on characterization results, not tested in production.
2. Spikes shorter than the limiting duration are suppressed.

SPI/I^{2}S characteristics

Unless otherwise specified, the parameters given in *Table 70* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 21: General operating conditions*. The additional general conditions are:

- OSPEEDRy[1:0] set to 11 (output speed)
- capacitive load C = 30 pF
- measurement points at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 70. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 1.65 < V_{DD} < 3.6 V Range 1	-	-	32	MHz
		Master transmitter 1.65 < V_{DD} < 3.6 V Range 1			32	
		Slave receiver 1.65 < V_{DD} < 3.6 V Range 1			32	
		Slave transmitter/full duplex 2.7 < V_{DD} < 3.6 V Range 1			32	
		Slave transmitter/full duplex 1.65 < V_{DD} < 3.6 V Range 1			23	
		1.65 < V_{DD} < 3.6 V Range 2			8	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	4 x T_{PCLK}	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	2 x T_{PCLK}	-	-	ns
$t_{w(SCKH)}$	SCK high time	Master mode	T_{PCLK} - 1.5	T_{PCLK}	T_{PCLK} + 1.5	ns
$t_{w(SCKL)}$	SCK low time	Master mode	T_{PCLK} - 1.5	T_{PCLK}	T_{PCLK} + 1.5	ns
$t_{su(MI)}$	Master data input setup time	-	1	-	-	ns
$t_{su(SI)}$	Slave data input setup time	-	1	-	-	ns
$t_{h(MI)}$	Master data input hold time	-	5	-	-	ns
$t_{h(SI)}$	Slave data input hold time	-	1	-	-	ns
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns
$t_{v(SO)}$	Slave data output valid time	2.7 < V_{DD} < 3.6 V Range 1	-	9	14	ns
		1.65 < V_{DD} < 3.6 V Range 1	-	9	21	
		1.65 < V_{DD} < 3.6 V Voltage Range 2	-	11	24	
$t_{v(MO)}$	Master data output valid time	-	-	3	5	ns

Table 70. SPI characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(SO)}$	Slave data output hold time	-	5	-	-	ns
$t_{h(MO)}$	Master data output hold time	-	1	-	-	ns

1. Based on characterization results, not tested in production.

Figure 27. SPI timing diagram - slave mode and CPHA = 0

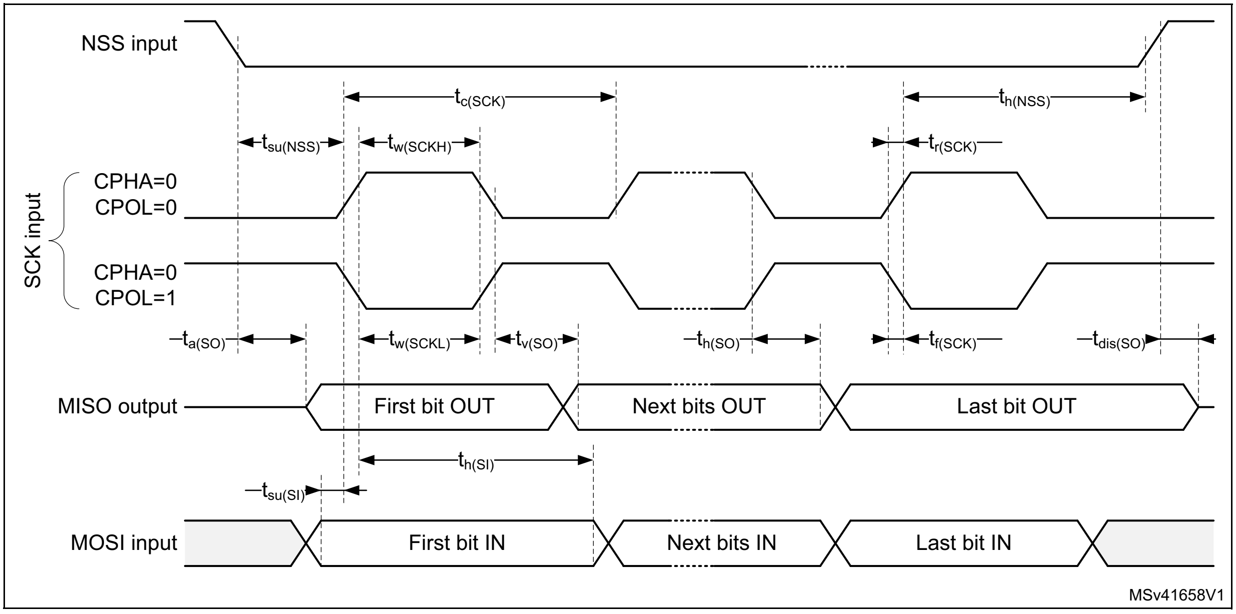
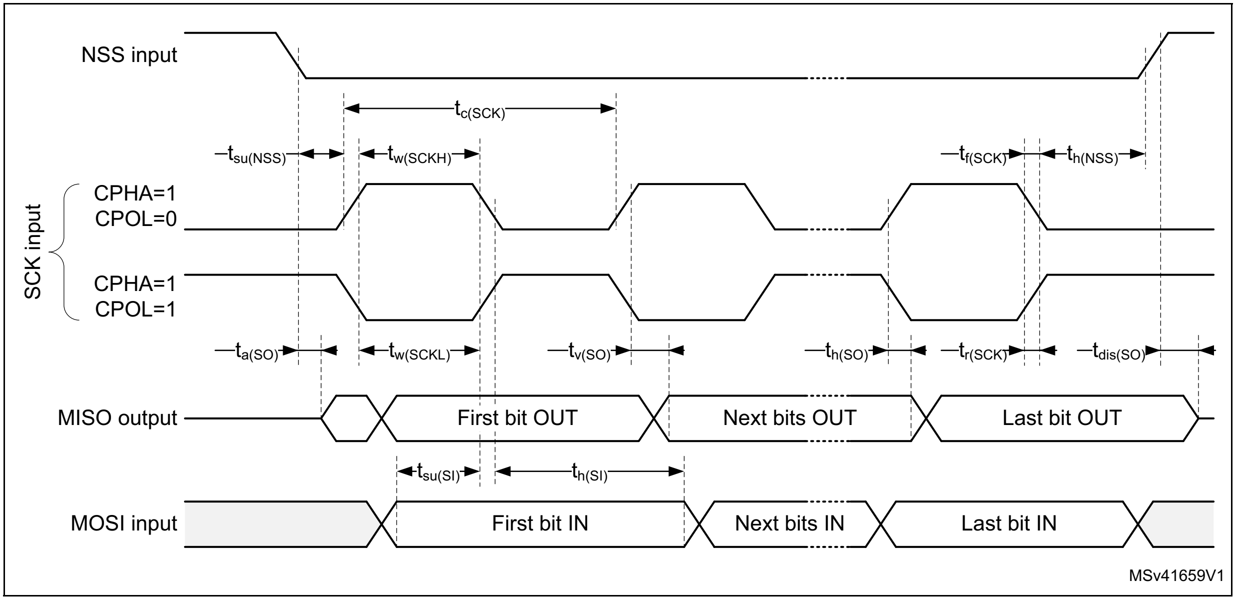
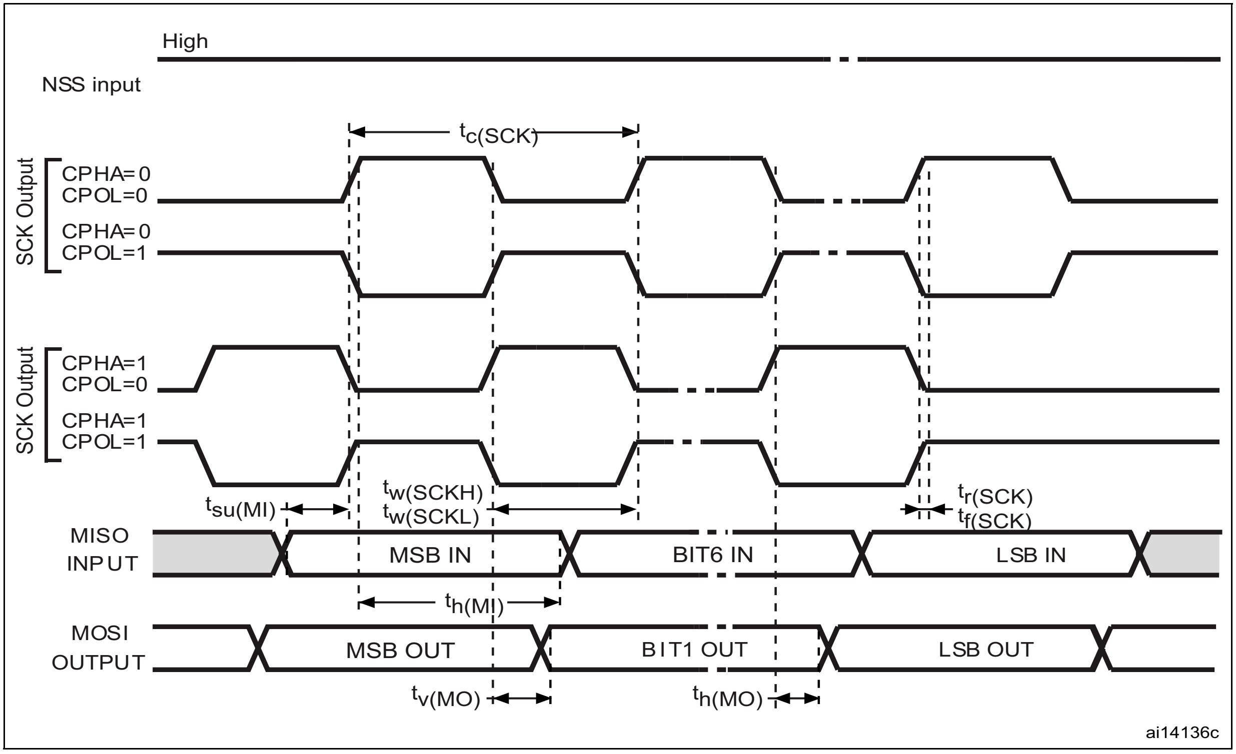


Figure 28. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 29. SPI timing diagram - master mode



1. Measurement points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 71. I^{2}S characteristics(1)

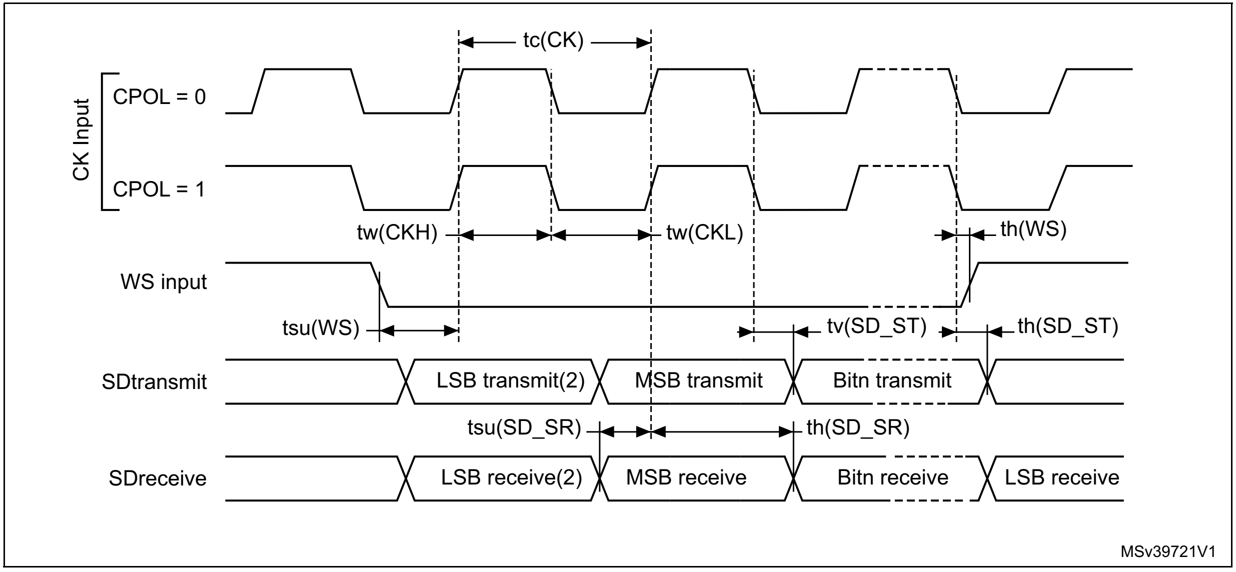
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	f_{MCK}= 256 x Fs; (Fs = audio sampling frequency) Fs_{min} = 8 kHz; Fs_{max} = 192 kHz;	2.048	49.152	MHz
f_{CK}	I2S clock frequency	Master data	-	64xFs	MHz
		Slave data	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%

Table 71. I^{2}S characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(WS)}$	WS valid time	Master mode	-	8	ns
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	4	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	4	-	
$t_{su(SD\_SR)}$		Slave receiver	5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	4.5	-	
$t_{h(SD\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_ST)}$	Data output valid time - slave transmitter	after enable edge; $2.7 < V_{DD} < 3.6V$	-	16	
		after enable edge; $1.65 < V_{DD} < 3.6V$		23	
$t_{v(SD\_MT)}$	Data output valid time - master transmitter	after enable edge	-	5.5	
$t_{h(SD\_ST)}$	Data output hold time - slave transmitter	after enable edge	8	-	
$t_{h(SD\_MT)}$	Data output hold time - master transmitter	after enable edge	1	-	

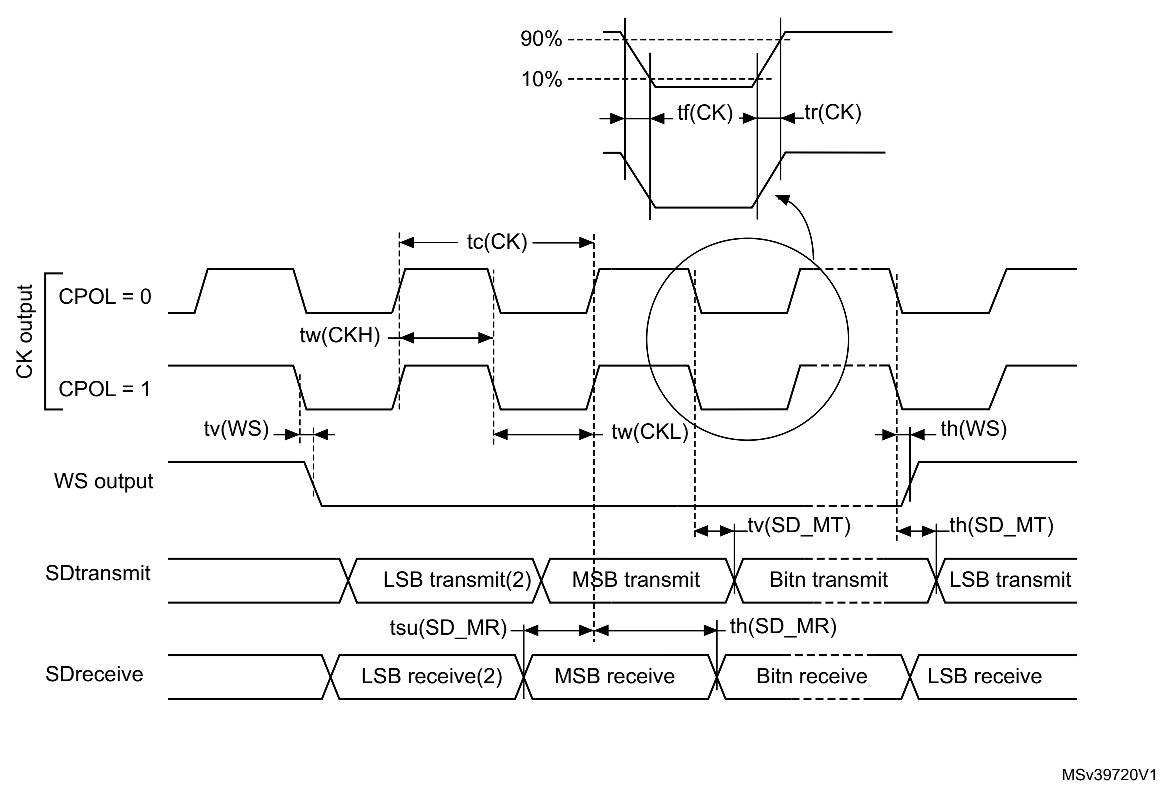
1. Based on characterization results, not tested in production.

Figure 30. I^{2}S slave timing diagram (Philips protocol)



1. Measurement points are done at CMOS levels: 0.3 V_{DDIO1} and 0.7 V_{DDIO1}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 31. I^2S master timing diagram (Philips protocol)



1. Based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USART characteristics

Unless otherwise specified, the parameters given in *Table 72* for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 21: General operating conditions*. The additional general conditions are:

- OSPEEDRy[1:0] set to 10 (output speed)
- capacitive load C = 30 pF
- measurement points at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, and RX for USART).

Table 72. USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	8	MHz
		Slave mode	-	-	21	

Table 72. USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker} + 2	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(CKH)}$	CK high time	Master mode	1 / f_{CK} / 2 - 1	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1	
$t_{w(CKL)}$	CK low time					
$t_{su(RX)}$	Data input setup time	Master mode	t_{ker} + 2	-	-	
		Slave mode	4	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	1	-	-	
		Slave mode	0.5	-	-	
$t_{v(TX)}$	Data output valid time	Master mode	-	0.5	1	
		Slave mode	-	10	19	
$t_{h(TX)}$	Data output hold time	Master mode	0	-	-	
		Slave mode	7	-	-	

5.3.25 UCPD characteristics

UCPD1 and UCPD2 controllers comply with USB Type-C Rev.1.2 and USB Power Delivery Rev. 3.0 specifications.

Table 73. UCPD operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	UCPD operating supply voltage	Sink mode only	3.0	3.3	3.6	V
		Sink and source mode	3.135	3.3	3.465	V

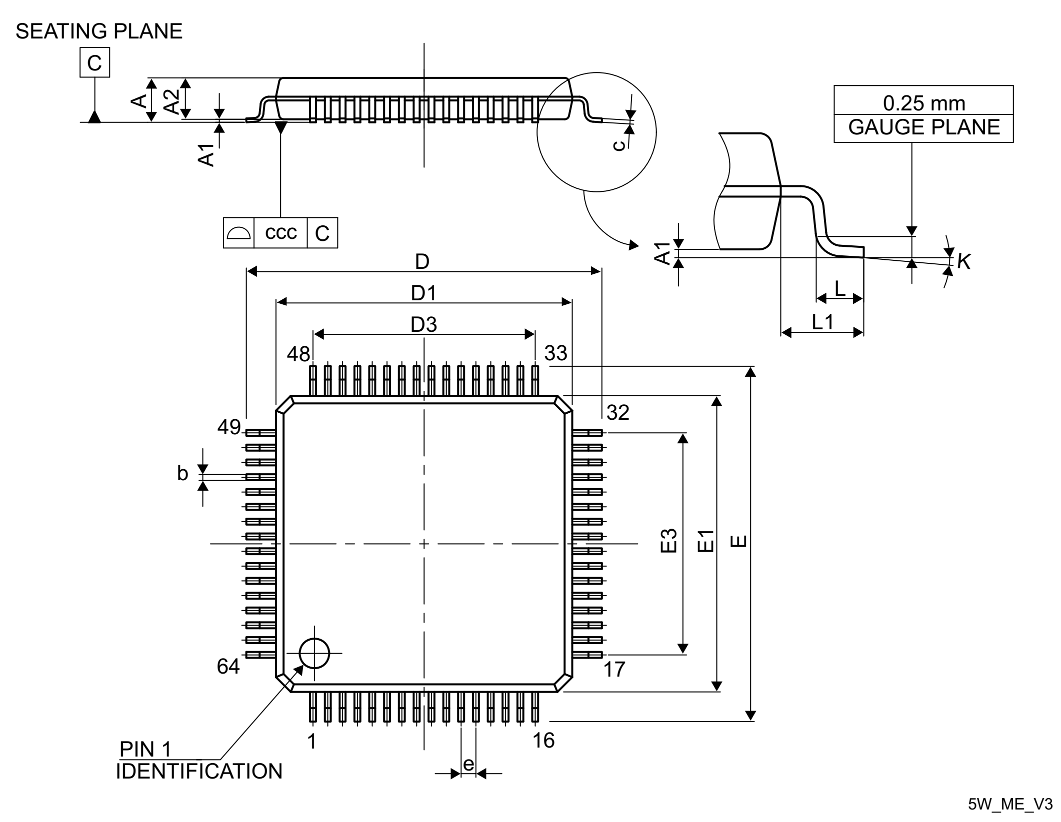
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 32. LQFP64 package outline



1. Drawing is not to scale.

Table 74. LQFP64 package mechanical data

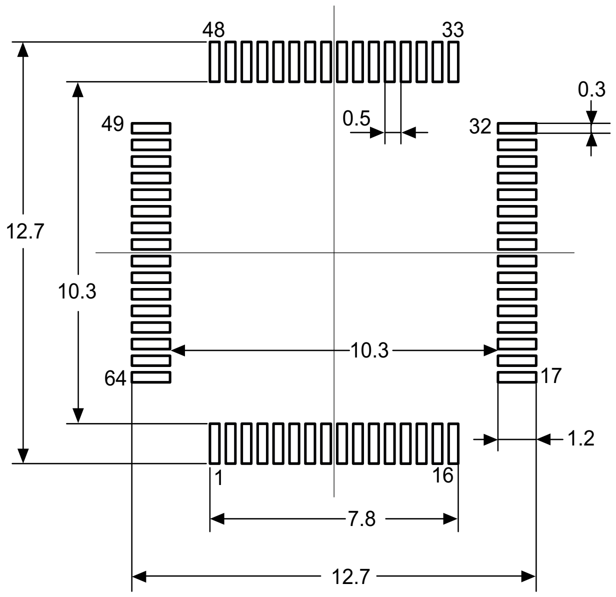
Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 74. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 33. Recommended footprint for LQFP64 package



1. Dimensions are expressed in millimeters.

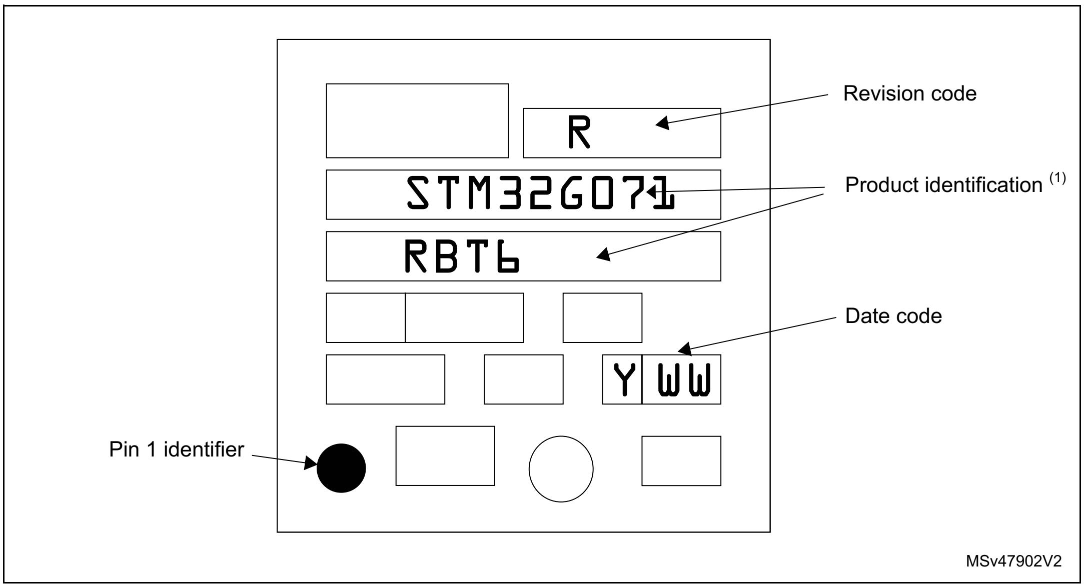
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 34. LQFP64 package marking example

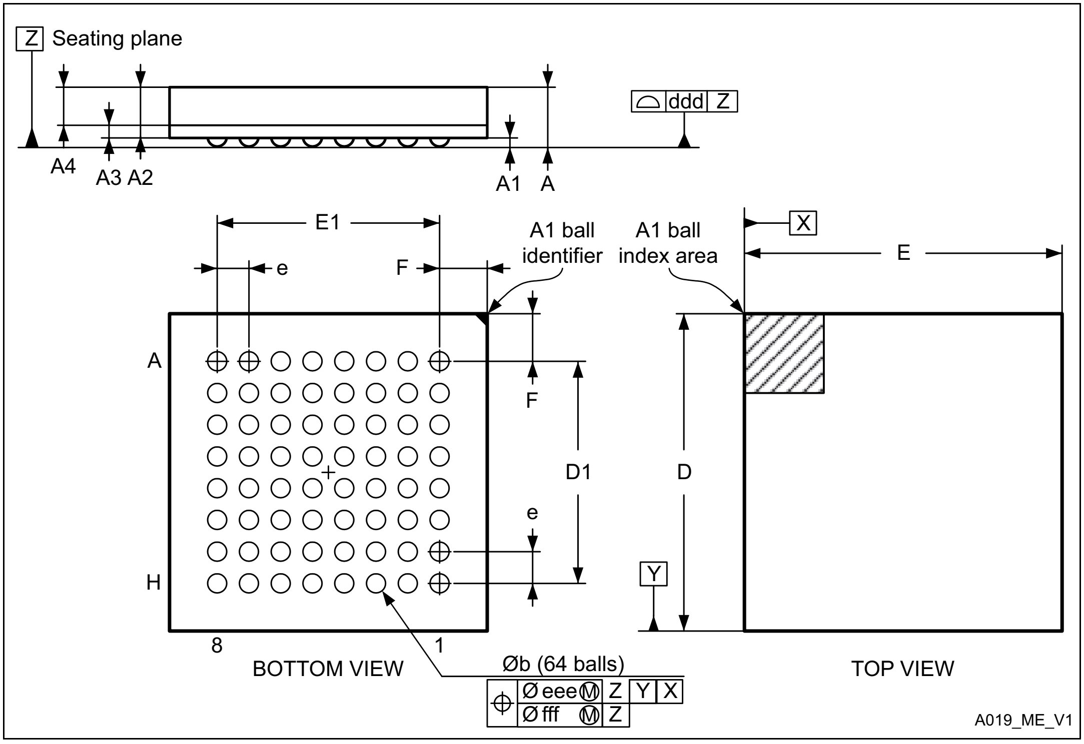


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.2 UFBGA64 package information

UFBGA64 is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra-low-profile fine-pitch ball grid array package.

Figure 35. UFBGA64 package outline



1. Drawing is not to scale.

Table 75. UFBGA64 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

Table 75. UFBGA64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. Recommended footprint for UFBGA64 package

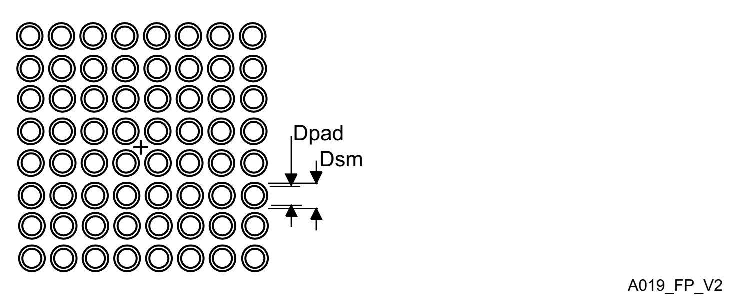


Table 76. Recommended PCB design rules for UFBGA64 package

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

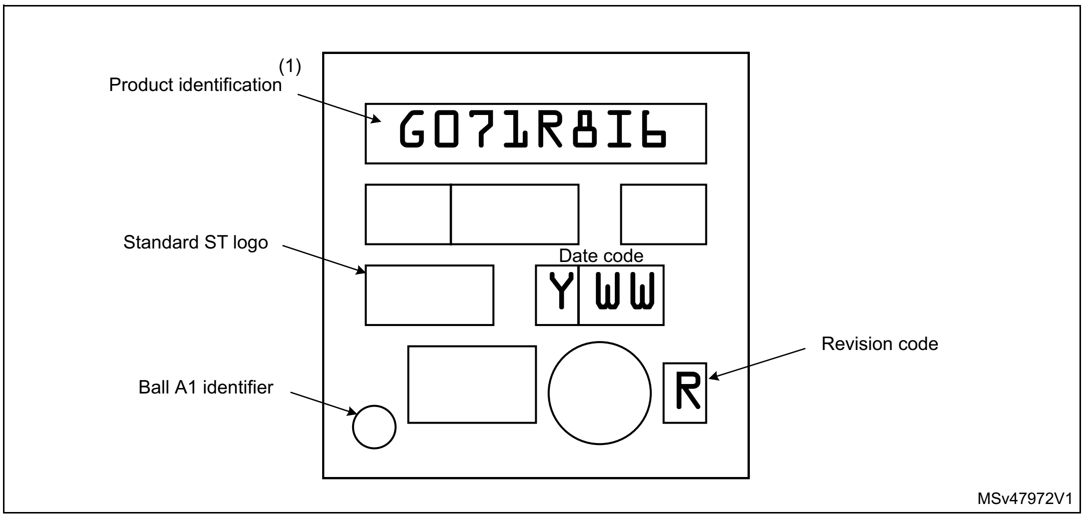
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 37. UFBGA64 package marking example

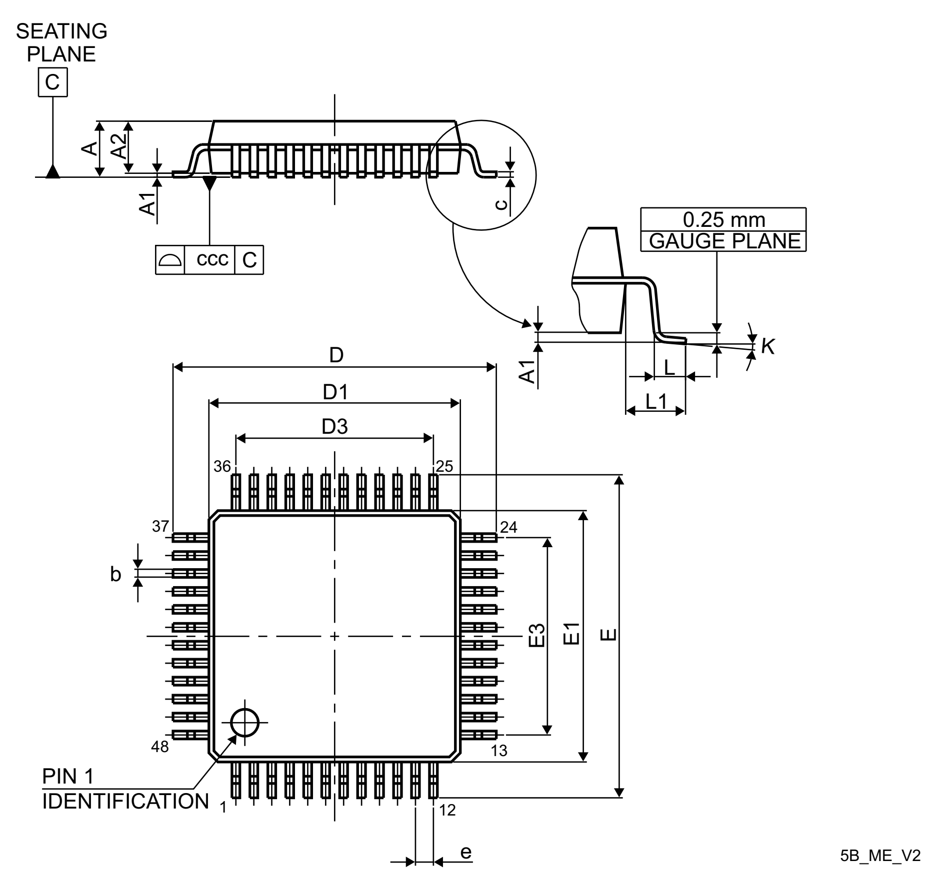


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.3 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

Figure 38. LQFP48 package outline



1. Drawing is not to scale.

Table 77. LQFP48 mechanical data

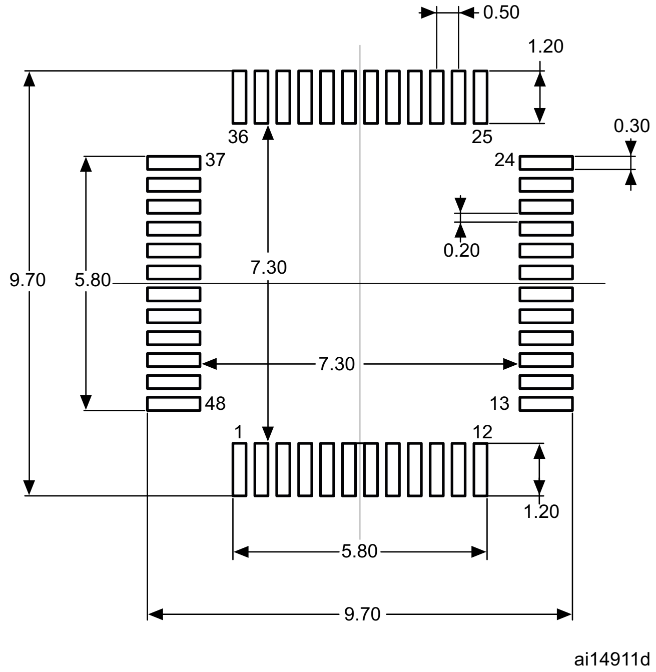
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-

Table 77. LQFP48 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. Recommended footprint for LQFP48 package



1. Dimensions are expressed in millimeters.

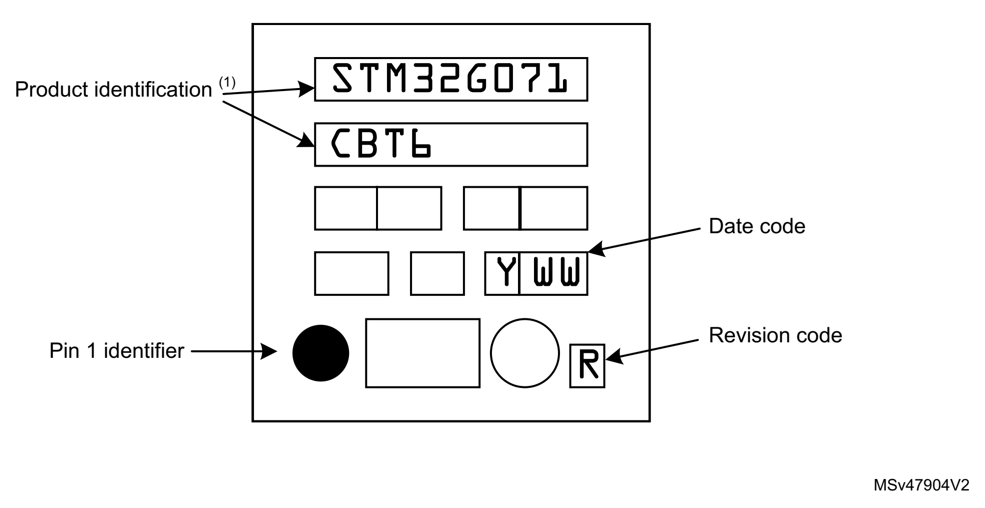
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 40. LQFP48 package marking example

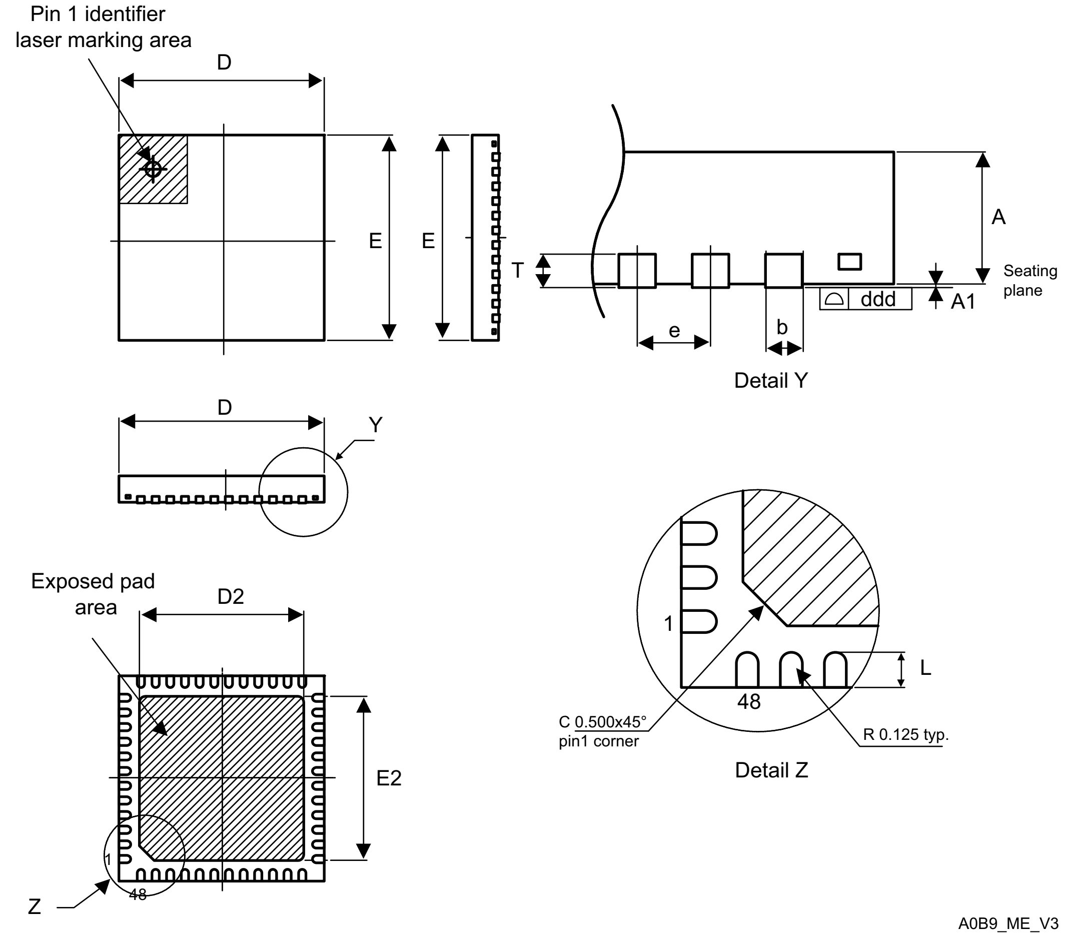


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.4 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package

Figure 41. UFQFPN48 package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 78. UFQFPN48 package mechanical data

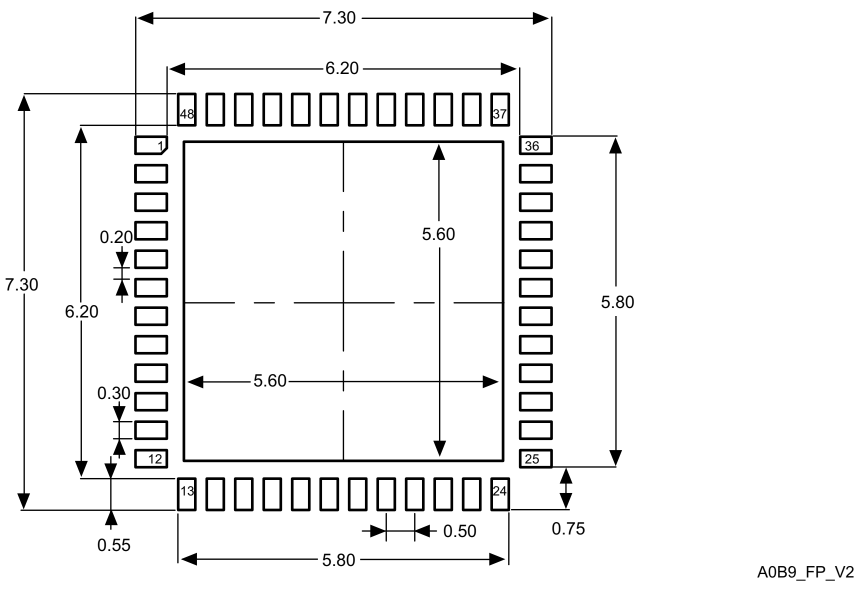
Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244

Table 78. UFQFPN48 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. Recommended footprint for UFQFPN48 package



1. Dimensions are expressed in millimeters.

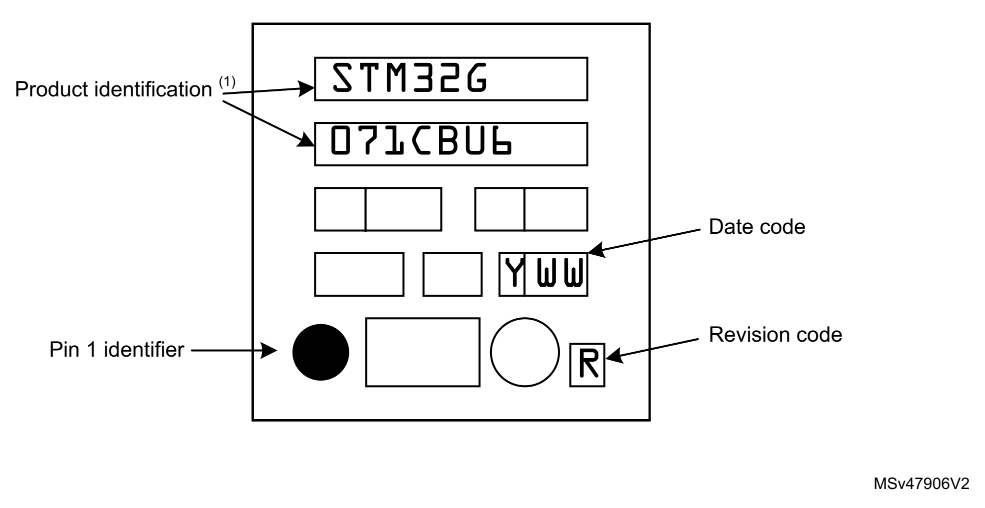
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 43. UFQFPN48 package marking example

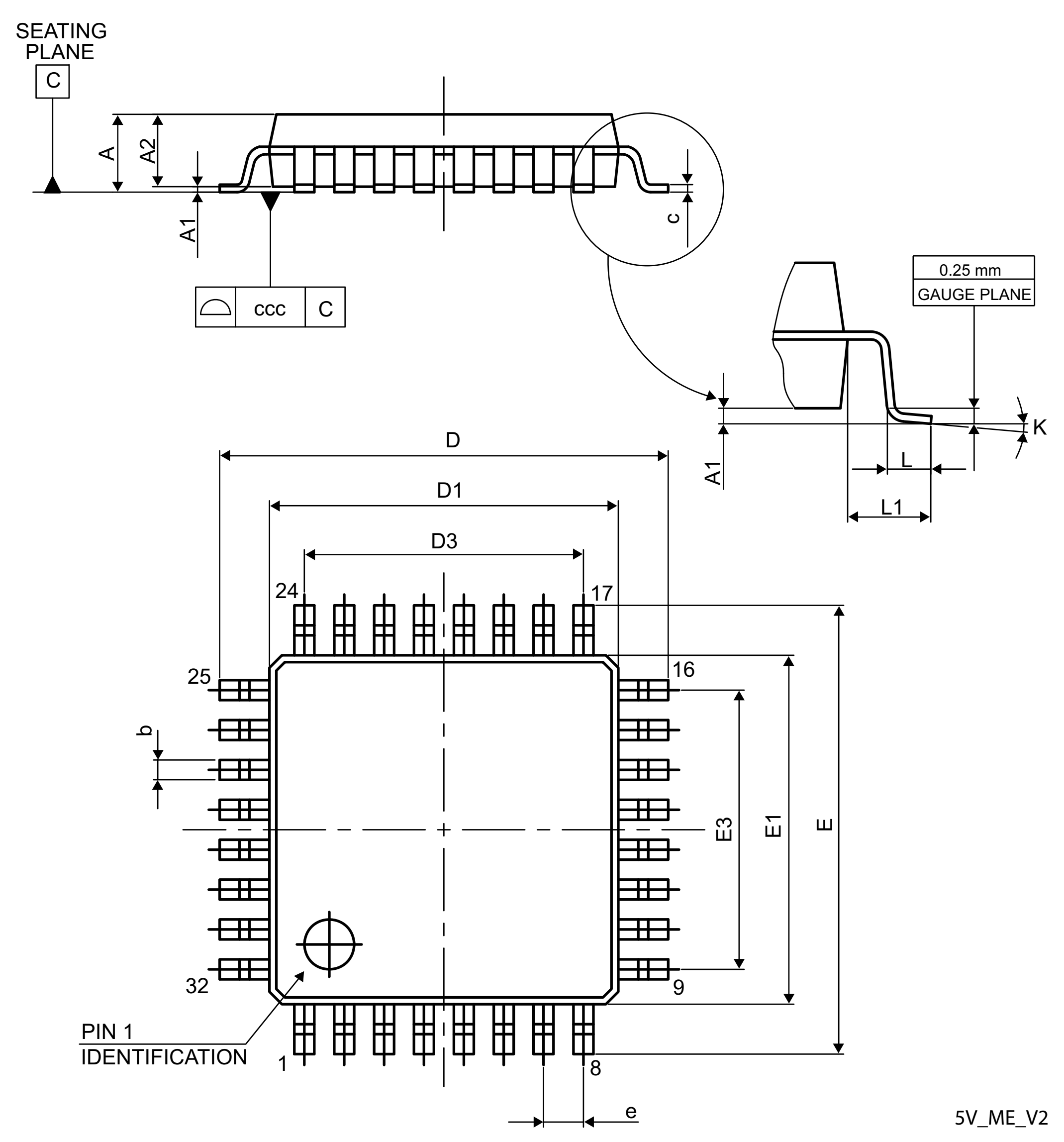


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.5 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7 mm low-profile quad flat package.

Figure 44. LQFP32 package outline



1. Drawing is not to scale.

Table 79. LQFP32 mechanical data

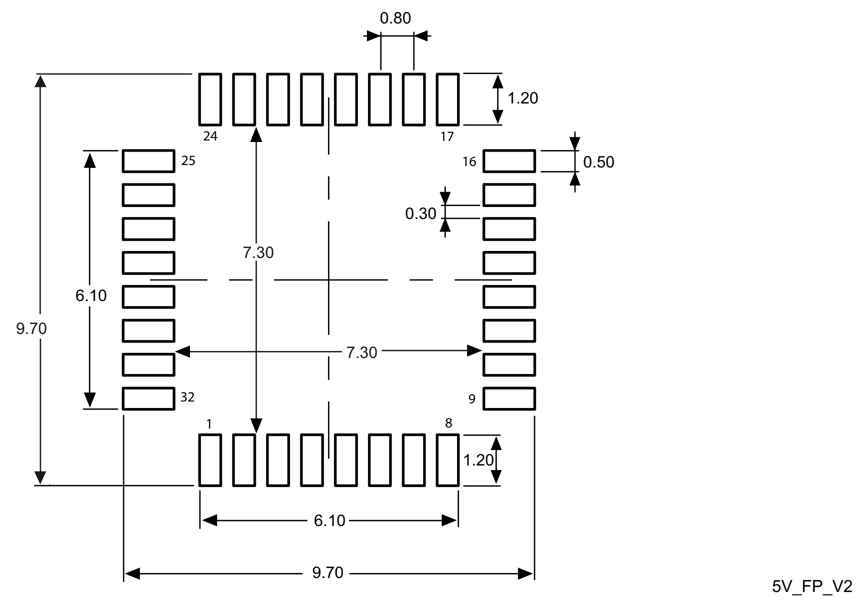
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 79. LQFP32 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. Recommended footprint for LQFP32 package



1. Dimensions are expressed in millimeters.

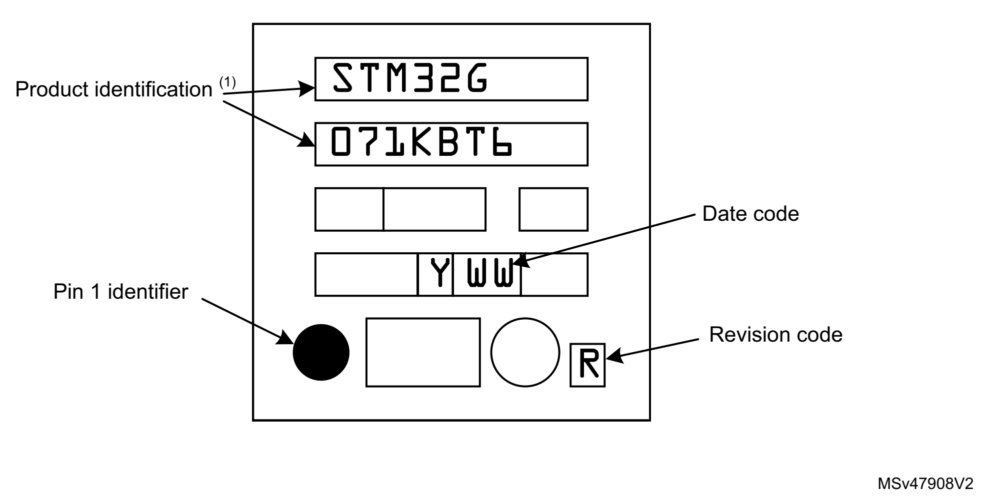
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 46. LQFP32 package marking example

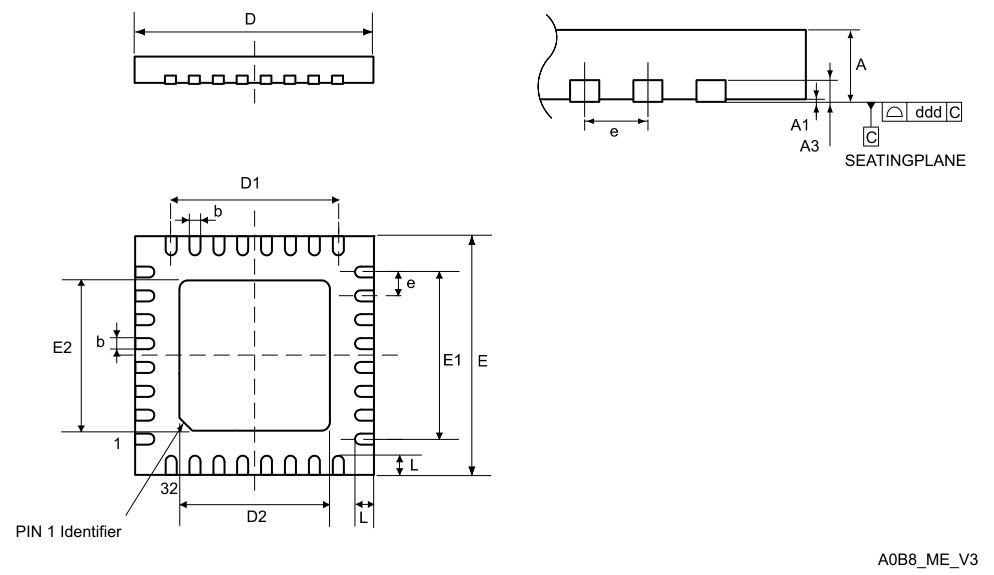


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.6 UFQFPN32 package information

UFQFPN32 is a 32-pin, 5x5 mm, 0.5 mm pitch ultra-thin fine-pitch quad flat package.

Figure 47. UFQFPN32 package outline



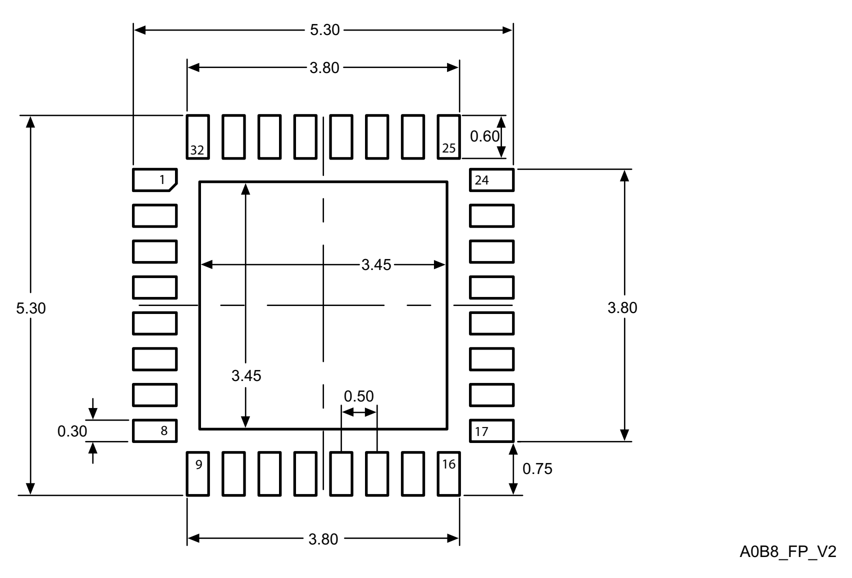
1. Drawing is not to scale.
2. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.

Table 80. UFQFPN32 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	-	0.050	-	-	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. Recommended footprint for UFQFPN32 package



1. Dimensions are expressed in millimeters

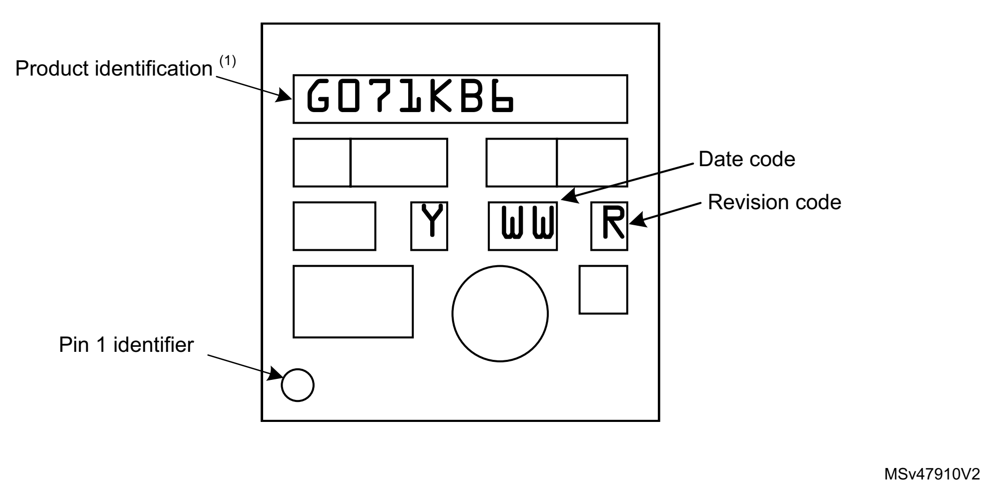
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 49. UFQFPN32 package marking example



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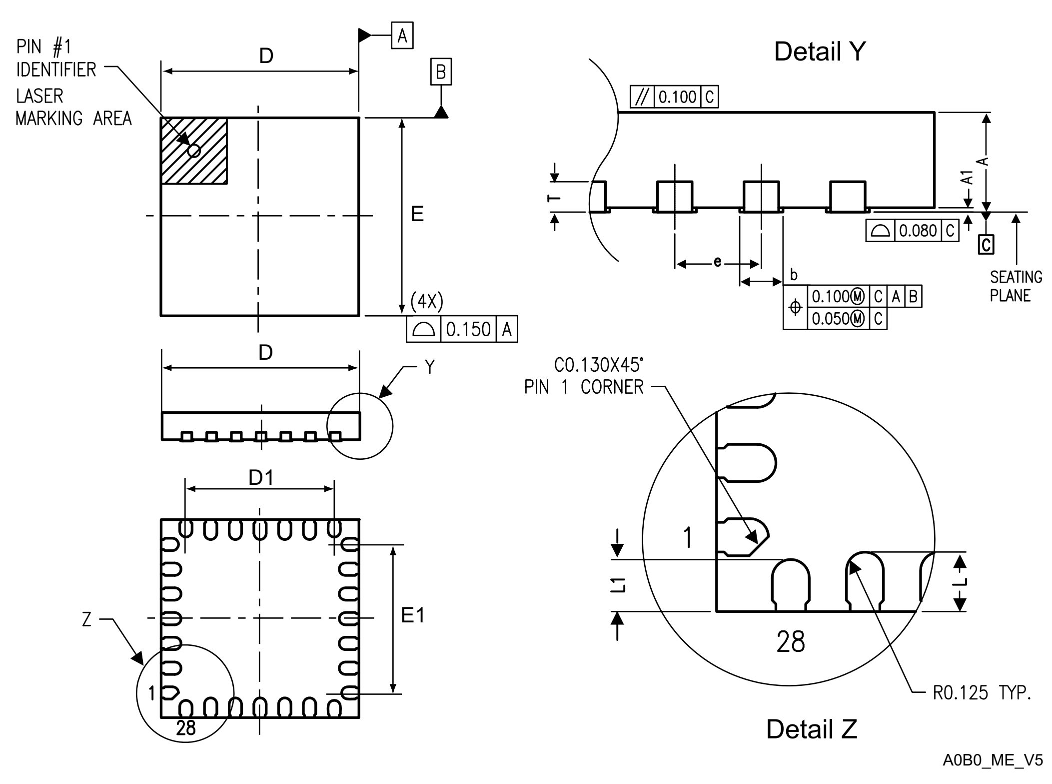
6.7 UFQFPN28 package information

UFQFPN is a 28-lead, 4x4 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 50. UFQFPN28 package outline



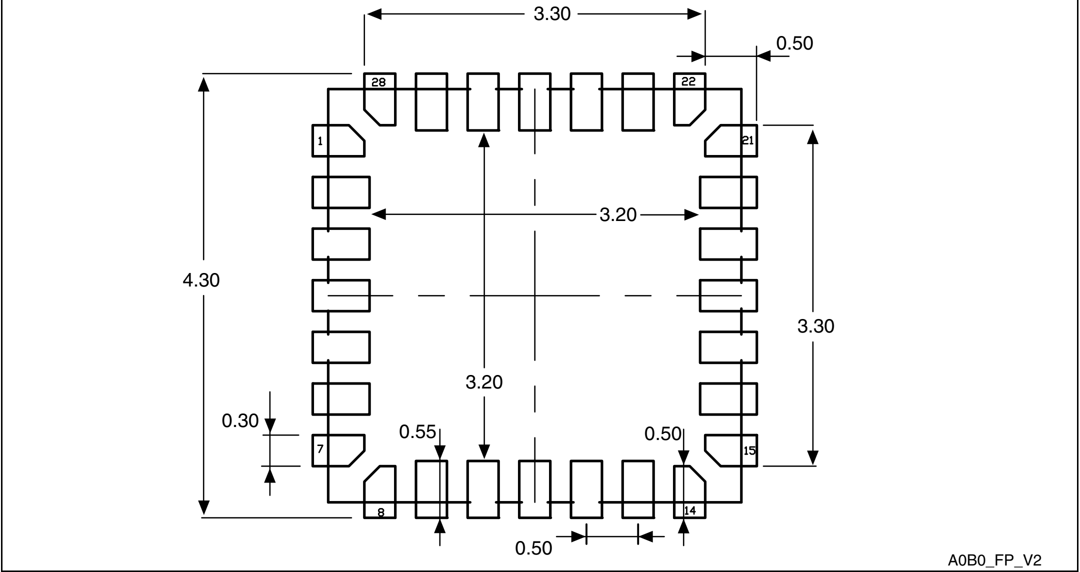
1. Drawing is not to scale.

Table 81. UFQFPN28 package mechanical data[(1)]

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 51. Recommended footprint for UFQFPN28 package



1. Dimensions are expressed in millimeters.

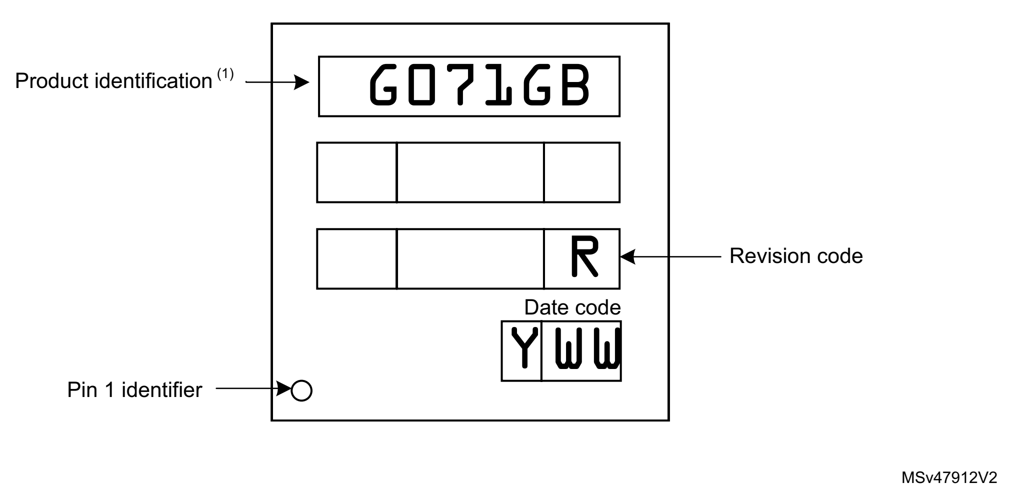
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 52. UFQFPN28 package marking example



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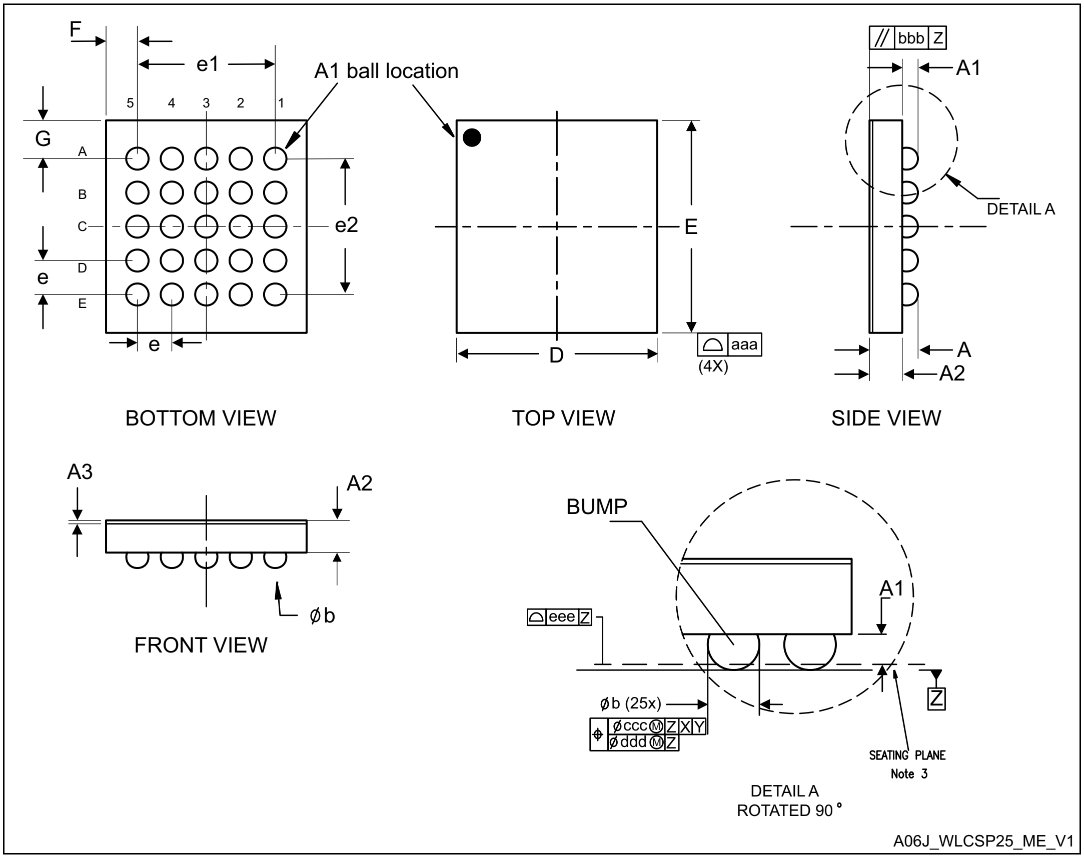
6.8 WLCSP25 package information

Figure 53. WLCSP25 chip-scale package outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 82. WLCSP25 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025[3]	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	2.28	2.30	2.32	0.090	0.091	0.091
E	2.46	2.48	2.50	0.097	0.098	0.098
e	-	0.40	-	-	0.016	-
e1	-	1.60	-	-	0.063	-

Table 82. WLCSP25 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e2	-	1.60	-	-	0.063	-
F[4]	-	0.350	-	-	0.014	-
G[4]	-	0.440	-	-	0.017	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 3 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal values and tolerances of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Calculated dimensions are rounded to the 3rd decimal place

Figure 54. Recommended PCB pad design for WLCSP25 package

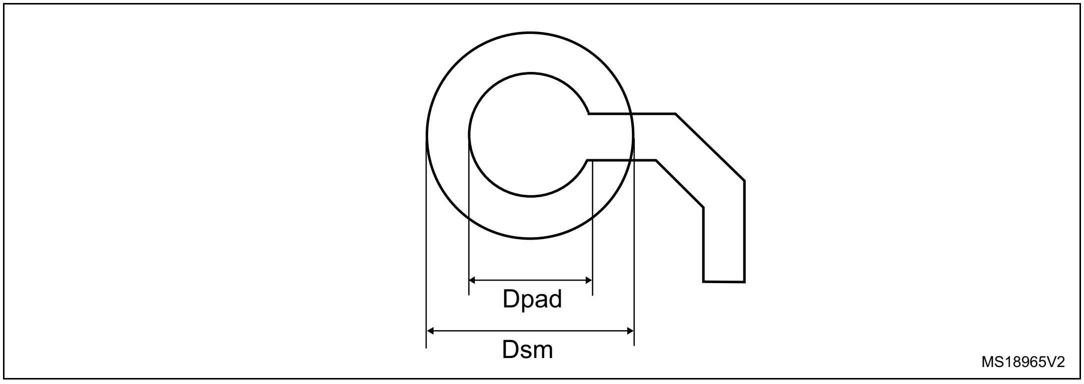


Table 83. Recommended PCB pad design rules for WLCSP25 package

Dimension	Recommended value (mm)
Pitch	0.4
Dpad	225
Dsm	0.290 typ.[1]
Stencil opening	0.250
Stencil thickness	0.100

1. Depends on the solder mask registration tolerance

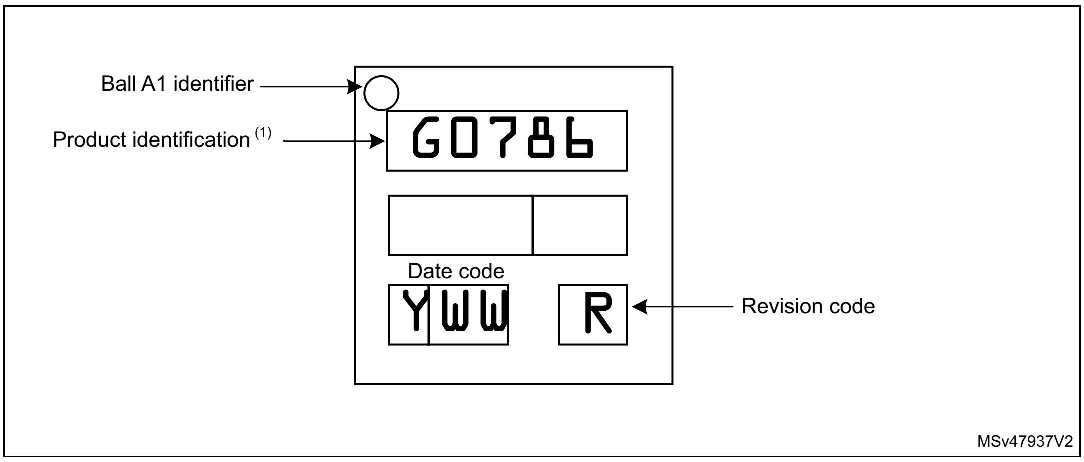
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks that identify the parts throughout supply chain operations, are not indicated below.

Figure 55. WLCSP25 package marking example



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6.9 Thermal characteristics

The operating junction temperature T_J must never exceed the maximum given in *Table 21: General operating conditions*.

The maximum junction temperature in °C that the device can reach if respecting the operating conditions, is:

$$T_J(max) = T_A(max) + P_D(max) \times \Theta_{JA}$$

where:

- $T_A(max)$ is the maximum operating ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D = P_{INT} + P_{I/O}$,
  - P_{INT} is power dissipation contribution from product of I_{DD} and V_{DD}
  - $P_{I/O}$ is power dissipation contribution from output ports where:
    $P_{I/O} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIO1} - V_{OH}) \times I_{OH})$,
    taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 84. Package thermal characteristics

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	LQFP64 10 × 10 mm	65	°C/W
		UFBGA64 5 × 5 mm	74	
		LQFP48 7 × 7 mm	75	
		UFQFPN48 7 × 7 mm	30	
		LQFP32 7 × 7 mm	76	
		UFQFPN32 5 × 5 mm	34	
		UFQFPN28 4 × 4 mm	44	
		WLCSP25 2.3 × 2.5 mm	70	

6.9.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (still air). Available from www.jedec.org.

6.9.2 Selecting the product temperature range

The temperature range is specified in the ordering information scheme shown in *Section 7: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and to a specific maximum junction temperature.

As applications do not commonly use microcontrollers at their maximum power consumption, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range best suits the application.

The following example shows how to calculate the temperature range needed for a given application.

Example:

Assuming the following worst application conditions:

- ambient temperature T_A = 50 °C (measured according to JESD51-2)
- I_{DD} = 50 mA; V_{DD} = 3.6 V
- 20 I/Os simultaneously used as output at low level with I_{OL} = 8 mA (V_{OL}= 0.4 V), and
- 8 I/Os simultaneously used as output at low level with I_{OL} = 20 mA (V_{OL}= 1.3 V),

the power consumption from power supply P_{INT} is:

P_{INT} = 50 mA × 3.6 V= 118 mW,

the power loss through I/Os P_{IO} is

P_{IO} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW,

and the total power P_D to dissipate is:

$P_{D\,=}$ 180 mW + 272 mW = 452 mW

For product in LQFP48 with Θ_{JA}= 75°C/W, the junction temperature stabilizes at:

T_J = 50°C + (75°C/W × 452 mW) = 50 °C + 33.9 °C = 83.9°C

As a conclusion, product version with suffix 6 (maximum allowed T_J = 105° C) is sufficient for this application.

If the same application was used in a hot environment with maximum T_A greater than 71°C, the junction temperature would exceed 105°C and the product version allowing higher maximum T_J would have to be ordered.

7 Ordering information

Example STM32 G 071 K 8 T 6 xyy

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

G = general-purpose

Device subfamily

071 = STM32G071

Pin count

E = 25
G = 28
K = 32
C = 48
R = 64

Flash memory size

8 = 64 Kbytes
B = 128 Kbytes

Package type

I = UFBGA
T = LQFP
U = UFQFPN
Y = WLCSP

Temperature range

6 = -40 to 85°C (105°C junction)
7 = -40 to 105°C (125°C junction)
3 = -40 to 125°C (130°C junction)

Options

xTR = tape and reel packing; x = N (PD product version) or blank
x␣␣ = tray packing; x = N (PD product version) or blank
other = 3-character ID incl. custom Flash code and packing information; x = N for PD product version

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 85. Document revision history

Date	Revision	Changes
8-Nov-2018	1	Initial release.
28-Nov-2018	2	*Table 19*: $I_{INJ(PIN)}$ parameter definition modified; *Table 21*: V_{IN} parameter definition modified; *Table 51*: FT_d type added to I_{lkg} parameter specification, note attached to I_{lkg} values, and TT_xx modified to TT_a; *Table 56*: “single ended mode” removed from $I_{DDV(ADC)}$ parameter definition; *Table 84*: UFBGA64 5x5 mm package Θ_{JA} corrected
06-Mar-2020	3	Cover page updated; *Section 2: Description* updated; *Section 3.3.1: Securable area* added; *Section 3.7.1: Power supply schemes*: corrected minimum VDD and VDDA values; *Section 3.14.1: Temperature sensor*: “engineering bytes” replaced “System memory”; *Section 3.20: Inter-integrated circuit interface (I^2C)*: SMBus and PMBus feature points; *Section 3.21: Universal synchronous/asynchronous receiver transmitter (USART)*: max. speed corrected; *Table 12*: Note 3 inserted and note 4 modified; *Table 18* updated; *Table 19*: Note 2 removed; *Table 21*: Redefined V_{IN} for I/Os of other than TT_xx and FT_c type; *Table 49*: LU class modified from “II” to “II Level A”; *Table 52*: I/O current condition for relaxed V_{OL}/V_{OH} corrected from 18 mA to 15 mA; section *Output driving current* corrected accordingly; *Table 56*: major update; *Section 3.12: DMA request multiplexer (DMAMUX)* added; Figures with package marking examples corrected.

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