



Automotive-grade N-channel 40 V, 6.1 mΩ typ., 18 A STripFET™V Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

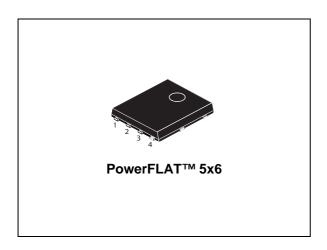
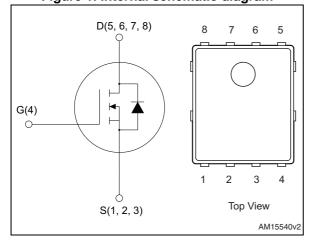


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)max}	I _D
STL70N4LLF5	40 V	$6.7~\mathrm{m}\Omega$	18 A

- Designed for automotive applications and AEC-Q101 qualified
- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Applications

· Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to a FOM that is among the best in its class.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL70N4LLF5	70N4LLF5	PowerFLAT™ 5x6	Tape and reel

Contents STL70N4LLF5

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Packaging mechanical data13	3
6	Revision history15	5

STL70N4LLF5 Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	40	V
V _{GS}	Gate-source voltage	± 22	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	70	А
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	44	А
I _D ⁽²⁾	Drain current (continuous) at T _{pcb} = 25 °C	18	А
I _D ⁽²⁾	Drain current (continuous) at T _{pcb} =100 °C	11.5	А
I _{DM} ^{(2),(3)}	Drain current (pulsed)	72	Α
P _{TOT} (1)	Total dissipation at T _C = 25 °C	72	W
P _{TOT} (2)	Total dissipation at T _{pcb} = 25 °C	4.8	W
	Derating factor ⁽²⁾	0.03	W/°C
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

- 1. The value is rated according to $R_{\text{thj-c}}$.
- 2. The value is rated according to $R_{\mbox{\scriptsize thj-pcb.}}$
- 3. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	2.08	°C/W
R _{thj-pcb} (1)	Thermal resistance junction-pcb	31.3	°C/W

^{1.} When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec.

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I _{AV}	Not-repetitive avalanche current, (pulse width limited by Tj max)	9	Α
E _{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AV}$, $V_{DD} = 24$ V)	1090	mJ

Electrical characteristics STL70N4LLF5

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 250 μA	40			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 40 V, V _{DS} = 40 V,T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±22 V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1			V
R _{DS(on)}	Static drain-source on- resistance	V_{GS} = 10 V, I_{D} = 9 A V_{GS} = 4.5 V, I_{D} = 9 A		6.1 7.6	6.7 9	mΩ

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	1570	-	pF
C _{oss}	Output capacitance	V _{DS} = 25 V, f=1 MHz,	-	257	-	pF
C _{rss}	Reverse transfer capacitance	V _{GS} =0	-	32	-	pF
Qg	Total gate charge	V _{DD} =15 V, I _D = 18 A	-	12.9	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 4.5 V	-	3.9	-	nC
Q _{gd}	Gate-drain charge	(Figure 14)	-	5.3	-	nC
R _G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20 mV I _D =0	-	1.5	-	W

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V 45.V 1 0 A	-	14	-	ns
t _r	Rise time	V _{DD} =15 V, I _D = 9 A, R _G =4.7 Ω, V _{GS} =10 V	-	42	-	ns
t _{d(off)}	Turn-off delay time	(Figure 13)	-	37	-	ns
t _f	Fall time	(1.3-1.1.)	-	5.2	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		18	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		72	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 18 A, V _{GS} =0	-		1.1	V
t _{rr}	Reverse recovery time	I _{SD} = 18 A,	-	27.2		ns
Q _{rr}	Reverse recovery charge	di/dt = 100 A/μs,	-	24.5		nC
I _{RRM}	Reverse recovery current	V _{DD} = 25 V, T _J =150 °C	-	1.8		А

- 1. Pulse width limited by safe operating area.
- 2. Pulsed: pulse duration=300 μ s, duty cycle 1.5%

Electrical characteristics STL70N4LLF5

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

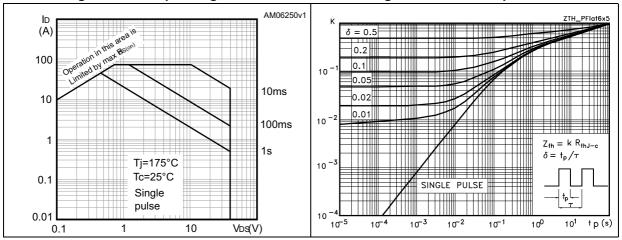


Figure 4. Output characteristics

Figure 5. Transfer characteristics

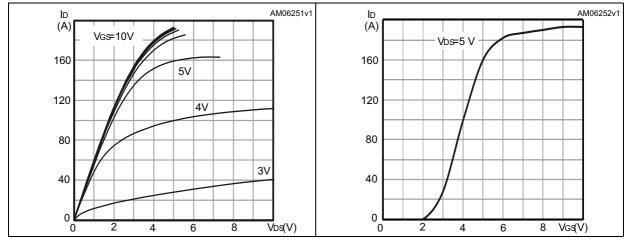


Figure 6. Normalized B_{VDSS} vs temperature

Figure 7. Static drain-source on-resistance

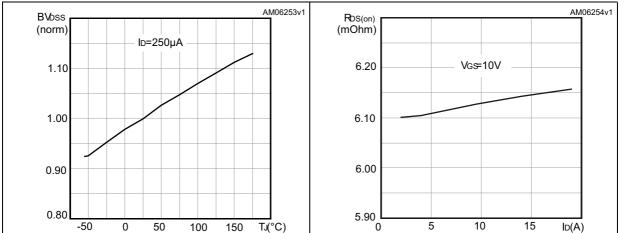


Figure 8. Gate charge vs gate-source voltage

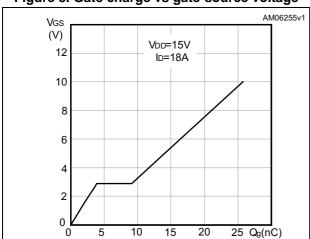


Figure 9. Capacitance variations

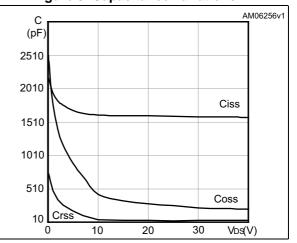
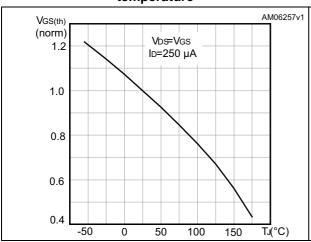


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on-resistance vs temperature



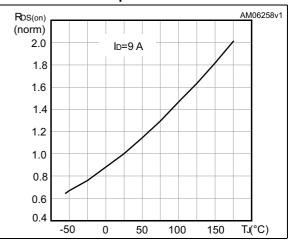
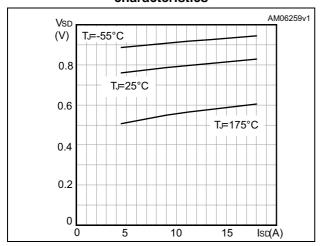


Figure 12. Source-drain diode forward characteristics



Test circuits STL70N4LLF5

3 Test circuits

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

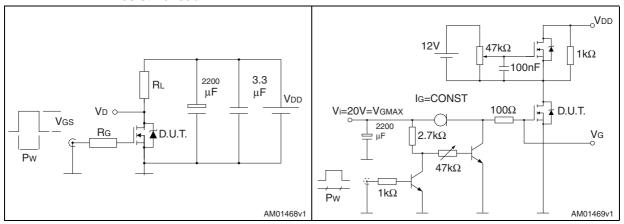


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

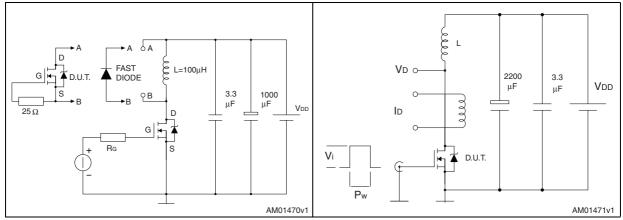
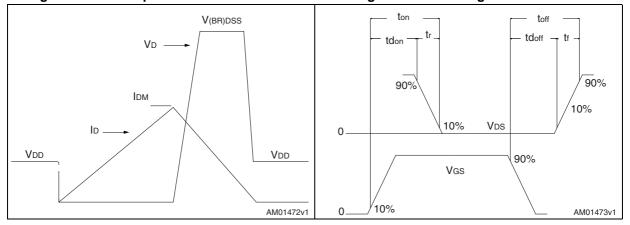


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



47/

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.



Table 9. PowerFLAT™ 5x6 type S-C mechanical data

Dim.		mm	
Diiii.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
е		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

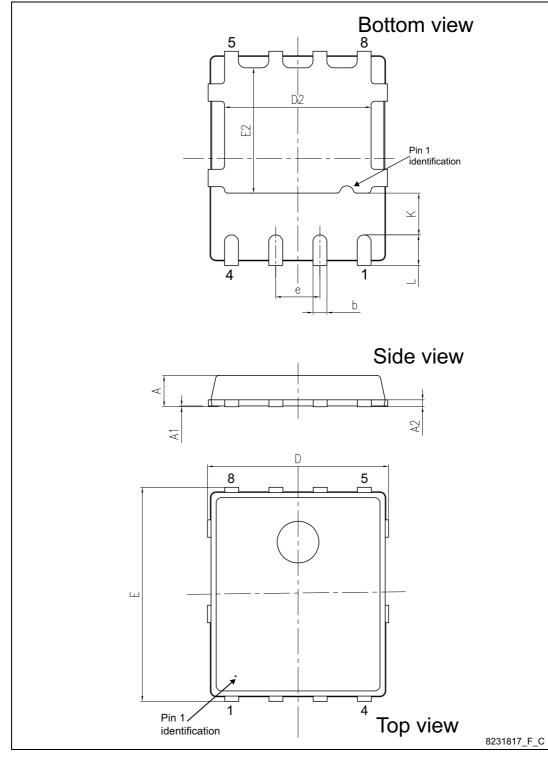


Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

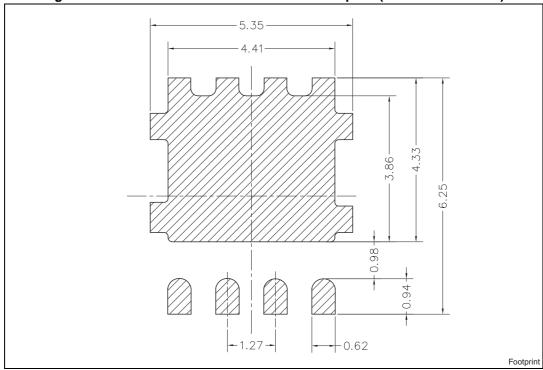


Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)

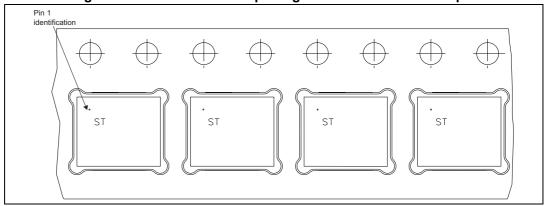
12/16 DocID15229 Rev 6

Packaging mechanical data 5

P₂ 2.0±0.1 (I) P₀ 4.0±0.1 (II) T (0.30±0.05) E₁ -- 1.75±0.1 Do Ø1.55±0.05 F(5.50±0.1)(III) P1(8.00±0.1) Ko (1.20±0.1) SECTION Y-Y (I) Measured from centerline of sprocket hole to centerline of pocket. Base and bulk quantity 3000 pcs (II) Cumulative tolerance of 10 sprocket holes is $\pm\ 0.20$. (III) Measured from centerline of sprocket hole to centerline of pocket.

Figure 21. PowerFLAT™ 5x6 tape^(a)

Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.



8234350_Tape_rev_C

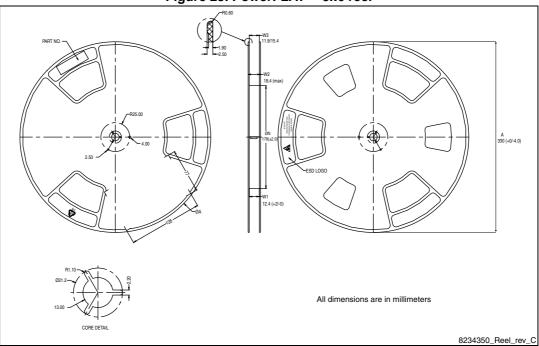


Figure 23. PowerFLAT™ 5x6 reel

14/16 DocID15229 Rev 6

STL70N4LLF5 Revision history

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Dec-2008	1	First release
18-Jul-2011	2	Section 4: Package mechanical data has been modified: - Added Table 9: PowerFLAT TM 5x6 type S-C mechanical data - Added Figure 19: PowerFLAT TM 5x6 type S-C mechanical data - Added PowerFLAT TM 5x6 type C-B mechanical data - Added PowerFLAT TM 5x6 type C-B drawing - Minor text changes.
21-Dec-2011	3	Section 4: Package mechanical data has been modified.
25-Jan-2013	4	 Table 1: Device summary has been updated. Minor text changes. Changed: Figure 1 Added: Section 5: Packaging mechanical data
12-Feb-2013	5	 Updated T_J and T_{stg} in Table 2: Absolute maximum ratings. Updated Section 4: Package mechanical data and Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape
24-May-2013	6	Modified: title and Section 4: Package mechanical data Minor text changes

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16/16 DocID15229 Rev 6

