Octal 3-State Inverting Buffer/Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

The MC74HC240A is identical in pinout to the LS240. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

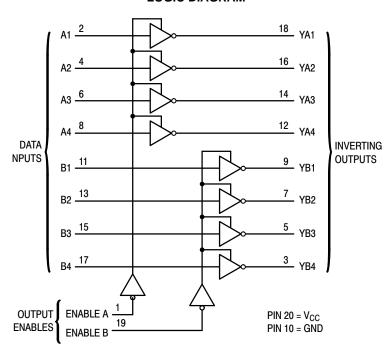
This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other sub-oriented systems. The device has inverting outputs and two active-low output enables.

The HC240A is similar in function to the HC244A.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 120 FETs or 30 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

LOGIC DIAGRAM





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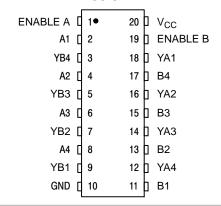
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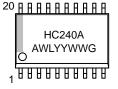


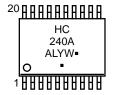
SOIC-20 DW SUFFIX CASE 751D TSSOP-20 DT SUFFIX CASE 948E

PIN ASSIGNMENT



MARKING DIAGRAMS





SOIC-20

TSSOP-20

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or • = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inpu	Outputs				
Enable A, Enable B	A, B	YA, YB			
L	L	Н			
L	Н	L			
H	X	Z			

Z = high impedance

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
l _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C

TSSOP Package: -6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time $V_{CC} = 2.0 \text{ V}$ (Figure 1) $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gu	aranteed Li	mit	
Symbol	Parameter	Test Conditions	V _{CC} V	–55 to 25°C	≤ 85°C	≤ 125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$	2.0	1.5	1.5	1.5	V
		$ I_{out} \le 20 \mu\text{A}$	3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V	2.0	0.5	0.5	0.5	V
		$ I_{out} \le 20 \mu\text{A}$	3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V_{OH}	Minimum High-Level Output	$V_{in} = V_{IH}$	2.0	1.9	1.9	1.9	V
	Voltage	$ I_{out} \le 20 \mu\text{A}$	4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$ $ I_{out} \le 2.4 \text{ mA}$	3.0	2.48	2.34	2.2	
		$ I_{out} \leq 6.0 \text{ mA}$	4.5	3.98	3.84	3.7	
		$ I_{out} \le 7.8 \text{ mA}$	6.0	5.48	5.34	5.2	
V_{OL}	Maximum Low–Level Output	$V_{in} = V_{IL}$	2.0	0.1	0.1	0.1	V
	Voltage	$ I_{out} \le 20 \mu\text{A}$	4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IL}$ $ I_{out} \le 2.4 \text{ mA}$	3.0	0.26	0.33	0.4	
		$ I_{out} \leq 6.0 \text{ mA}$	4.5	0.26	0.33	0.4	
		$ I_{out} \le 7.8 \text{ mA}$	6.0	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μΑ
I_{OZ}	Maximum Three–State Leakage	Output in High-Impedance State	6.0	± 0.5	± 5.0	± 10	μΑ
	Current	$V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$					
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	4.0	40	160	μΑ

AC ELECTRICAL CHARACTERISTICS (C $_L$ = 50 pF, Input $t_{\rm f}$ = $t_{\rm f}$ = 6 ns)

			Gu			
Symbol	Parameter	v _{cc} v	–55 to 25°C	≤ 85°C	≤ 125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0 3.0 4.5 6.0	80 40 16 14	100 50 20 17	120 60 24 20	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 60 22 19	140 70 28 24	165 80 33 28	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 60 22 19	140 70 28 24	165 80 33 28	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 32 18 15	ns
C _{in}	Maximum Input Capacitance	-	10	10	10	pF
C _{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	-	15	15	15	pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Transceiver Channel)*	32	pF

^{*}Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

SWITCHING WAVEFORMS

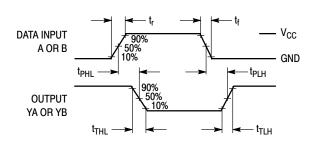


Figure 1.

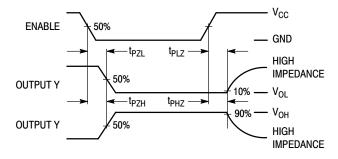
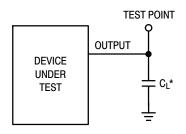
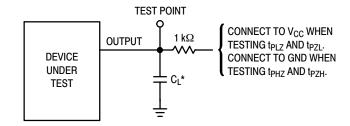


Figure 2.



*Includes all probe and jig capacitance

Figure 3. Test Circuit



*Includes all probe and jig capacitance

Figure 4. Test Circuit

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4 (Pins 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

Enable A, Enable B (Pins 1, 19)

Output enables (active-low). When a low level is applied to these pins, the outputs are enabled and the devices

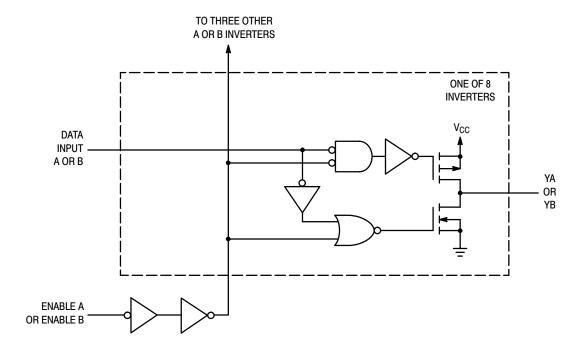
function as inverters. When a high level is applied, the outputs assume the high-impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (Pins 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output-enable pins, these outputs are either inverting outputs or high-impedance outputs.

LOGIC DETAIL



ORDERING INFORMATION

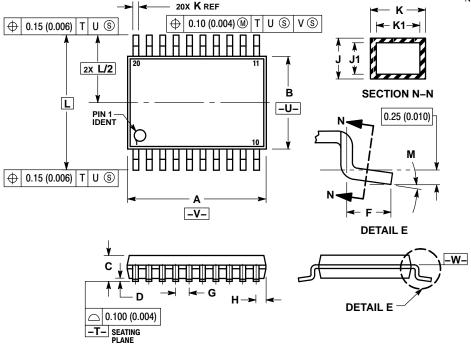
Device	Package	Shipping [†]
MC74HC240ADWG	SOIC-20 WIDE (Pb-Free)	38 Units / Rail
NVL74HC240ADWG*	SOIC-20 WIDE (Pb-Free)	38 Units / Rail
MC74HC240ADWR2G	SOIC-20 WIDE (Pb-Free)	1000 Tape & Reel
NVL74HC240ADWR2G*	SOIC-20 WIDE (Pb-Free)	1000 Tape & Reel
MC74HC240ADTR2G	TSSOP-20 (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

PACKAGE DIMENSIONS

TSSOP-20 **DT SUFFIX** CASE 948E-02 ISSUE C



- NOTES:

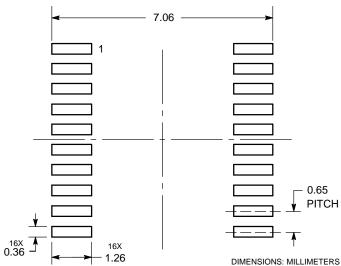
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION.

 - INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION.
 SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE
 DAMBAR PROTRUSION. ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.08
 (0.003) TOTAL IN EXCESS OF THE K
 DIMENSION AT MAXIMUM MATERIAL
 CONDITION.

 - CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	6.40	6.60	0.252	0.260
В	4.30	4.50	0.169	0.177
С	-	1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	0.65 BSC		BSC
Н	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40		0.252 BSC	
M	0°	8°	0°	8°

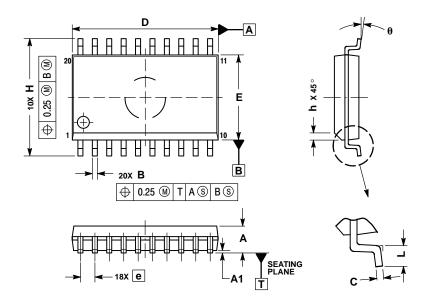
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOIC-20 DW SUFFIX CASE 751D-05 ISSUE G



NOTES:

- DIMENSIONS ARE IN MILLIMETERS.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M. 1994.
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- MAXIMUM MIGLE PROTROSION 1.13 FER 3184
 PROTRUSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS			
DIM	MIN	MAX		
Α	2.35	2.65		
A1	0.10	0.25		
В	0.35	0.49		
C	0.23	0.32		
D	12.65	12.95		
Е	7.40	7.60		
е	1.27	BSC		
Н	10.05	10.55		
h	0.25	0.75		
L	0.50	0.90		
θ	0 °	7 °		

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