19-0205; Rev 0; 7/94

EVALUATION KIT AVAILABLE

PDA/Hand-Held Computer Power Controller

General Description

The MAX781 is a system-engineered power-supply controller for subnotebook computers, PDAs, or similar battery-powered equipment. It provides high-performance, step-down (buck), pulse-width modulated (PWM) control for generating +3.3V and constant-current battery charging. Dual PCMCIA VPP outputs are powered by a regulated flyback winding. Five high-side gate drivers and a buffered analog multiplexer are also included. All functions are controlled by an SPI/Microwire™ compatible four-wire serial interface.

The MAX781 generates +3.3V with high efficiency through synchronous rectification and PWM operation at heavy loads. It uses Idle Mode™ operation at light loads. Only small external components are required because of the device's high switching frequency (300kHz) and advanced current-mode PWM architecture that allows for output capacitance as low as 50µF per ampere of load.

The MAX781 is configured by 32 bits of serial data. These bits select the operating mode, set the switch-mode battery charger current level, select one of eight analog multiplexer channels, and turn on/off the five high-side gate drivers. A status byte read from the serial interface indicates if the battery has been removed, if the DC charging source has been connected, or if there is a fault condition on the +3.3V output. An interrupt output signals the CPU if a status signal changes.

Features

- **+3.3V Step-Down Controller**
- **Dual PCMCIA 2.0 Compatible VPP Outputs (0V/3.3V/5V/12V)**
- **Digitally Adjustable Switching Current Source for Battery Charging**
- **5 High-Side Switch Gate-Driver Outputs**
- **SPI Serial Interface**
- **300kHz Switching Frequency**
- **Oscillator SYNC Input**
- **2.5V ±1.5% Reference Output**
- **36-Pin SSOP Package**

Applications

Subnotebook Computers

PDAs

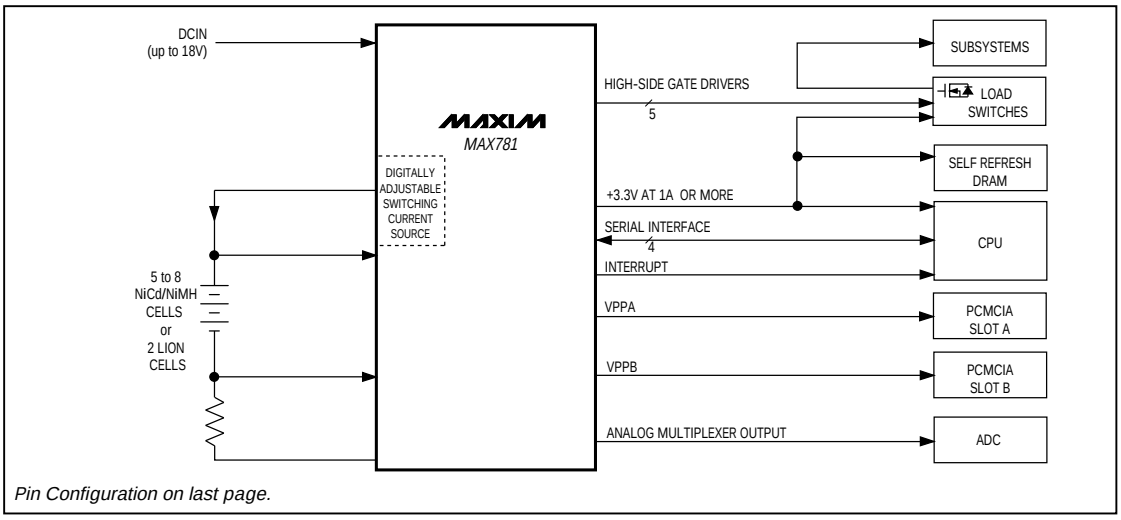
Communicating Computers

Handy-Terminals

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX781CBX	0°C to +70°C	36 SSOP
MAX781EBX	-40°C to +85°C	36 SSOP

Typical Application Diagram



Pin Configuration on last page.

™SPI is a trademark of Motorola Inc. Microwire is a trademark of National Semiconductor Corp.
Idle Mode is a trademark of Maxim Integrated Porducts.

ABSOLUTE MAXIMUM RATINGS

BATT, VCHG, VHI to AGND .....-0.3V, 20V
VPPA, VPPB to AGND .....-0.3V, 20V
FAST, GD1, GD2, GD3, GD4, GD5 to AGND .....-0.3V, 20V
BST to AGND .....-0.3V, 30V
BST to LX .....-0.3V, 7V
DHI to LX .....-0.3V, (BST + 0.3V)
PGND to AGND .....-0.3V, +0.3V
All Other Pins to AGND or PGND .....-0.3V, 7V
VPPA, VPPB Current 100mA
5OUT Current 100mA
3OUT Current 40mA
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 11.76mW/°C above +70°C) 941mW
Operating Temperature Ranges
MAX781CBX .....0°C to +70°C
MAX781EBX .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(BATT = 6V, power-on reset state, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE					
BATT Quiescent Supply Current	Shutdown mode, $\overline{SHDN}$ = 0V			10	µA
	Low-power mode, $\overline{SHDN}$ = BATT = 18V		60	120	
	Standby mode, $\overline{SHDN}$ = BATT = 18V		250	750	
	Operate mode, $\overline{SHDN}$ = BATT = 18V		1	2	mA
REF Output Voltage	No load	2.463	2.5	2.537	V
REF Load Regulation	I_{SOURCE} = -20µA to 100µA	-20		20	mV
5OUT Output Voltage	Operate or standby mode, 5.5V < BATT < 18V, 0mA < I_{5OUT} < 25mA	4.8		5.2	V
	Low-power mode, 5.5V < BATT < 18V, 0mA < I_{5OUT} < 10mA	4.8		5.2	
Internal Undervoltage Lockout Threshold (measured at 5OUT, UVLO = AGND)	V_{5OUT} rising	4.30	4.60	4.80	V
	V_{5OUT} falling	4.10	4.35	4.50	
UVLO Threshold (measured at UVLO)	V_{UVLO} rising	97		103	%REF
	V_{UVLO} falling	90		96	
UVLO Input Bias Current				50	nA
INTERNAL OSCILLATOR					
Internal Oscillator Frequency	SYNC = REF	270	300	340	kHz
	SYNC = AGND or 5OUT	170	230	260	
SYNC Capture Range (Note 1)		270		350	kHz
SYNC Minimum Pulse Width (Note1)		500			ns
SYNC Fall Time (Note 1)				200	ns
SYNC Rise Time (Note 1)				1	µs
SYNC Input Voltage Low				0.75	V
SYNC Input Voltage High		3.8			V
SYNC Leakage Current		-100		100	nA

ELECTRICAL CHARACTERISTICS (continued)

(BATT = 6V, power-on reset state, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V OUTPUT					
3OUT Output Voltage	Low-power mode, 4V < BATT < 18V, 0mA < I_{3OUT} < 1mA	3.17		3.43	V
	Standby mode, 4V < BATT < 18V, 0mA < I_{3OUT} < 10mA	3.17		3.43	
	Operate mode, 4V < BATT < 18V, CS to 3OUT = 0mV to 80mV	3.17		3.43	
CS to 3OUT Current-Limit Threshold		80	100	130	mV
3VINT Fault-Detect Threshold	3OUT falling	2.9	3.0	3.1	V
3VINT Fault-Detect Hysteresis			150		mV
DLO On-Resistance	High, 5OUT = 4.75V			15	Ω
	Low, 5OUT = 4.75V			10	
DHI On-Resistance	High or low, BST - LX = 4.5V			10	Ω
BATTINT Battery-Detect Threshold (measured at TEMP)	TEMP falling	75	81		%3OUT
	TEMP rising		83	89	
VPP REGULATOR					
VHI Regulation Threshold	Operate mode	12.8	13.5	14.2	V
VHI Clamp Voltage	Operate mode, I_{SINK} = 200µA, VPPA1 = VPPA0 = 0, VPPB1 = VPPB0 = 0, GDSEL1 to GDSEL5 = 0			20	V
VHI Clamp Current	VHI = 20V	1			mA
VHI Input Bias Current	Operate mode, VHI = 18V, VPPA1 = VPPA0 = 0, VPPB1 = VPPB0 = 0, GDSEL1 to GDSEL5 = 0			45	µA
VPP_Output Voltage	I_{SINK} = 1mA, VPP_1 = 0, VPP_0 = 0			0.25	V
	14.2V < VHI < 18V, VPP_1 = 0, VPP_0 = 1, 0mA < IVPP_ < 60mA	4.75	5.0	5.25	
	14.2V < VHI < 18V, VPP_1 = 1, VPP_0 = 0, 0mA < IVPP_ < 60mA	11.4	12.0	12.6	
	14.2V < VHI < 18V, VPP_1 = 1, VPP_0 = 1, 0mA < IVPP_ < 60mA	3.14	3.3	3.49	
HIGH-SIDE GATE DRIVERS					
GD_ Output High Voltage	VHI = 14.2V, GDSEL_ = 1, I_{SOURCE} = 1µA	14			V
GD_ Output Low Voltage	VHI = 14.2V, GDSEL_ = 0, I_{SINK} = 20µA			0.25	V
GD_ Source Current	GD_ = 2.5V, GDSEL_ = 1, VHI = 14.2V	6	10	18	µA
GD_ Sink Current	GD_ = 2.5V, GDSEL_ = 0, VHI = 14.2V	200	450	900	µA

ELECTRICAL CHARACTERISTICS (continued)

(BATT = 6V, power-on reset state, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER					
AOUT Output Voltage	MUX2 = 0, MUX1 = 0, MUX0 = 0	65.33	66.67	68.00	%3OUT
	MUX2 = 0, MUX1 = 0, MUX0 = 1	44.54	45.45	46.36	%5OUT
	MUX2 = 0, MUX1 = 1, MUX0 = 0	19.90	20.00	20.10	%BATT
	MUX2 = 0, MUX1 = 1, MUX0 = 1	65.33	66.67	68.00	%TEMP
	MUX2 = 1, MUX1 = 0, MUX0 = 0	18.49	18.87	19.25	%VPPA
	MUX2 = 1, MUX1 = 0, MUX0 = 1	18.49	18.87	19.25	%VPPB
	MUX2 = 1, MUX1 = 1, MUX0 = 0	99.8	100	100.2	%VREF
	MUX2 = 1, MUX1 = 1, MUX0 = 1	65.33	66.67	68.00	%AUXIN
AOUT Output Low	I_{SINK} = 10µA			10	mV
SERIAL INTERFACE					
CE, SCLK, DIN Logic Input High Voltage		2			V
CE, SCLK, DIN Logic Input Low Voltage				0.8	V
SCLK, DIN Leakage Current		-100		100	nA
CE Internal Pull-Down Resistance		60	100	140	kΩ
DOUT, INT Logic Output High Voltage	I_{SOURCE} = 1mA	2.7			V
DOUT, INT Logic Output Low Voltage	I_{SINK} = 1.6mA			0.4	V
CE, SCLK, DIN Logic Input Rise/Fall Time (Note 1)				50	ns
BATTERY CHARGER					
DCHG On Resistance	High or low, 5OUT = 4.75V			10	Ω
CSBAT Full-Scale Current-Sense Voltage	CHG6 to CHG0 = 1, CHARGE = 1	190	200	210	mV
COMP Current-Sense Amplifier Offset Voltage	CSBAT = 0V	-2	0	2	mV
Current-Sense Amplifier CSBAT to COMP Transconductance (gm)		400	600	750	µmho
FAST OUTPUT					
Output Sink Current	FAST = 3V, FASTON = 1	1.0	2.0		mA
	FAST = 18V, FASTON = 0			±1.0	nA

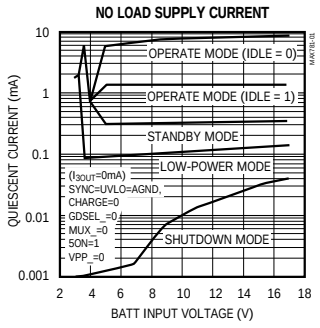
TIMING CHARACTERISTICS (Note 1)

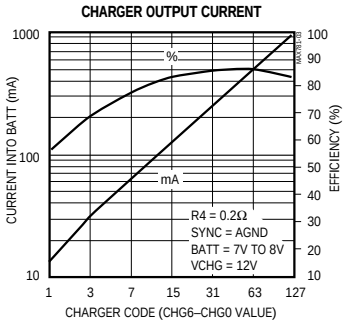
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DIN to SCLK Data Setup Time	t_{DS}	125			ns
DIN to SCLK Data Hold Time	t_{DH}	0			ns
SCLK to DOUT Valid Propagation Delay	t_{DO}	30		200	ns
SCLK Clock Period	t_{CP}	400			ns
SCLK High Pulse Width	t_{CH}	125			ns
SCLK Low Pulse Width	t_{CL}	125			ns
CE Assertion to DOUT Enable	t_{DV}			120	ns
CE Deassertion to DOUT Disable	t_{TR}			120	ns
CE Assertion to SCLK Rising-Edge Setup Time	t_{CSS}	200			ns
SCLK Rising Edge to CE Deassertion	t_{CSH}	200			ns
CE High Pulse Width	t_{CSW}	300			ns
SCLK Rising Edge to CE Assertion	t_{CS0}	200			ns
CE Deassertion to SCLK Rising Edge	t_{CS1}	200			ns

Note 1: Guaranteed by design.

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

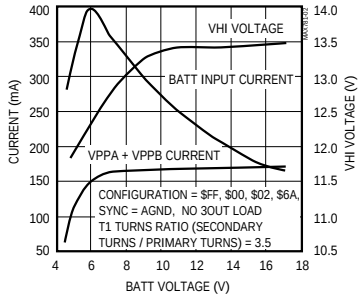




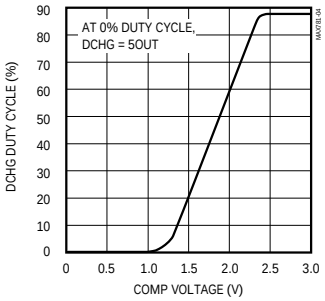
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

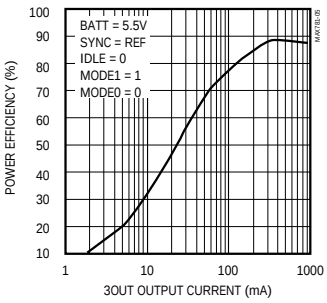
VPPA AND VPPB OUTPUT POWER VPPA SHORTED TO VPPB AND CLAMPED TO 11.5V



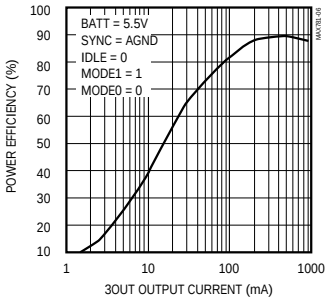
DCHG DUTY CYCLE vs. COMP VOLTAGE



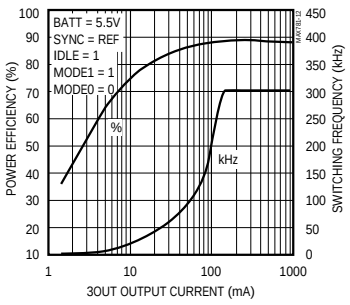
3OUT OPERATE MODE POWER EFFICIENCY (FIXED 300kHz SWITCHING FREQUENCY)



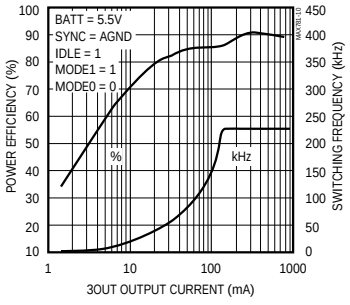
3OUT OPERATE MODE POWER EFFICIENCY (FIXED 230kHz SWITCHING FREQUENCY)



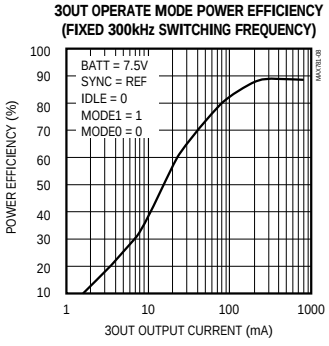
3OUT OPERATE MODE POWER EFFICIENCY (VARIABLE SWITCHING FREQUENCY)



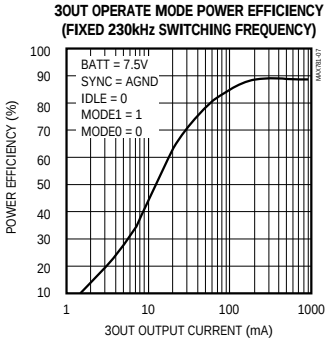
3OUT OPERATE MODE POWER EFFICIENCY (VARIABLE SWITCHING FREQUENCY)



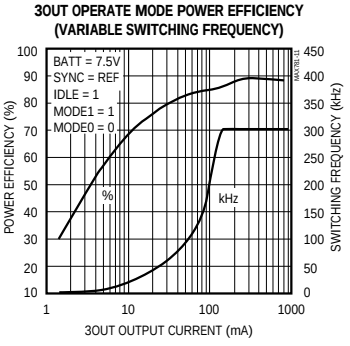
3OUT OPERATE MODE POWER EFFICIENCY (FIXED 300kHz SWITCHING FREQUENCY)



3OUT OPERATE MODE POWER EFFICIENCY (FIXED 230kHz SWITCHING FREQUENCY)



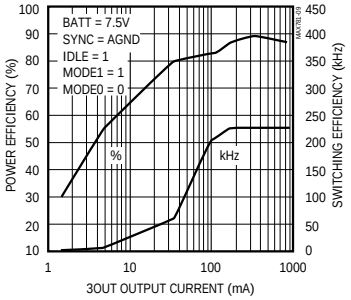
3OUT OPERATE MODE POWER EFFICIENCY (VARIABLE SWITCHING FREQUENCY)



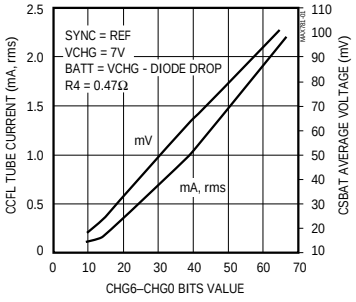
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

3OUT OPERATE MODE POWER EFFICIENCY VARIABLE SWITCHING FREQUENCY



USING THE BATTERY CHARGER TO DRIVE A CCFL BACKLIGHT ROYER OSCILLATOR



Pin Description

PIN	NAME	FUNCTION
1–4	GD2–GD5	High-Side Gate-Driver Outputs
5	VPPA	VPP-Programming Voltage Output A
6	VHI	VPPA, VPPB Linear-Regulator Input Power
7	VPPB	VPP-Programming Voltage Output B
8	AGND	Analog Ground
9	SYNC	Oscillator Frequency Control and Synchronization Input
10	CE	Serial-Interface Chip-Enable Input—active high
11	SCLK	Serial-Interface Clock Input
12	DOUT	Serial-Interface Data Output
13	DIN	Serial-Interface Data Input
14	INT	Interrupt Output
15	FAST	General-purpose open-drain output
16	COMP	Battery-Charger Compensation
17	CSBAT	Battery-Charger Current-Sense Input
18	5OUT	Linear-Regulated +5V Output
19	DCHG	Battery-Charger MOSFET Gate-Driver Output
20	PGND	Power Ground
21	DLO	+3.3V Regulator, Synchronous Rectifier, Gate-Driver Output
22	BST	+3.3V Regulator Boost Capacitor Connection (0.1µF to LX)
23	DHI	+3.3V Regulator High-Side Gate-Driver Output
24	LX	+3.3V Regulator Inductor Connection

Pin Description (continued)

25	3OUT	+3.3V Regulator Feedback Connection and Linear-Regulated + 3.3V Output
26	CS	+3.3V Regulator Current-Sense Input
27	SS	+3.3V Regulator Soft-Start Capacitor Connection
28	BATT	Battery Voltage Input
29	VCHG	Charger Voltage Input
30	UVLO	Undervoltage Lockout Threshold Input
31	REF	+2.5V Reference Output
32	AOUT	Analog Multiplexer Buffered Output
33	TEMP	Analog Multiplexer Input and Battery Sense Input
34	AUXIN	Analog Multiplexer Input
35	$\overline{SHDN}$	Shutdown-Mode Control Input
36	GD1	High-Side Gate-Driver Output

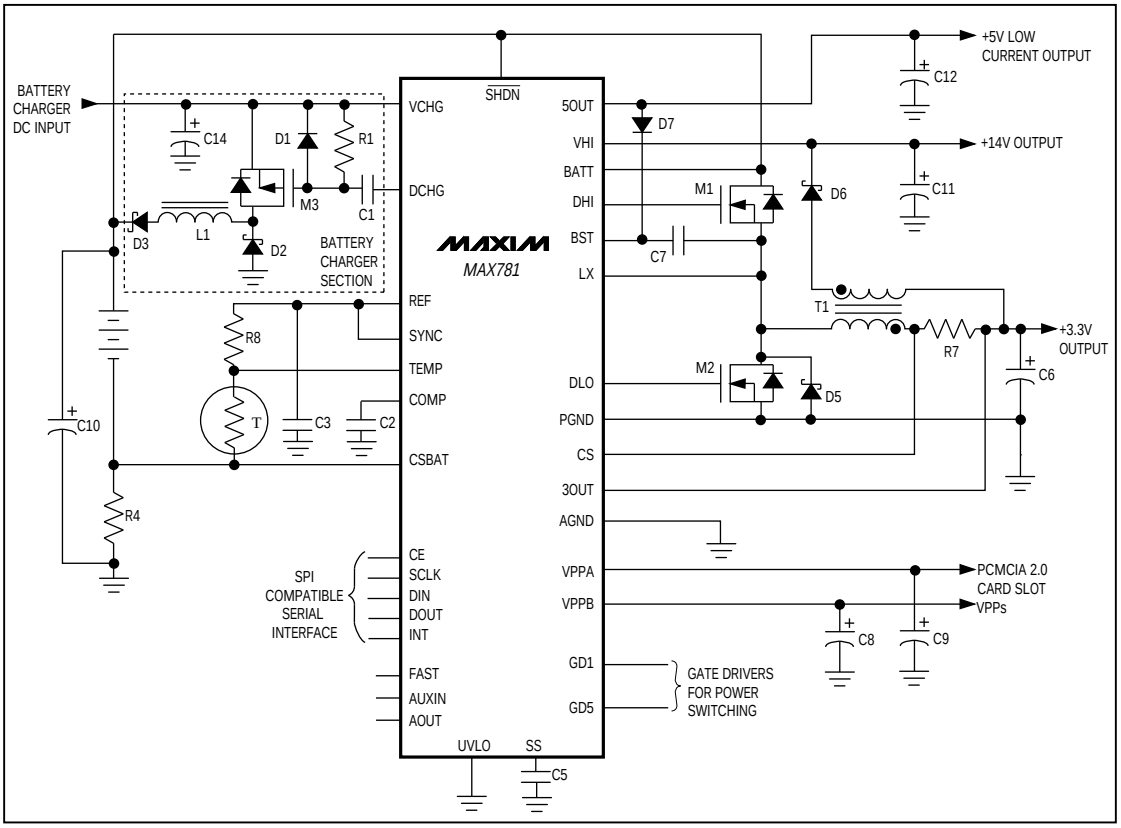


Figure 1. Typical Operating Circuit

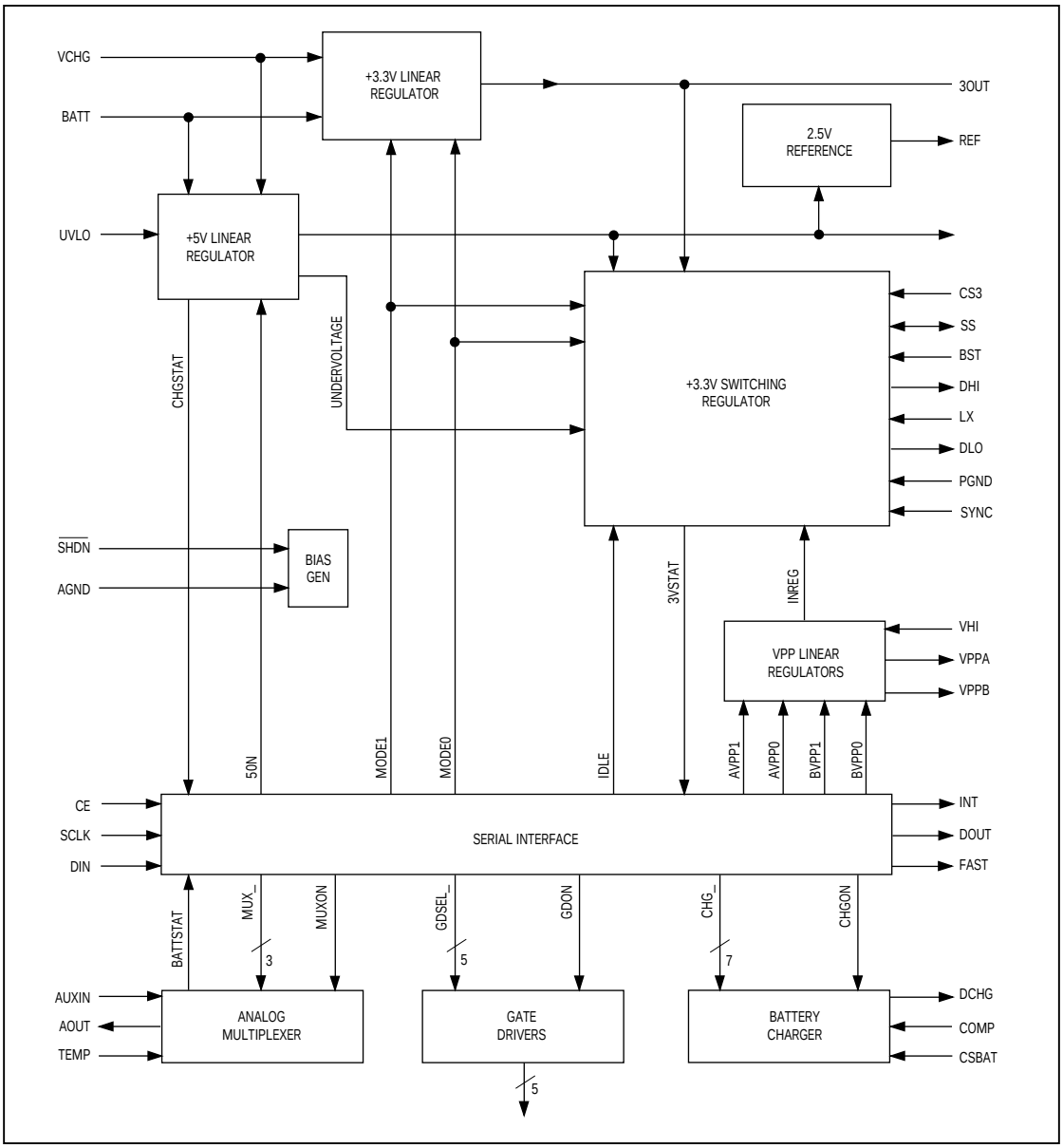


Figure 2. MAX781 Block Diagram

Detailed Description

Modes of Operation

Table 1 describes the MAX781's four modes of operation, and Table 2 shows how to select the desired mode. MODE1 and MODE0 are the two bits, out of a total of 32 bits of configuration data, which select the operational mode. See Table 3 for a complete list of the 32 bits of configuration data.

Table 1. MAX781 Modes of Operation

MODE	DESCRIPTION
Shutdown	• Entire chip shut down • All blocks turned off • I_Q < 10µA • 3OUT, 5OUT, REF off
Low Power	• Default on power-up • 3OUT supplies 10mA at +3.3V linear regulated from BATT • VPP outputs off (VPPA = VPPB = High-Z) • Analog multiplexer off (AOUT = High-Z) • High-side gate drivers off (GD1 = GD2 = GD3 = GD4 = GD5 = 0V) • Battery-charging current source off (DCHG = 5OUT)
Standby	• 3OUT supplies 10mA at +3.3V linear regulated from BATT • VPP outputs off (VPPA = VPPB = High-Z) • Analog multiplexer enabled • High-side gate drivers off • Battery-charging current source enabled
Operate	• Buck switching regulator on • 3OUT regulated to +3.3V • VPP outputs enabled • VHI regulated to +14V • Analog multiplexer enabled • High-side gate drivers enabled • Battery-charging current source enabled

With $\overline{SHDN}$ pulled up to the battery voltage, the MAX781 powers on in low-power mode. After power-up, pulling CE high temporaily places the MAX781 into operate mode and allows data to be shifted into the internal shift register. As soon as CE goes low, the MAX781 enters the mode programmed by the MODE1 and MODE0 bits.

Table 2. Operating Modes

$\overline{SHDN}$	MODE1	MODE0	CE	Resulting Mode
0	x	x	x	Shutdown
1	1	1	1	Operate
1	1	1	0	Low Power (default on power-up)
1	0	1	1	Standby
1	0	1	0	Low Power
1	0	0	x	Standby
1	1	0	x	Operate

Serial Interface

The MAX781 is controlled by 32 bits of configuration data. These 32 bits must be written, MSB first, into the MAX781 using a synchronous serial interface. Table 3 describes the function of each bit of configuration data. To turn the gate drivers on/off, select VPP voltages or program the analog multiplexer. CE, SCLK, DIN, and DOUT are the synchronous serial-interface pins. Figure 3 shows an example of the signal timing necessary to send 32 bits of data to the MAX781. The first six bits clocked out of DOUT are the status bits, and the remaining 26 bits clocked out of DOUT should be ignored. Figure 4 shows the detailed timing requirements of the synchronous serial interface.

To write the last eight bits of the configuration data without affecting the rest of the configuration bits, clock eight bits instead of 32 into DIN. This allows the CHARGE, IDLE, MODE1, MODE0, and VPP control bits to be updated in only eight serial clock cycles. As the eight bits are clocked into DIN, the status bits are clocked out of DOUT. Figure 5 shows an example of such a quick access. If eight zeros are sent in a quick access, no configuration data is updated. This allows the status bits to be read quickly without affecting the last byte of configuration data.

Status Bits

As the 32 bits of serial-configuration data are written into the MAX781, 32 bits of data are read out of DOUT. The first six bits contain status information, and the remaining 26 bits should be ignored.

BATTINT and BATTSTAT (Table 3) indicate battery status. It is assumed that the battery pack used with the MAX781 has a thermistor attached to its negative termi-

Table 3. Configuration Data-Bit Assignments

BIT	R/W	*	NAME	DESCRIPTION
31	R/W	0	BATTINT	1 = TEMP pin voltage crossed 0.82* 3OUT
30	R	0	BATTSTAT	1 = TEMP > 0.82*3OUT, 0 = TEMP < 0.82*3OUT
29	R/W	0	3VINT	1 = 3OUT fault detected
28	R	0	3VSTAT	1 = 3OUT out of regulation, 0 = in regulation
27	R/W	0	CHGINT	1 = VCHG > BATT detected
26	R	0	CHGSTAT	1 = VCHG > BATT, 0 = VCHG < BATT
25				Unused
24	W	0	GDSEL5	1 = GD5 sources from VHI, 0 = GD5 sinks to AGND
23	W	0	GDSEL4	1 = GD4 sources from VHI, 0 = GD4 sinks to AGND
22	W	0	GDSEL3	1 = GD3 sources from VHI, 0 = GD3 sinks to AGND
21	W	0	GDSEL2	1 = GD2 sources from VHI, 0 = GD2 sinks to AGND
20	W	1	GDSEL1	1 = GD1 sources from VHI, 0 = GD1 sinks to AGND
19	W	0	MUX2	Analog multiplexer bit 2
18	W	1	MUX1	Analog multiplexer bit 1
17	W	0	MUX0	Analog multiplexer bit 0
16	W	0	CHG6	Charger current setting DAC bit 6
15	W	0	CHG5	Charger current setting DAC bit 5
14	W	0	CHG4	Charger current setting DAC bit 4
13	W	0	CHG3	Charger current setting DAC bit 3
12	W	0	CHG2	Charger current setting DAC bit 2
11	W	1	CHG1	Charger current setting DAC bit 1
10	W	0	CHG0	Charger current setting DAC bit 0
9	W	1	50N	1 = 5OUT linear regulator on, 0 = off
8	W	0	FASTON	1 = FAST sinks current, 0 = FAST open drain
7	W	1	CHARGE	1 = DCHG switching current source on, 0 = off
6	W	1	IDLE	1 = Idle regulation, 0 = PWM regulation
5	W	1	MODE1	Operating mode select bit, 1, see Table 2
4	W	1	MODE0	Operating mode select bit, 0, see Table 2
3	W	0	VPPB1	VPPB voltage select bit 1, see Table 5
2	W	0	VPPB0	VPPB voltage select bit 0, see Table 5
1	W	0	VPPA1	VPPA voltage select bit 1, see Table 5
0	W	0	VPPA0	VPPA voltage select bit 0, see Table 5

* = Power-on reset default state

nal, causing the battery pack to need at least three terminals: BATT+, BATT,- and THERM. The MAX781's TEMP pin connects to the battery pack's thermistor (Figure 6). Without the battery pack installed, R8 pulls the MAX781's TEMP pin up to 3OUT, and BATTSTAT = 1. When the battery pack is inserted, the resistive divider formed by the thermistor and R8 pulls the TEMP pin below 3OUT, forcing BATTSTAT = 0. Any transition of BATTSTAT sets BATTINT. Clear BATTINT by writting a logic 1 in bit 31 of the serial-configuration data. The BATTSTAT comparator is disabled in low-power and shutdown modes, and outputs a logic zero regardless of the state of its inputs.

3VINT and 3VSTAT indicate the status of the 3OUT output (+3.3V ±4%). 3OUT is out of regulation when its output voltage falls below +3.1V. 3VSTAT = 0 when 3OUT is in regulation, and 3VSTAT = 1 when 3OUT is out of regulation. A rising edge on 3VSTAT sets 3VINT; thus, 3OUT going out of regulation sets 3VINT.

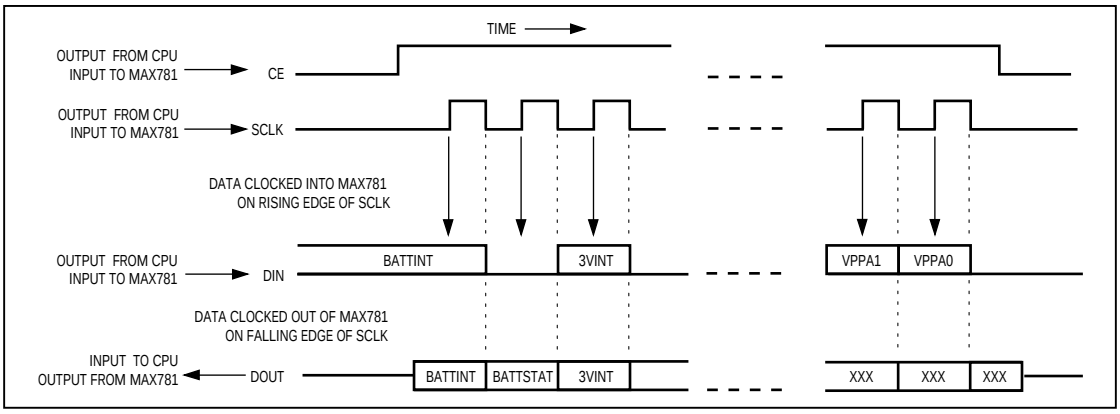


Figure 3. Serial Configuration Data Example Timing

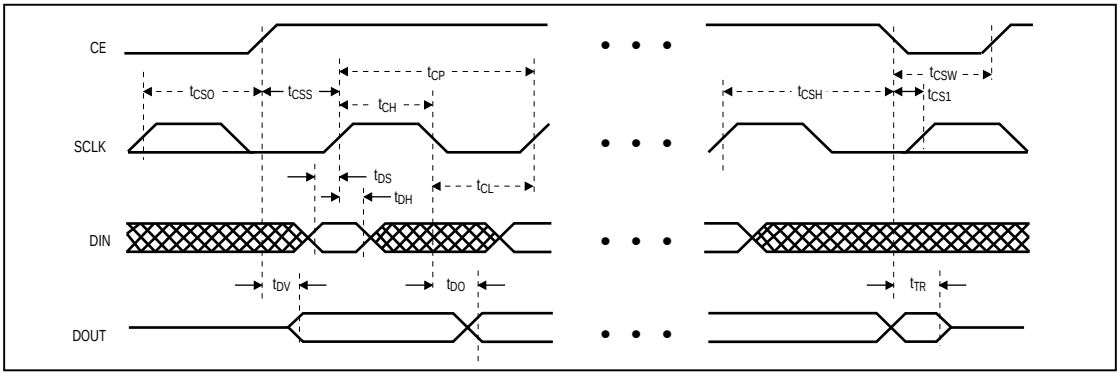


Figure 4. Detailed Timing Diagram

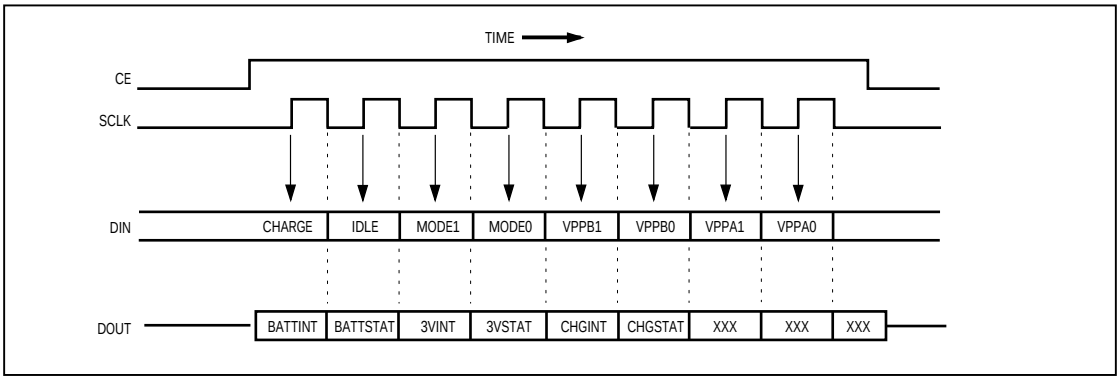


Figure 5. Quick-Access Example Timing

The 3VSTAT comparator is disabled in the low-power, standby, and shutdown modes, and outputs a logic zero regardless of the state of its inputs. The MAX781 serial-interface outputs are powered from 3OUT. If 3OUT is short circuited to ground, then neither DOUT nor INT will be able to source current.

CHGINT and CHGSTAT indicate the status of the charging voltage applied to VCHG. The MAX781 powers itself from either BATT or VCHG, whichever has the higher voltage. CHGSTAT = 0 when BATT is approximately 200mV greater than VCHG. CHGSTAT = 1 when BATT falls below VCHG plus approximately 200mV. Any transition on CHGSTAT sets CHGINT. The CHGSTAT comparator is disabled only in shutdown mode.

At power-up, BATTINT is set if the charger is not connected, CHGINT is set if the charger is connected.

Table 4. Status Detection in the Four Operating Modes

STATUS BIT	MODE			
	Shutdown	Low Power	Standby	Operate
BATTSTAT	Disabled	Disabled	Enabled	Enabled
3VSTAT	Disabled	Disabled	Enabled	Enabled
CHGSTAT	Disabled	Enabled	Enabled	Enabled

The INT pin outputs the logical OR of the BATTINT, 3VINT, and CHGINT status bits. The INT pin generates an interrupt on the CPU that controls the MAX781.

Supply and Reference

5OUT outputs +5V, linear regulated from either BATT or VCHG, in all modes except shutdown. 5OUT can source up to 25mA. Power comes from BATT as long as the BATT voltage is greater than the VCHG voltage. When the VCHG voltage exceeds BATT, VCHG supplies the 5OUT linear regulator.

The MAX781's internal circuitry is powered from 5OUT. When the DLO pin drives high, it sources current from 5OUT. The DOUT and INT pin output drivers are powered from 3OUT. If an external 5V supply is available and connected to the 5OUT pin, the 5OUT linear regulator can be disabled by clearing the 5ON bit. If 5ON is cleared without an external +5V supply connected to 5OUT, or if 5OUT is shorted to ground, the MAX781 internal registers will be cleared to their power-on state.

3.3V Output

3OUT outputs +3.3V in all modes except for shutdown. In low-power and standby modes, 3OUT is linear regulated from either BATT or VCHG, whichever has the higher voltage. In operate mode, the switch-mode buck (step-down) converter is activated to regulate 3OUT to 3.3V. In operate mode, the 3OUT linear regulator is off.

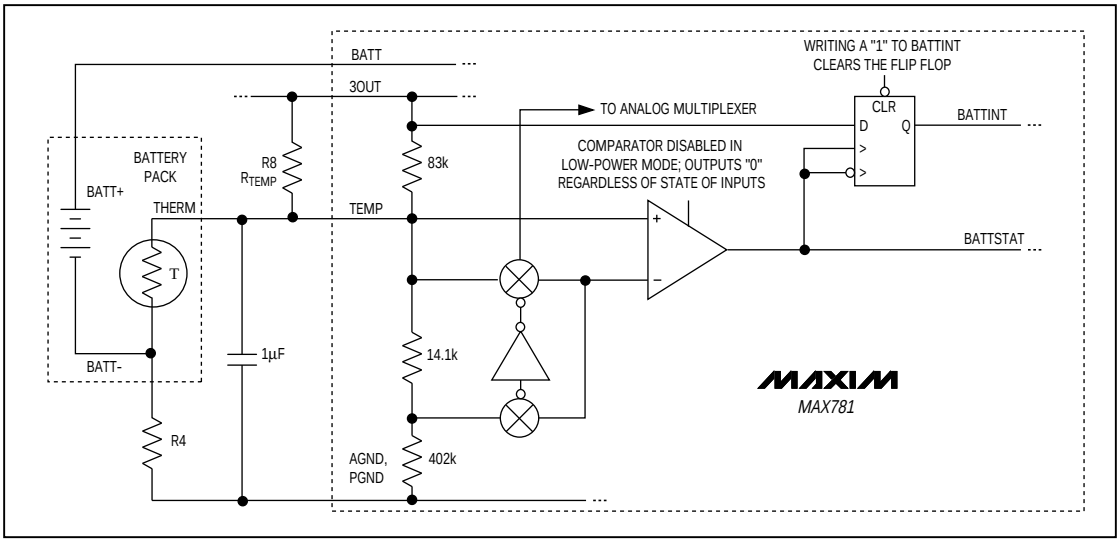


Figure 6. BATTINT, BATTSTAT Status Circuitry

DHI high-side drives an external N-channel power MOSFET, M1. Inside the MAX781, the DHI driver is well-isolated so it can be powered separately from the rest of the chip. The DHI driver is powered by current that flows into BST and out of LX. Thus, BST is the "power" connection and LX is the "ground" connection for the DHI driver. An internal level shifter allows the MAX781 internal circuitry to communicate with the DHI driver.

R_{SENSE}, connected from CS to 3OUT, senses current in the primary of transformer T1. With no load on VHI, the primary of T1 can be treated as the inductor in a current-mode buck converter. R_{SENSE} detects current in the primary and turns off M1 when the current limit is reached. The current limit is adjusted to ensure that 3OUT stays at 3.3V. With M1 off, M2 stays on until the voltage on R_{SENSE} reaches zero. There is an absolute current limit that protects the output in the event 3OUT is short circuited to ground. When the voltage from 3OUT to CS reaches 100mV, M1 is turned off whether or not 3OUT is in regulation.

A capacitor (C5) on the soft-start (SS) pin allows the current limit to slowly ramp up when power is first applied. A 4µA current source from 3OUT feeds the SS pin. The ramp time to full current limit is approximately 1ms for every nanofarad of capacitance on SS, with a minimum value of 10ns. Once the SS pin reaches 3.3V, the maximum peak current is available.

UVLO prevents the buck regulator and battery charger from switching if 5OUT is out of regulation. The voltage on UVLO is compared to REF. If UVLO is greater than REF, the buck regulator and battery charger will function normally. With UVLO less than REF, the buck regulator and battery charger stay off and the low-power mode linear regulator supplies 3OUT, whether or not operate mode has been set. Tying UVLO to AGND allows an internal resistive divider to feed the UVLO comparator, preventing operation of the buck regulator and battery charger for 5OUT voltages less than approximately 4.35V (see the *Electrical Characteristics*).

The MAX781 3.3V buck regulator is similar to the 3.3V buck regulator on the MAX783. For further information, refer to the MAX783 data sheet

Idle Regulation vs. PWM Regulation

In operate mode, 3OUT can be regulated using pulse-skipping (Idle-Mode™ regulation) or pulse-width-modulation (PWM) regulation. The IDLE bit selects the regulation scheme used for load current below about 25% of current limit.

Idle-Mode™ regulation pulses M1 until 25% of the absolute current limit is reached, at which point M1 turns off. M1 does not turn on again until 3OUT falls below 3.3V. This scheme improves light-load efficiency by minimizing the number of times M1 needs to be turned on to keep 3OUT in regulation. However, the operating frequency varies with load. At load currents above 25% of current limit, the regulator uses resonant frequency PWM regulation independent of the idle bit.

PWM regulation turns M1 on at a constant frequency and modulates M1's duty cycle to maintain the current required to keep 3OUT in regulation. The switching frequency remains constant regardless of the load current. Operating with a constant frequency results in lower amplitude and more easily filtered output ripple.

The SYNC pin either sets the internal switching frequency or synchronizes the MAX781 to an external oscillator. Tying SYNC to REF sets a switching frequency of 300kHz. Tying SYNC to 5V or AGND sets a 230kHz switching frequency. Driving SYNC with an external oscillator synchronizes the PWM switching with the external oscillator.

VPP Regulator

VPPA and VPPB linear regulate VHI down to 0V/+3.3V/+5V/+12V for use as a PCMCIA VPP voltage. The VPPB0, VPPB1, VPPA0, VPPA1 bits control the VPPB and VPPA output voltage. Programming VPPA or VPPB to 0V shuts off the linear regulator and saves quiescient supply current. Table 5 shows how to program the VPPA and VPPB control bits.

During the flyback phase of the buck converter (DLO on), VHI loads 3OUT. As long as DLO is on, power can be supplied to VHI. When 3OUT has a light load, DLO may not stay on long enough to supply power to VHI. To prevent VHI from sagging, an internal comparator checks VHI. If VHI sags below 12.8V, DLO is turned on for 1µs to provide power to VHI, regardless of the voltage on RSENSE. Power can only be delivered to VHI in operate mode when the buck switching regulator is active.

The VHI pin includes an overvoltage clamp that sinks current if VHI exceeds 19V.

This prevents the parasitic capacitance in transformer T1 from causing the VHI voltage to climb without limit.

™Idle-Mode is a trademark of Maxim Integrated Products.

Table 5. VPPA and VPPB Control Bits

VPPA1	VPPA0	VPPA Voltage (V)
0	0	0
0	1	5
1	0	12
1	1	3.3
VPPB1	**VPPB0**	**VPPB Voltage (V)**
0	0	0
0	1	5
1	0	12
1	1	3.3

Gate Drivers

GD1 through GD5 are gate-driver outputs that high-side drive external N-channel power MOSFETs. Loads connected to 3OUT can be connected or disconnected by using the circuitry shown in Figure 7. Clearing GDSEL1 (GDSEL1 = 0) causes GD1 to sink up to 450µA to AGND. Setting GDSEL1 (GDSEL = 1) causes GD1 to source up to 10µA from VHI. GD2–GD5 operate the same way. VHI is active (i.e., regulated to at least 12.8V) only in operate mode, so the gate drivers also only function in operate mode. GDSEL1 defaults to a 1 on power-up. GDSEL2 through GDSEL5 default to 0 on power-up.

FAST is a general-purpose output pin that sinks current when FASTON = 1 and goes open drain when FASTON = 0. FAST can be pulled up to any voltage up to 19V. To use FAST as a general-purpose 3.3V logic output, pull it up to 3OUT with a 100kΩ resistor. FAST may be used to pull the gate of M3 down to connect the battery to the input supply. The MAX781 does not limit the battery current when FAST is used in this way.

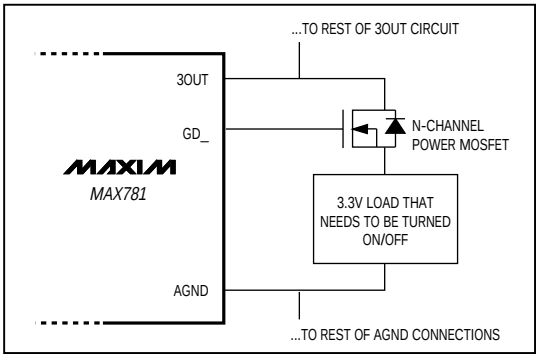


Figure 7. Using the Gate Drivers for High-Side Load Switching

Battery Charger

The battery charger is a voltage-mode average current regulator. Figure 8 shows a functional diagram of the battery charger circuitry. The GMAMP is a transconductance amplifer with approximately 62dB of open-loop DC gain. Set the GMAMP bandwidth with the capacitor on COMP.

GMAMP bandwidth in hertz = gm / C

where gm = 0.0006 mho (mho = 1/Ω) and C = capacitance on COMP in farads.

Average the current-sense signal by setting the GMAMP bandwidth much lower than the battery-charger switching frequency. The voltage output of the GMAMP at COMP is converted to a duty cycle, which is driven out of DCHG.

Serial-configuration bits CHG6–CHG0 set the average current level. When CHG6–CHG0 are all set (1111111), CSBAT is regulated to an average of 200mV. When CHG6–CHG0 equals binary 0111111, CSBAT is regulated to an average of 100mV.

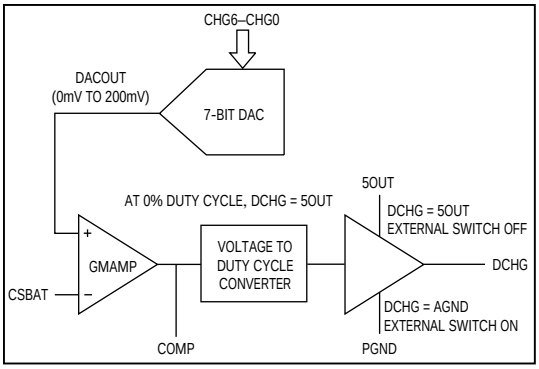


Figure 8. Battery-Charger Block Diagram

Analog Multiplexer

The MAX781's built-in buffered analog multiplexer selects one of eight different signal sources to be output from the AOUT pin. Figure 9 shows the analog multiplexer circuitry. The AOUT buffer amplifier is disabled in the shutdown and low-power modes, leaving the 89.7kΩ resistor to pull AOUT down to ground. Program the MUX0, MUX1, MUX2 bits in the serial-configuration data to select the analog multiplexer channel (Table 6). Resistive dividers in the signal paths scale the channels to ensure that AOUT is scaled to REF. The AOUT buffer amplifier can sink or source 1mA.

Table 6. Analog Multiplexer Channel Selection

MUX2	MUX1	MUX0	AOUT OUTPUTS
1	1	1	AUXIN/1.5
1	1	0	REF
1	0	1	VPPB/5.3
1	0	0	VPPA/5.3
0	1	1	TEMP/1.5
0	1	0	BATT/5
0	0	1	5OUT/2.2
0	0	0	3OUT/1.5

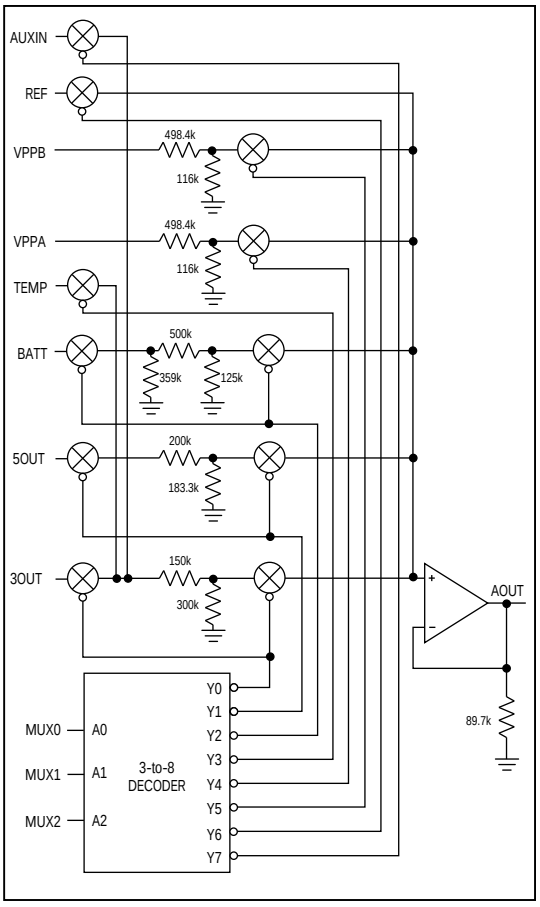


Figure 9. Analog Multiplexer Circuitry

_Component Selection and Layout

3.3V Output

Input and Output Bypass Capacitors

Capacitor C15 ensures that the buck regulator has a low AC-impedance power source. C15's root mean square ripple-current rating must be greater than 0.5 x (maximum power output capability of the system) / 3.3V. Capacitor C6 keeps 3OUT output ripple low and stabilizes the regulation loop. C15 and C6 must have low equivalent series resistance (ESR), preferably with less than 0.2Ω of ESR at 200kHz. Tantalum capacitors typically have the lowest ESR. C15's ground connection must be as close as possible to C6's ground connection; ideally, the two capacitors will be grounded at the same point. The MAX781's AGND pin should only connect to system ground at the ground connection of C15 and C6. If the PC board has a ground plane, a separate trace should directly connect AGND to the ground connections of C15 and C6. Likewise, the BATT pin should only connect to the battery at C15's positive terminal.

The capacitance and ESR of C6 determine loop stability. To ensure loop stability, the minimum capacitance and maximum ESR values are:

$$C6 > 2.5V / (3.3V \times R7 \times 2 \times p \times GBWP)$$

with C6 specified in Farads, R7 specified in ohms, GBWP = gain bandwidth product of 60,000Hz, and:

$$C6\ ESR < (3.3V \times R7) / 2.5V$$

with C6 ESR specified in ohms, and R7 specified in ohms.

In order to achieve the required low ESR, it may be appropriate to select a value greater than the minimum for C6, or to construct a composite C6 by paralleling several smaller capacitors.

Current-Sense Resistor

Current-sense resistor R7 sets the maximum peak current through power switch M1 and the primary of transformer T1. The MAX781's maximum peak current limit is 120mV / R, where R is the minimum possible resistance for R7, and 120mV is the maximum electrical specification for the current-limit threshold. For example, selecting a 0.082Ω ±1% resistor for R7 yields a maximum peak current limit of 120mV / 0.082Ω x 0.99 = 1.478A. The maximum peak current limit must be less than or equal to the maximum allowed continuous DC current through either M1 or the primary of T1.

R7 also determines how much power 3OUT, VPPA, and VPPB can deliver. The current-limit threshold can be as small as 80mV and, using a 0.082Ω ±1% resistor,

R7 can be as large as 0.082Ω x 1.01 = 0.0828Ω, yielding a minimum peak current limit of 80mV / 0.0828Ω = 0.966A.

Use the spreadsheet in Listings 1 and 2 to calculate the power available at 3OUT as a function of the current-sense resistor choice.

Listing 1. Spreadsheet for Calculating 3OUT Current Capability

Parameter (Cell A1)	Min (Cell B1)	Max (Cell C1)	Units
Current-Limit Threshold	80	120	mV
Current Sense R7	81	83	mΩ
Current Limit	0.964	1.481	A
Switching Frequency	270	340	kHz
Switching Period	2.941	3.704	µs
T1 Primary Inductance	16	24	µH
3OUT Regulation Point	3.170	3.430	V
BATT Input Range	5.000	17.500	V
(Cell A10)			
Current Limit	0.964		A
Switching Period		3.704	µs
T1 Primary Inductance	16		µH
3OUT		3.430	
BATT		17.500	
VHI Load Current		60	mA
T1 Turns Ratio		3.5	
T1 Coupling Loss		80	%
(Cell A20)			
T1 Ripple Current		0.638	A
T1 Continuous Current		0.325	A
3OUT Current, No VHI load		0.645	A
VHI Load Power		0.926	W
3OUT Guaranteed Current		0.307	A
(Cell A26)	(Cell B26)	(Cell C26)	

Listing 2. Calculating 3OUT Current-Capability Formulas

B4: +B2/C3

C4: +C2/B3

B6: 1/C5*1000

C6: 1/B5*1000

B12: +B4

C13: +C6

B14: +B7

C15: +C8

C16: +C9

C21: @MIN(+C15/C16*C13*(C16-C15)/B14,B12)

C22: +B12-C21

C23: @IF(C22=0,0.5*(B14/1000000)*C21^2*1000000/C13/C15,C22+C21/2)

C24: +C15*(C18+1)*C17/1000

C25: +C23-C24/(C19/100)/C15

R7 must have as little series inductance as possible and be as physically small as possible. 3OUT and CS3 need to Kelvin sense R7. A pair of traces running in parallel should leave 3OUT and CS3 and diverge only when they meet R7. Minimize the distance between R7 and the positive terminal of C6.

Power MOSFETs

M1 and M2 must be logic level, low $r_{DS(ON)}$, N-channel power MOSFETs. M1's drain should be as close as possible to C15's positive terminal and M2's source should be as close as possible to C15's ground connection point.

Transformer T1

T1's primary inductance must be between 10µH and 100µH. The peak current allowed through the primary with the secondary open circuited must be greater than the worst-case peak current set by R7. T1's turns ratio (number of turns on secondary / number of turns on primary) should be 3.5. If VHI rises up to 20V when 3OUT is loaded in operate mode, T1 may have too much interwinding capacitance. Minimize interwinding capacitance to prevent energy waste in the VHI clamp (which clamps VHI to 19V to protect the MAX781).

Applications Information

Design Example

Table 7 shows the targets for a typical design requirement. Since both PCMCIA slots will not be programmed at the same time, VPPA and VPPB will never be at +12V at the same time; thus the worst case for power consumption is when both 3.3V and VPPA or VPPB is fully loaded.

Total power consumption = (max 3OUT voltage) x (max 3OUT load current) + (VHI voltage) x (max VPP or load current) / (transformer efficiency).

Table 7. Specifications for a Typical Design

PARAMETER	DESIGNATION	MIN	MAX	UNITS
Input Power	5 NiCD cells	5		V
	15V DC adapter		17.5	
3.3V Output Current		300		mA
VPPA Output Current	+12V output when programming flash memory in Slot A	60		mA
VPPB Output Current	+12V output when programming flash memory in Slot A	60		mA
Charge Current	Digitally programmable	0	1	A

VPPA and VPPB are linear regulated from VHI, so the power consumed by loads on VPPA or VPPB equals the VHI voltage times the load current. Barring a Schottky diode drop, VHI equals the 3OUT voltage x (1 + turns ratio). With the specifications of Table 7 and an 80% transformer efficiency, the total power consumption works out to 2.037W; thus the average current through the primary of T1 is 594mA. The peak current through the primary of T1 will depend on the minimum primary inductance. As a rule of thumb, the peak current will be about 1.5 times the average current. For an average current of 594mA, the peak current would be about 900mA. To achieve a 900mA peak current, select R7 to be 80mV / 900mA = 0.088Ω. The closest comercially available value would be 0.082Ω ±1%. The spreadsheet in Listing 1 calculates how high a guaranteed output current can be, given commercially available component values, and taking component tolerances into account.

Table 8 shows the electrical specifications for a transformer that meets the requirements of Listing 1.

Power MOSFETs M1 and M2 should have an on-resistance at logic-level gate drive ($r_{DS(ON)}$ at V_{GS} = 4.5V) of the same order as T1's primary DC resistance. The Siliconix Si9955DY dual N-channel MOSFET satisfies this requirement with a 0.2Ω maximum on-resistance per device.

Table 8. Dale Electronics M/N LPE-6562-A070 Specifications

PARAMETER	MIN	TYP	MAX	UNITS
Primary Inductance	16	20	24	µH
Leakage Inductance (at $0.1V_{RMS}$, 100kHz)			0.03	µH
Primary Continuous DC Current			2.6	A
Primary DC Resistance			0.075	Ω
Secondary DC Resistance			0.51	Ω
Turns Ratio (secondary/primary)		3.5		

Table 9 lists the bill of materials for an example circuit that fulfills the requirements of Table 7.

Driving a CCFL Backlight Royer Oscillator

The digitally adjustable current from the battery charger can be used to drive a Royer oscillator. The Royer oscillator is a resonant circuit fed by a constant current. The root mean square current out of the secondary winding of the Royer transformer is proportional to the current fed into the center tap of the Royer transformer. Figure 10 shows the application circuit. The diode from VCHG to BATT keeps BATT from dropping too far below 5OUT, which causes excess supply current. Figure 11 shows how the programmed current corresponds to the CCFL root mean square tube current.

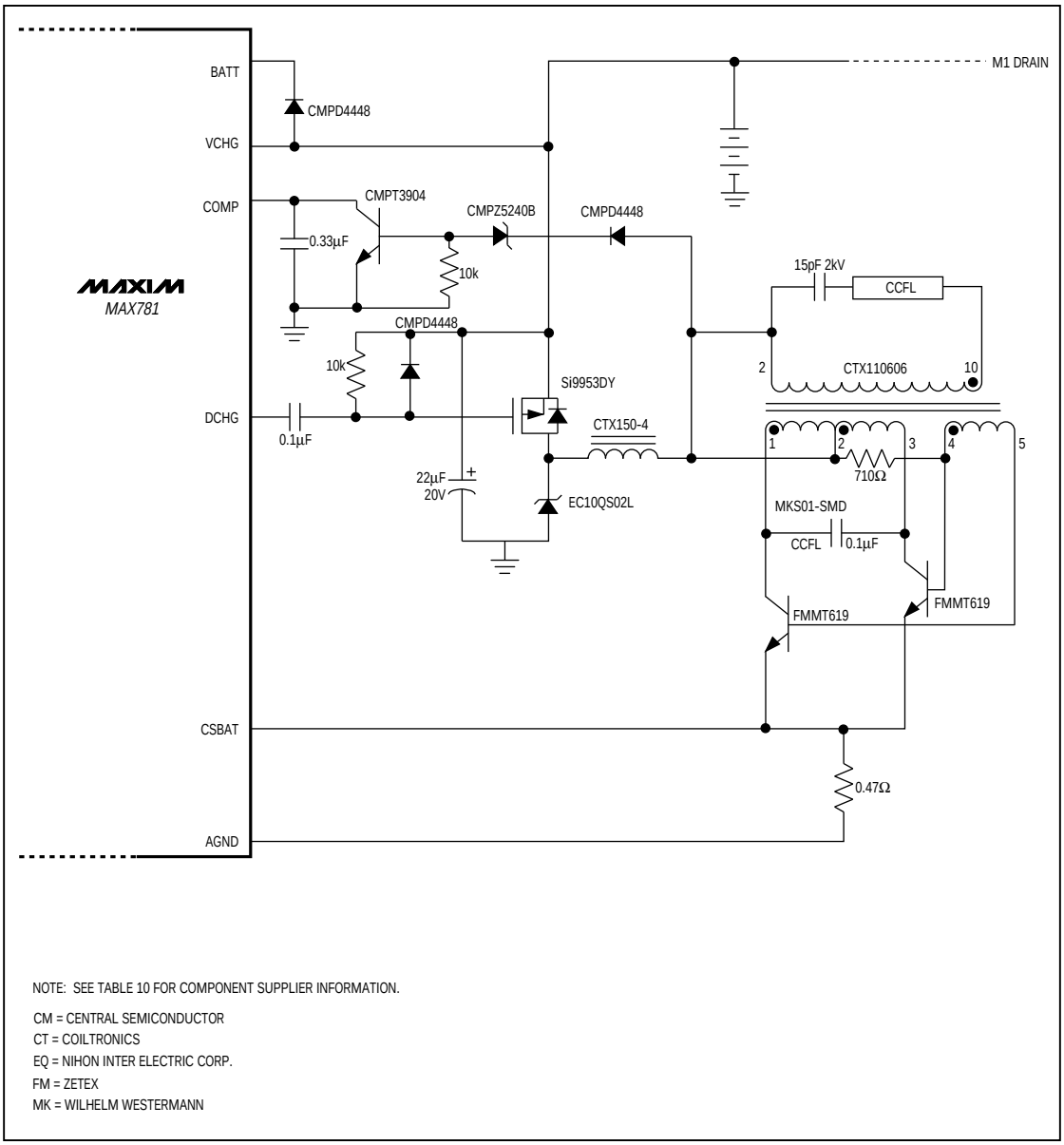
The NPN transistor connected to COMP and the zener diode protects the transformer from an open-tube condition by shutting off the Si9953DY if pin 2 of the CTX110606 exceeds 0.6V + 10V + 0.6V. This limits the voltage on the secondary to 11.2 x 171 x 2 = 3830.4V peak-to-peak = $1354V_{RMS}$, which is well within the CTX110606 maximum secondary voltage specification of $2010V_{RMS}$.

Table 9. Design Example Bill of Materials

SYMBOL	DESCRIPTION	PART No.	MANUFACTURER
T1	transformer	M/N LPE-6562-A070	Dale
L1	47µH, 1.5A IDC inductor	CDR125-470	Sumida
M1, M2	N-Channel MOSFETs	Si9955DY	Siliconix
M3	P-Channel MOSFET	Si9953DY	Siliconix
R1	100kΩ, ±20% resistor		
R4	0.2Ω, ±1% resistor		IRC
R7	0.082Ω, ±1% resistor		IRC
R8	10kΩ, ±1% resistor		
C1	0.1µF, 20V capacitor		
C2	0.33µF, 6V capacitor		
C3	1µF, 6V capacitor		
C5	0.01µF, 6V capacitor		
C6	120µF, 6.3V capacitor, 0.09Ω ESR at 100kHz	195D127X06R3R2T	Sprague
C7	0.1µF, 10V capacitor		
C8	1µF, 16V capacitor		
C9	1µF, 16V capacitor		
C10	22µF, 25V capacitor	195D226X0025R2T	Sprague
C11	2.2µF, 25V capacitor		
C12	1µF, 6V capacitor		
C14	22µF, 25V capacitor	195D226X0025R2T	Sprague
D1	20V 1N4150 type diode	CMPD4150	Central
D2	20V Schottky diode	EC10QS03	Nihon
D3	20V Schottky diode	EC15QS03	Nihon
D5	20V Schottky diode	EC10QS03	Nihon
D6	50V Schottky diode	EC10QS05	Nihon
D7	20V 1N4150 type diode	CMPD4150	Central

Table 10. Component Suppliers

SUPPLIER	PHONE	FAX
Central Semiconductor	(516) 435-1110	(516) 435-1824
Coiltronics	(407) 241-7876	(407) 241-9339
Dale	(605) 665-9301	(605) 665-1627
IRC	(213) 772-2000	(213) 772-9028
Nihon Rep: Quantum Marketing	Japan 81-3-3494-7411 USA (805) 867-2555	81-3-3494-7414 (805) 867-2698
Siliconix	(800) 554-5565	(408) 970-3950
Sprague	(603) 224-1961	(603) 224-1430
Sumida	(708) 956-0666	(708) 956-0702
Wilhelm Westerman Rep: Inter-Technical Group	Germany 0621-408012 USA (914) 347-2474	0621 403538 (914) 347-7230
Zetex	USA (516) 543-7100 UK 061-627-4963	(516) 864-7630 061-627-5467



NOTE: SEE TABLE 10 FOR COMPONENT SUPPLIER INFORMATION.

CM = CENTRAL SEMICONDUCTOR
CT = COILTRONICS
EQ = NIHON INTER ELECTRIC CORP.
FM = ZETEX
MK = WILHELM WESTERMANN

Figure 10. Digitally Adjustable CCFL Backlight Circuit

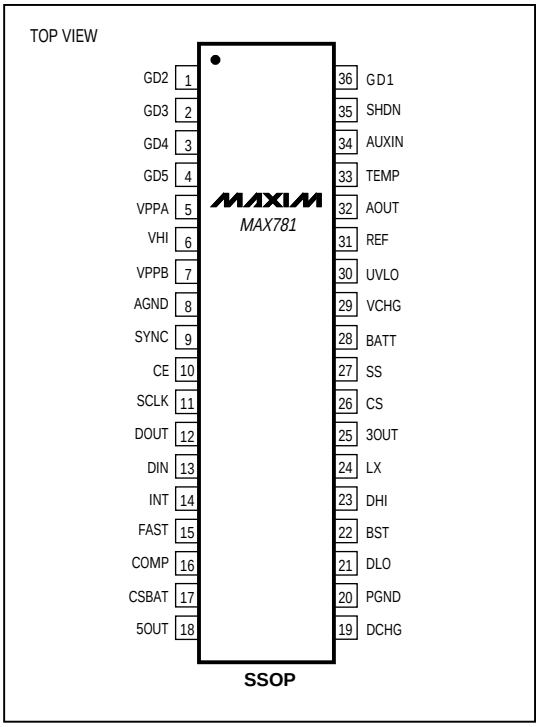
Interfacing the MAX781 to an IBM Compatible PC

Figure 1 shows the MAX781 typical operating circuit. On power-up, with 4.8V < BATT < 18V and CE = SCLK = DIN = 0V, the MAX781 is in low-power mode. 3OUT outputs +3.3V linear regulated from BATT, and REF outputs +2.5V. INT should output a 3.3V logic high. Neither DHI nor DLO should be switching. Serial data must be sent to the MAX781 in order to change modes. The parallel printer interface on a personal computer can be used to send serial control data to the MAX781. Listing 3 shows a simple Microsoft Quick Basic program for communicating with the MAX781 over the LPT1 parallel interface port.

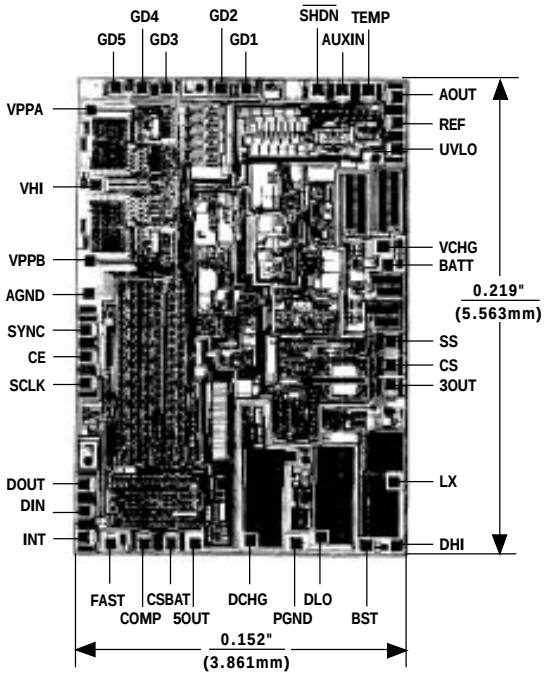
Listing 3. MAX781 Control Program in QBasic

```
REM Connect a DB25 parallel cable from LPT1 to the circuit of
REM of figure 1.      Roger Chen  MAXIM Applications 7/8/93
REM written in MS-DOS QBasic v1.0.
REM Connect pin 2 of the DB25 to CE, pin 3 to SCLK,
REM pin 4 to DIN, pin 13 to DOUT.
DEF SEG = &H0: address = (PEEK(&H409) * 256) + (PEEK(&H408))
DIM bytes$(3)
bytes$(3) = "00000000"
bytes$(2) = "00010100"
bytes$(1) = "00001010"
bytes$(0) = "11110000"
OUT address, 0
start:
h = 0
i = 3
PRINT "****  MAX781 CONTROL PROGRAM", DATE$, TIME$; "  ****"
PRINT "ENTER 'S' AT BYTE 2 TO SEND ONLY ONE BYTE, 'Q' TO QUIT"
loopstart:
   PRINT "Byte"; i; "= "; bytes$(i); ", Enter byte"; i;
   INPUT a$
   IF LEFT$(a$, 1) = "q" OR LEFT$(a$, 1) = "Q" THEN END
   IF LEFT$(a$, 1) = "s" OR LEFT$(a$, 1) = "S" THEN h = i + 1
   IF LEN(a$) = 8 THEN bytes$(i) = a$
   i = i - 1
IF i >= h THEN GOTO loopstart
d = 1
result$ = ""
OUT address, d
FOR i = 3 TO h STEP -1
   FOR character = 1 TO 8
      IF MID$(bytes$(i), character, 1) <> "1" THEN GOTO zero
      d = d OR 4
      a$ = "1"
      GOTO zeroend
zero:
      d = d AND (255 - 4)
      a$ = "0"
zeroend:
      OUT address, d
      PRINT a$;
      temp = ABS((INP(address + 1) AND 16) = 16)
      result$ = result$ + CHR$(ASC("0") + temp)
      d = d OR 2
      OUT address, d
      d = d AND (255 - 2)
      OUT address, d
      NEXT
NEXT
OUT address, 0
PRINT
PRINT result$
GOTO start
```

Pin Configuration



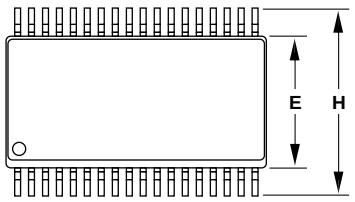
Chip Topography



TRANSISTOR COUNT: 2661

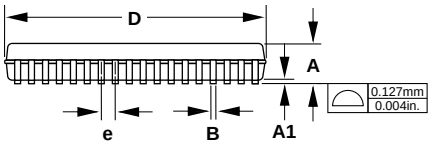
SUBSTRATE CONNECTED TO AGND.

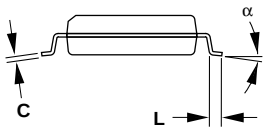
Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.64
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
D	0.604	0.610	15.34	15.49
E	0.292	0.298	7.42	7.57
e	0.032 BSC		0.80 BSC	
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89
α	0°	8°	0°	8°

21-0032A





36-PIN PLASTIC SHRINK SMALL-OUTLINE PACKAGE