19-5522; Rev 0; 9/10

MAX19527 Evaluation Kit

Evaluates: MAX19527

General Description

The MAX19527 evaluation kit (EV kit) is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX19527 50Msps octal, 12-bit analog-to-digital converter (ADC). The EV kit also includes Windows® 2000-, Windows XP®-, and Windows Vista®-compatible software that provides a simple graphical user interface (GUI) for exercising the features of the ADC.

The EV kit accepts single-ended analog inputs from an analog signal source and provides an on-board circuit that transforms the analog single-ended signal into a differential signal. The ADC digital LVDS outputs can be captured easily with Maxim's data converter evaluation platform (DCEP). The EV kit operates from a single 3.3V power supply and provides on-board regulation for the analog, digital, and logic circuitries.

Features

- **Single Power-Supply Operation**
- **Direct Interface with the Maxim DCEP Data Board Using a QSH Connector**
- **Low-Voltage and Low-Power Operation**
- **On-Board Single-Ended-to-Differential Transformer Circuitry**
- **Differential or Single-Ended Clock Configuration**
- **On-Board Clock-Shaping Circuit with Adjustable Duty Cycle**
- **On-Board or Stand-Alone SPI™ Interface Control**
- **DCEP Board Available**
- **Fully Assembled and Tested**

Ordering Information

PART	TYPE
MAX19527EVKIT+	EV Kit
DCEP	Data Converter Evaluation Platform

+Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
B9, CMOUT, TP1–TP8	10	Red PC test points
C1–C16, C58, C62–C65, C114	22	0.1µF ±10%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104K or Murata GRM155R61A104K
C41–C56	16	39pF ±5%, 50V C0G ceramic capacitors (0402) TDK C1005C0G1H390J or Murata GRM1555C1H390J
C57, C77, C81	3	1µF ±10%, 6.3V X5R ceramic capacitors (0402) TDK C1005X5R0J105K or Murata GRM155R60J105K
C59, C89, C90, C95–C98, C103–C106, C111, C112, C113, C130, C133, C135, C136, C137, C140, C141, C144, C145, C146	24	0.1µF ±10%, 50V X5R ceramic capacitors (0603) TDK C1608X5R1H104K or Murata GRM188R51H104K
C60, C61, C66–C69	0	Not installed, ceramic capacitors (0603)
C74, C78	2	220µF ±20%, 6.3V tantalum capacitors (C case) AVX TPSC227M006R0250 or KEMET T495C227K006ATE225
C75, C79	0	Not installed, tantalum capacitors (C case)

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SPI is a trademark of Motorola, Inc.

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
C76, C80, C82	3	10µF ±20%, 10V X5R ceramic capacitors (1210) TDK C3225X5R1A106M or Murata GRM32ER61A106K
C83, C85, C86, C88, C131	5	10µF ±20%, 10V X5R ceramic capacitors (0805) TDK C2012X5R1A106K Murata GRM219R61A106K
C84, C87, C91–C94, C99-C102, C107–C110, C115, C116	16	0.01µF ±10%, 50V X5R ceramic capacitors (0603) Murata GRM188R61H103K or TDK C1608X5R1H103K
C132	1	1µF ±10%, 10V X5R ceramic capacitor (0603) TDK C1608X5R1A105K Murata GRM188R61A105K
C134	1	0.033µF ±10%, 16V (min) X5R ceramic capacitor (0603) Murata GRM188R71E333K or TDK C1608X7R1E333K
C138, C139, C142, C143	4	22pF ±5%, 50V C0G ceramic capacitors (0603) TDK C1608C0G1H220J
CLK, IN1–IN8	9	SMA PC-mount connectors
D1	1	Dual Schottky diode (SOT23) Central Semi CMPD6263S+ (Top Mark: D96)
H1	1	120-position high-speed connector
H2	1	Dual-row (2 x 20) 40-pin header
J1	1	Dual-row (2 x 16) 32-pin header
J2	1	2-pin header
J10	1	Dual-row (2 x 5) 10-pin header
JU1–JU8, JU10, JU14, JU15	11	2-pin headers
JU9	1	3-pin header
JU11, JU12, JU13	3	4-pin headers
JU20–JU27	0	Not installed, 2-pin headers—short
L101	0	Not installed, ferrite bead (0603)

DESIGNATION	QTY	DESCRIPTION
P1	1	USB type-B right-angle PC-mount receptacle
R1–R32, R73–R76, R81–R84, R89, R90, R93, R95	44	100Ω ±1% resistors (0603)
R33–R48	16	10Ω ±1% resistors (0402)
R57–R72	16	0Ω ±5% resistors (0805)
R77–R80, R85–R88, R91, R92, R96, R98, R99, R102, R103, R104, R105	0	Not installed, resistors (0603) R99, R103, and R104 are short (PC trace); all others are open
R94	1	10kΩ potentiometer, 19-turn, 3/8in
R97	1	100kΩ ±1% resistor (0603)
R100, R101	2	49.9Ω ±1% resistors (0603)
R130, R131	2	27Ω ±5% resistors (0603)
R132	1	1.5kΩ ±5% resistor (0603)
R133	1	2.2kΩ ±5% resistor (0603)
R134, R137	2	10kΩ ±5% resistors (0603)
R135	1	470Ω ±5% resistor (0603)
R136	1	1.1Ω ±5% resistor (0603)
SW1	1	Momentary 6mm pushbutton switch
T1–T8	8	1:1, 800MHz RF transformers Mini-Circuits ADT1-1WT+
T9	1	1:2 RF transformer Coilcraft TTWB-2-B
U1	1	Octal 12-bit 50Msps ADC (144 CTBGA) Maxim MAX19527EXE+
U2, U3	2	500mA LDO regulators (8 TDFN-EP*) Maxim MAX8902AATA+ (Top Mark: ABG)
U4, U5, U6	3	Dual 2 x 2 crosspoint switches (32 TQFP) Maxim MAX9392EHJ+
U7	1	TinyLogic ULP-A inverter (6 SC70) Fairchild NC7WV04P6X (Top Mark: V07)

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
U8	1	UART-to-USB converter (32 TQFP) FTDI FT232BL
U9	1	93C46 type 3-wire EEPROM (8 SO) Atmel AT93C46EN-SH-B
U10	1	Ultra-high-speed microcontroller (44 TQFP) Maxim DS89C450-ENL+
U11	1	Level translator (20 TSSOP) Maxim MAX3002EUP+
U12	1	Quad three-state driver (14 SO) Fairchild 74AC125SC
U13	0	Not installed, LDO regulator (5 SC70)
U14	0	Not installed, level translator (14 TSSOP)
Y1	1	14.7456MHz crystal
Y2	1	6MHz crystal
—	15	Shunts (JU1–JU15)
—	1	PCB: MAX19527 EVALUATION KIT+

**EP = Exposed pad.*

Component Suppliers

SUPPLIER	PHONE	WEBSITE
AVX Corporation	843-946-0238	www.avxcorp.com
Central Semiconductor Corp.	631-435-1110	www.centralsemi.com
Coilcraft, Inc.	847-639-6400	www.coilcraft.com
Fairchild Semiconductor	888-522-5372	www.fairchildsemi.com
KEMET Corp.	864-963-6300	www.kemet.com
Mini-Circuits	718-934-4500	www.minicircuits.com
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
Samtec, Inc.	800-726-8329	www.samtec.com
TDK Corp.	847-803-6100	www.component.tdk.com

Note: *Indicate that you are using the MAX19527 when contacting these component suppliers.*

MAX19527 EV Kit Files

FILE	DESCRIPTION
INSTALL.EXE	Installs the EV kit files on your computer
MAX19527.EXE	Application program
FTD2XX.INF	USB device driver file
UNINST.INI	Uninstalls the EV kit software
USB_Driver_Help_200.PDF	USB driver installation help file

Quick Start

Recommended Equipment

- MAX19527 EV kit
- Single 3.3V, 1A DC power supply
- Signal generator with low phase noise and low jitter for clock input (e.g., HP 8644B)
- Signal generator for analog signal input (e.g., HP 8644B)
- Maxim DCEP
- Analog bandpass filters (e.g., K&L Microwave) for input and clock signals
- User-supplied Windows 2000, Windows XP, or Windows Vista PC with two spare USB ports

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

Procedure

The EV kit is a fully assembled and tested surface-mount board. Follow the steps below to verify board operation. **Caution: Do not turn on power supplies or enable signal generators until all connections are completed.**

1) Verify that shunts are configured in their default positions (Table 1) for proper startup operation of the EV kit software.
2) Connect the clock generator output to the clock bandpass filter input.
3) Connect the output of the clock bandpass filter to the EV kit CLK SMA connector.
4) Connect the outputs of the analog signal generators to the input of the signal bandpass filters. Keep the cable connection between the signal generators, filters, and EV kit board as short as possible for optimum dynamic performance.
5) Connect the output of the signal bandpass filters to the IN_ SMA connectors. It is recommended that a 3dB or 6dB attenuation pad be used to reduce reflections and distortion from the bandpass filter.
6) Carefully connect the boards by aligning J5 on the DCEP board to H1 on the EV kit. Gently press them together.
7) Connect the USB cable from the computer's type-A USB port to the DCEP board's type-B USB port.
8) Connect the 3.3V, 1A power supply to the +3.3V PCB pad. Connect the ground terminal of this supply to the corresponding GND pad.
9) Visit **www.maxim-ic.com/evkitsoftware** to download the latest version of the EV kit software and install it on your computer by running the INSTALL.EXE program. The program files are copied and icons are created in the Windows **Start | Programs** menu.
10) Apply power to the DCEP board at J4 using the DCEP board provided supply connector.
11) Enable the 3.3V power supply.
12) Enable the signal generators.
13) Set the clock signal generator for an output amplitude of ≥ 2.7V_{P-P} (recommended +16dBm to +19dBm for optimum AC performance for input frequencies > 25MHz) and the frequency (f_{CLK}) as appropriate.
14) Set the analog input signal generators for an output amplitude of ≤ 1.5V_{P-P}, and to the desired frequency.
15) Verify that the signal generators are phase locked to each other. Adjust the output power level of the signal generators to overcome cable, bandpass filter, and attenuation pad losses at the input.
16) Start the EV kit program by opening its icon in the **Start | Programs** menu.
17) Refer to the Data Converter Evaluation Platform (DCEP) User's Guide for information on installing the DCEP software.
18) Start the DCEP program by opening its icon in the **Start | Programs** menu.
19) Create a new database in the DCEP by adding the device module file, MAX19527-EVK-xx.dsm. Refer to the *Opening a New Database* section in the Data Converter Evaluation Platform (DCEP) User's Guide for additional information.
20) Collect data using the DCEP software.

Table 1. Jumper Configuration (JU1–JU15)

JUMPER	SHUNT POSITION	EV KIT FUNCTION
JU1	Not installed	IN1 input network disconnected from CMOUT
	Installed*	IN1 input network connected to CMOUT
JU2	Not installed	IN2 input network disconnected from CMOUT
	Installed*	IN2 input network connected to CMOUT
JU3	Not installed	IN3 input network disconnected from CMOUT
	Installed*	IN3 input network connected to CMOUT
JU4	Not installed	IN4 input network disconnected from CMOUT
	Installed*	IN4 input network connected to CMOUT
JU5	Not installed	IN5 input network disconnected from CMOUT
	Installed*	IN5 input network connected to CMOUT
JU6	Not installed	IN6 input network disconnected from CMOUT
	Installed*	IN6 input network connected to CMOUT
JU7	Not installed	IN7 input network disconnected from CMOUT
	Installed*	IN7 input network connected to CMOUT
JU8	Not installed	IN8 input network disconnected from CMOUT
	Installed*	IN8 input network connected to CMOUT
JU9	1-2	SHDN connected to AVDD (power-management mode to SHDN = 1)
	2-3*	SHDN connected to GND (power-management mode to SHDN = 0)
JU10	Not installed	CMOUT disconnected from input networks
	Installed*	CMOUT connected to input networks
JU11	1-2*	SCLK signal supplied by the USB circuitry
	1-3	Maintains the ADC register's content
	1-4	For future use
	Not installed	SCLK signal supplied by an external source at header J10
JU12	1-2*	SDIO signal supplied by the USB circuitry
	1-3	Maintains the ADC register's content
	1-4	For future use
	Not installed	SDIO signal supplied by an external source at header J10
JU13	1-2*	$\overline{CS}$ signal supplied by the USB circuitry
	1-3	Maintains the ADC register's content
	1-4	For future use
	Not installed	$\overline{CS}$ signal supplied by an external source at header J10
JU14	Installed*	1.8V LDO (U2) powers the AVDD input
	Not installed	1.8V LDO(U2) output disconnected from the AVDD input
JU15	Installed*	1.8V LDO (U3) powers the OVDD input
	Not installed	1.8V LDO (U3) output disconnected from the OVDD input

**Default position.*

Detailed Description of Software

Software Startup

Before starting the MAX19527 EV kit software, verify that shunts are configured in their default states, as shown in Table 1 and a valid clock signal is applied at the EV kit CLK SMA connector. Upon starting the program, the EV kit software searches for the DS89C40 microcontroller interface circuit. The software then reads the ADC's registers (0x00 to 0x10), updates the software GUI in the **Input/Output/Clock** and **Power Management** tab sheets, and places the register contents (in hex format) next to their respective **Reg00-Reg10** register designators.

User-Interface Panel

The program's main window contains two tabs, **Input/Output/Clock** (Figure 1) and **Power Management** (Figure 2), which provide controls for the ADC's software-configurable features. The **Input/Output/Clock** tab sheet provides group box controls for **Output Format**, **LVDS Output Adjustments**, **Input Common Mode Voltage**, and **System Timing**. The **Power Management** tab sheet provides controls for power management.

Changes to the controls result in a write operation that updates the appropriate registers of the ADC. The registers are automatically read after each write operation to verify data sent. Additionally, a **ReadRegs** button is available to read all the ADC registers and to update the main window Reg00–Reg10 register designators. For reference, a list of registers and their content (in hex format) is provided in a column on the right side of the program's main window.

The **Reset** button resets the ADC registers to their power-on-default state.

The bottom status bar of the main window provides the communication status of the EV kit microcontroller interface circuitry. The **Address** and **Data** labels display the last register address written to and its corresponding data, respectively.

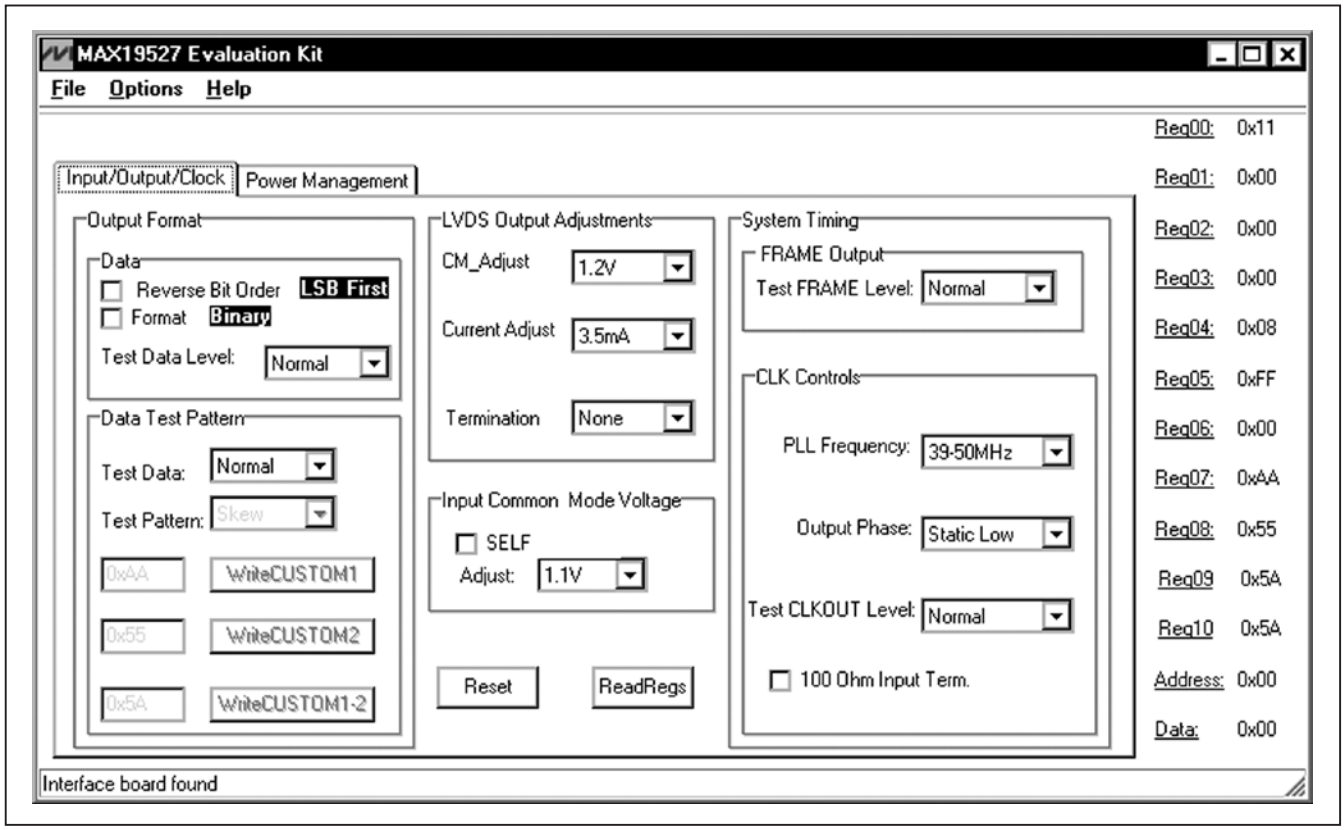

Figure 1. MAX19527 EV Kit Software (Input/Output/Clock Tab)

Input/Output/Clock Tab

Output Format

The **Output Format** group box contains several functions that format the output data.

The **Reverse Bit Order** checkbox allows the user to change the LVDS output data to a MSB-first format and displays the bit-order configuration. The **Format** checkbox configures the output data format to binary or two's complement, and displays the current data format. The **Test Data Level** drop-down list gives the user the option of configuring the ADC's OUT1–OUT8 channels to display the normal LVDS data outputs, or setting the channel's outputs to a static high or low state.

Data Test Pattern

The **Test Data** drop-down list gives the user the option to choose between normal and test data modes. Select **Normal** from the drop-down list to operate the LVDS outputs under normal conditions. In normal operation, all GUI functions in the **Data Test Pattern** group box (with the exception of the **Test Data** drop-down list) are disabled. When **Pattern** is selected, all GUI functions in the **Data Test Pattern** group box become active.

The **Test Pattern** drop-down list allows the user to choose between several test patterns for data-timing alignment. Selecting **Normal** from the **Test Data** drop-down list configures the test pattern channels according to the option selected in the **Test Data Level** drop-down list. Selecting **Pattern** from the **Test Data** drop-down list allows the user to generate factory test and custom patterns at the output channels. See Table 2 for generating the IC test patterns.

Three buttons (**WriteCUSTOM1**, **WriteCUSTOM2**, and **WriteCUSTOM1-2**) and their respective edit boxes also become active when **Pattern** is selected from the **Test Data** drop-down list. The buttons are available for loading customized 8-bit test patterns in the ADC's 0x07, 0x08, and 0x09 registers. The registers are updated by pressing the **WriteCUSTOM1**, **WriteCUSTOM2**, or **WriteCUSTOM1-2** buttons.

LVDS Output Adjustments

The **LVDS Output Adjustments** group box contains controls to set the channel OUT1–OUT8 common-mode output voltage, output current, and back termination. The **CM_Adjust** drop-down list sets the output driver's common-mode voltage. The **Current Adjust** drop-down list sets the output driver's current. The **Termination** drop-down list sets the termination resistance.

Input Common-Mode Voltage

When checked, the **SELF** checkbox applies a common-mode voltage to the ADC's IN_+/IN_- input pins and disables the common-mode input pins when not selected. The **Adjust** drop-down list sets the common-mode voltage according to the value selected. The selected common-mode voltage can be monitored through the CMOUT test point. When enabling **SELF**, verify that shunts are not installed on jumpers JU1–JU8

System Timing

The **Test FRAME Level** drop-down list gives the user the option of configuring the ADC's FRAME LVDS output channel to display the normal FRAME output frequency (identical to input clock frequency), or setting the FRAME output to a static high or low state.

The **CLK Controls** group box contains controls for manipulating the input clock signal. The **PLL Frequency** drop-down list programs the clock multiplier for the internal PLL in order to set the sampling frequency range. Ensure that the input clock frequency, applied at the EV kit CLK SMA connector, falls between the selected minimum and maximum frequency in the drop-down list.

The **Output Phase** drop-down list adjusts the phase of the serial LVDS output clock (CLKOUT), relative to the output data frame. Refer to the timing diagrams in the MAX19527 IC data sheet for additional information.

The **Test CLKOUT Level** drop-down list gives the user the option of configuring the ADC's CLKOUT LVDS output channel to display the normal CLKOUT signal, or setting the output signal to a static high or low state.

The **100 Ohm Input Term** checkbox switches 100Ω across differential clock inputs when checked.

Table 2. Test Pattern Selection

TEST PATTERNS	OUTPUT
Skew	(010101010101) → repeats every frame
SYNC	(111111000000) → repeats every frame
Custom	Custom test pattern → repeats every two frames
Ramp	12-bit ramp from 0 to 4095 and repeats
Pseudo9	Pseudorandom data pattern (short 2^9 sequence)
Pseudo23	Pseudorandom data pattern (long 2^{23} sequence)

Refer to the *System Timing Requirements* section in the MAX19527 IC data sheet for additional information for configuring the Data, FRAME, and CLKOUT test levels.

Power Management Tab

Power Management Controls

The **Power Management** group box contains two sets of controls. The first set is used only when the SHDN pin on the EV kit is set low and the second set is used only when the SHDN pin on the EV kit is set high. When checked, the **IN1 Active–IN8 Active** checkboxes enable the input channel, or disable the input channel when left unchecked. The **Sleep/Nap Mode** checkbox toggles between nap mode when checked and sleep mode when unchecked, as long as the **IN1 Active–IN8 Active** checkboxes are left unchecked. The **Enable All** and **Disable All** buttons are available to enable and disable all input channels simultaneously. For more details on power management, refer to the MAX19527 IC data sheet.

Advanced User Interface

A serial interface can be used by advanced users by selecting the **Options | Interface (Advanced Users)** menu item. Custom bit-banging firmware commands are used to implement a bidirectional SPI interface. Read addresses always begin with 0x8_ and write addresses always begin with 0x0_.

For writing to registers, click on the **Connection** tab (Figure 3). Enter the raw command bytes value of **0x77 0x05 0xA0 0xA0** (where 0x05 is the register write address in hexadecimal, and 0xA0, 0xA0 are the data in this example), then press the **Send raw command bytes** button. Note that the custom firmware uses data transfer of two bytes.

For reading registers, enter the raw command bytes value of **0x72 0x85** (where 0x85 is the register read address in hexadecimal), then press the **Send raw command bytes** button. The register address and content are displayed as the first and second byte of data listed under the **Returned data [hexadecimal]** label, respectively (Figure 4).

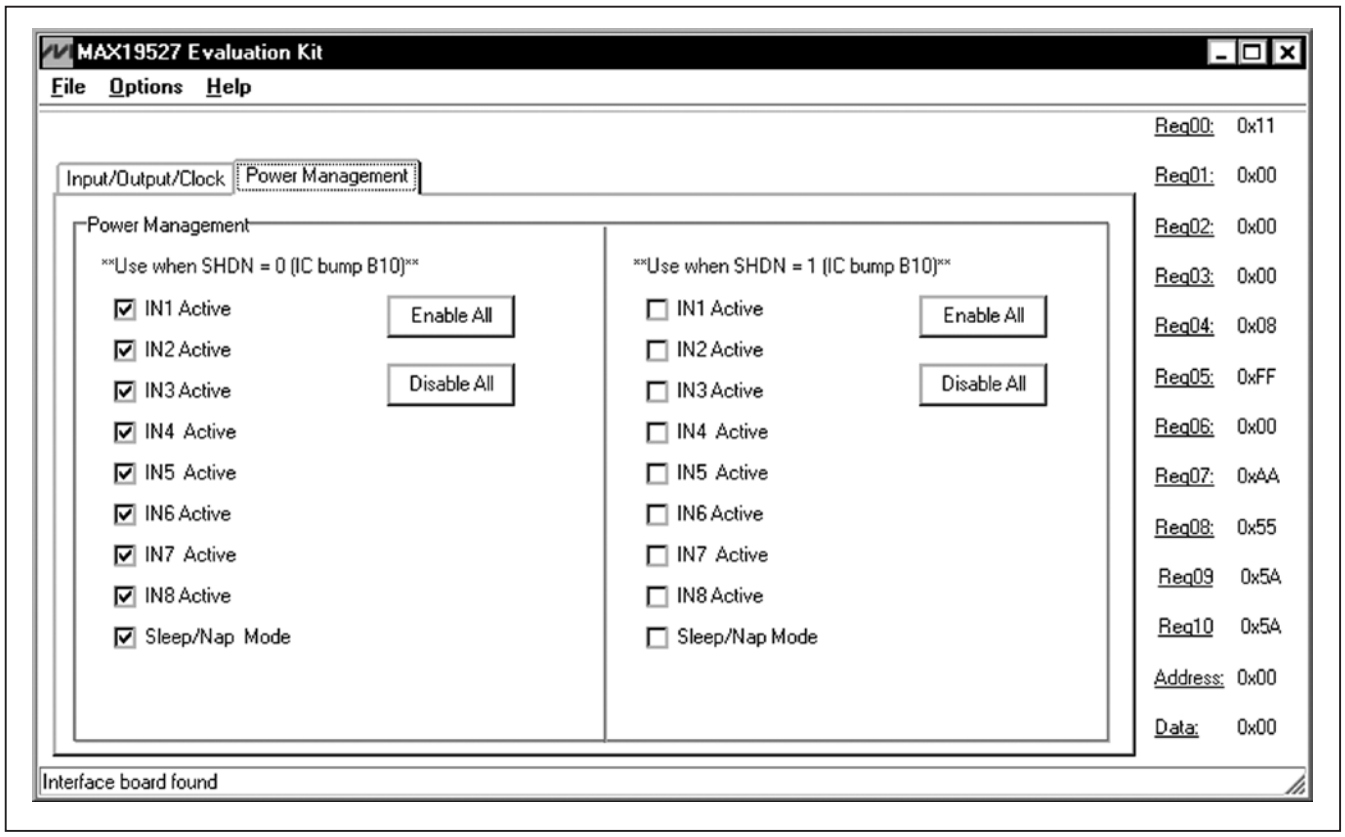

Figure 2. MAX19527 EV Kit Software (Power Management Tab)

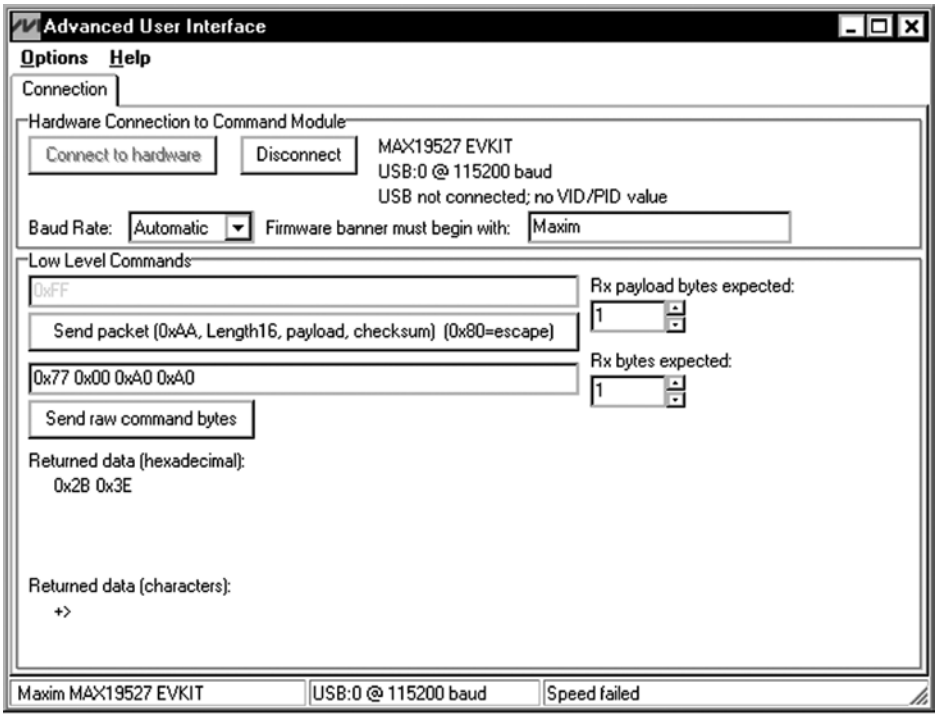

Figure 3. Advanced User Interface Window (3-Wire Interface Tab)—Writing to a Register

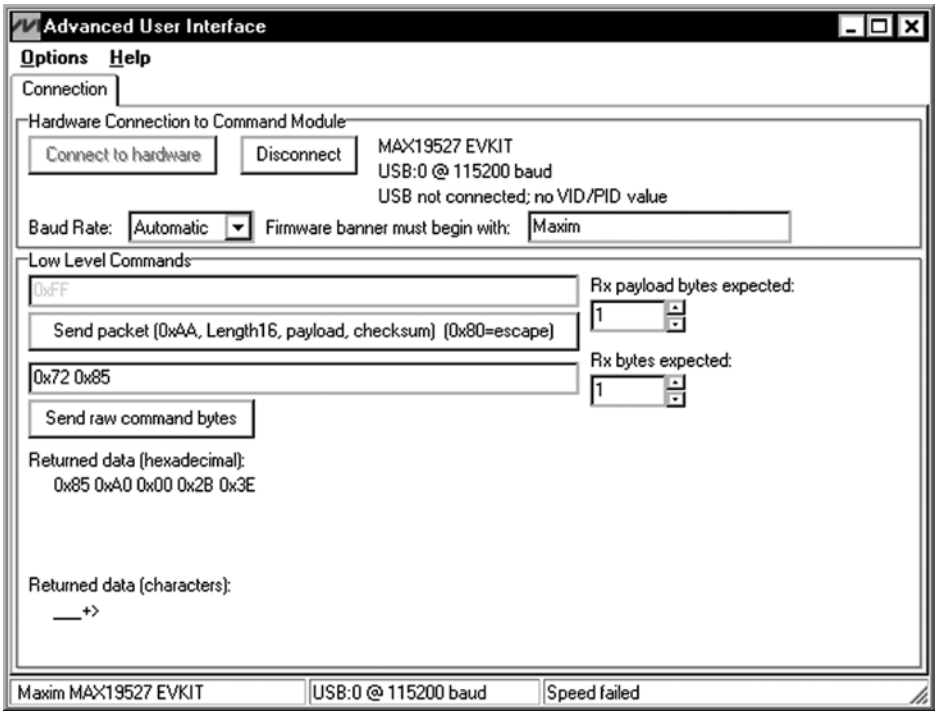

Figure 4. Advanced User Interface Window (3-Wire Interface Tab)—Reading a Register

Keyboard Navigation

Press Ctrl + Tab to navigate to the tab sheets. The selected tab sheet is indicated by a dotted outline. Press the Tab key to select each GUI control. The selected control is indicated by a dotted outline. Using Shift + Tab moves the selection to the previously selected control. Buttons respond to the keyboard's space bar and some controls respond to the keyboard's up and down arrow keys. Activate the program's menu bar by pressing the F10 key and then press the letter of the desired menu item. Most menu items have one letter underlined, indicating their shortcut key.

When a number is entered into the edit boxes, it can be sent to the device by pressing the Enter key. The data is also sent when Tab or Shift + Tab is pressed.

Detailed Description of Hardware

The MAX19527 EV kit is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX19527 50Msps octal, 12-bit ADC.

The ADC accepts differential input signals; however, on-board transformers (T1–T8) convert the single-ended signals applied to the IN1–IN8 SMA connectors to the required differential signals. The input signals of the ADC can be measured using a differential oscilloscope probe at header J1. The ADC's digital LVDS output signals are accessible at header H2. Output drivers (U4, U5, and U6) are used for buffering the LVDS output signals when interfacing the EV kit to the DCEP board.

The EV kit can be configured for communicating to the SPI interface using the on-board USB circuitry or a user-supplied external 3-wire controller using jumpers JU11 JU12, and JU13.

The EV kit is designed as a six-layer PCB to optimize the performance of the ADC. Separate analog, digital, and buffer power planes minimize noise coupling between analog and digital signals. The analog and clock inputs and the LVDS outputs use 100Ω differential microstrip transmission lines. All singled-ended digital outputs use 50Ω microstrip transmission lines. The trace lengths of the 100Ω differential LVDS output lines are matched to within a few thousands of an inch to minimize layout-dependent output-signal skew.

Power Supplies

The EV kit operates from a single 3.3V DC power supply applied at the +3.3V and GND PCB pads and provides on-board regulation to power the IC analog and digital circuit blocks, and the MAX9392 LVDS buffers.

The analog circuit block (AVDD) is regulated to 1.8V using the MAX8902A (U2). To power the analog circuit using the EV kit circuitry, install a shunt on jumper JU14. To disconnect the 1.8V power source, remove the shunt at JU14. See Table 3 for proper JU14 configuration.

The digital circuit block (OVDD) is regulated to 1.8V using the MAX8902A (U3). To power the digital circuit using the EV kit circuitry, install a shunt on jumper JU15. To disconnect the 1.8V power source from OVDD, remove the shunt on JU15. See Table 4 for proper JU15 configuration.

Jumpers JU14 and JU15 are provided to disconnect the power sources or to measure current through AVDD and OVDD, respectively.

Clock Input

The data converter allows either differential or single-ended signals to drive the clock inputs. The EV kit supports both methods.

In single-ended operation, the clock signal is applied at the CLK SMA connector and connects to the ADC through a buffer (U7). In differential mode, an on-board transformer converts a user-supplied single-ended analog input and generates a differential analog signal, which is then applied to the ADC's input pins. The clock signal applied to the ADC can be observed at header J2.

Table 3. AVDD Input Power Configuration (JU14)

SHUNT POSITION	AVDD (V)
Installed*	1.8V LDO (U2) powers the AVDD input
Not installed	Power disconnected from the AVDD input

**Default position.*

Table 4. OVDD Input Power Configuration (JU15)

SHUNT POSITION	OVDD (V)
Installed*	1.8V LDO (U3) powers the OVDD input
Not installed	Power disconnected from the OVDD input

**Default position.*

Configuring the EV Kit for Single-Ended Clock Operation

To configure the EV kit for single-ended clock operation, the following modifications must be made to the clock circuit:

1) Cut the traces at locations R99, R103, and R104.
2) Install 0Ω resistors at locations R96, R102, and R105.
3) Install a 49.9Ω ±1% resistor at location R98.

In single-ended clock configuration, potentiometer R94 can be utilized to control the duty cycle of the clock input signal. Measure the clock input at header J2 and adjust R94 until the desired duty cycle is achieved.

Input Signals

Although the ADC accepts differential analog input signals, the EV kit only requires single-ended analog input signals. Insertion losses due to a series-connected filter and the interconnecting cables decrease the amount of power seen at the EV kit input. Account for these losses when setting the signal generator amplitude. On-board transformers (T1–T8) convert the single-ended analog input signals and generate the recommended differential analog signals at the ADC's differential input pins.

Jumpers JU1–JU8 are available to provide a common-mode voltage to the EV kit input circuit networks when jumper JU10 is installed. JU10 supplies the programmed common-mode voltage supplied by the ADC's CMOUT output. Install a shunt on JU10 and the respective IN_ channel jumpers to set the input network common-mode voltage. See Table 5 for proper jumper configuration.

Output Signals

The ADC features eight 12-bit, serial, LVDS digital outputs (OUT_) that transmit the converted differential analog input signals (IN1–IN8). Two additional outputs (CLKOUT and FRAME) are provided for system timing. Refer to the *System Timing Requirements* section in the MAX19527 IC data sheet for additional information.

Output Termination

The ADC features trimmed, selectable internal termination resistors between the positive and negative line of each output (OUT1–OUT8, CLKOUT, and FRAME). The EV kit circuit also features 100Ω termination resistors for the ADC output, located at the inputs of the MAX9392 LVDS crosspoint switches (U4, U5, and U6). MAX9392 ICs are used to buffer the ADC's outputs when connecting the DCEP board to the EV kit, which allows monitoring of the output signals at header H2.

SPI Interface Control

The EV kit communicates to the ADC's SPI interface using the on-board USB circuitry or external 3-wire signals (applied at header J10).

Place shunts across pins 1-2 of jumpers JU11, JU12, and JU13 to control the SPI interface using the USB circuitry. Remove shunts from JU11, JU12, and JU13 when using external 3-wire signals at header J10. See Tables 6, 7, and 8 for proper JU11, JU12, and JU13 configuration, respectively.

Table 5. IN_ Common-Mode Input-Voltage Configuration (JU10, JU1–JU8)

SHUNT POSITION		INPUT NETWORKS (IN1–IN8) COMMON-MODE SETTING
JU10	JU1–JU8	
Installed*	Installed*	Input network connected to CMOUT
	Not installed	Input common-mode voltage disconnected from CMOUT
Not installed	X	Input networks disconnected from CMOUT

**Default position.*
X = Don't care

Table 6. SCLK Input Configuration (JU11)

SHUNT POSITION	SCLK PIN	EV KIT FUNCTION
1-2*	Connects to SCLK EV kit level translator circuitry	SCLK signal supplied by USB circuitry
1-3	Connects to ground	Maintains the ADC register's content
1-4	Connects to SCLK DCEP level translator circuitry	For future use
Not installed	Connects to header J10-1	SCLK signal supplied by an external source at header J10

**Default position.*

To maintain the ADC's current register content, place shunts across pins 1-3 of JU11, JU12, and JU13.

Shutdown (SHDN)

The ADC can also be placed in a low-power shutdown mode through jumper JU9. The SHDN pin is a toggle switch between two power-management states, shown in Figure 2 under the **Power Management** group box of the software interface. When a shunt is installed on pins 1-2 of JU9, SHDN is connected to AVDD and the user can select the appropriate settings for inputs **IN1 Active–IN8 Active** and **Sleep/Nap Mode** under the label ****Use when SHDN = 1 (IC bump B10)****. When a shunt is installed on pins 2-3 of JU9, SHDN is connected to GND and the user can select the appropriate settings for inputs **IN1 Active–IN8 Active** and **Sleep/Nap Mode** under the label ****Use when SHDN = 0 (IC bump B10)****. See Table 9 for proper JU9 configuration for shutdown control of the EV kit.

Connecting the DCEP to the EV Kit

The DCEP and EV kit board can be connected using the specified on-board connectors. H1 on the EV kit mates with J5 on the DCEP board. Alternatively, the two boards can be connected with coaxial ribbon cables (Samtec, part no. HQCD-060.00-STR-TBR-1). Note that it is necessary to use either the on-board connectors or cables to obtain a reliable electrical connection between the two boards.

Using the DCEP with the EV Kit

Maxim's DCEP is required for evaluation of this EV kit. An EV kit-specific device module file is required to configure the DCEP software. The most up-to-date device module file can be downloaded from **www.maxim-ic.com/evkitsoftware**. When loading the DCEP device module file, select MAX19527-EVK-xx.dsm and verify that the device module GUI window corresponds to Figure 5. Refer to the *Opening a New Database* section in the Data Converter Evaluation Platform (DCEP) User's Guide for additional information.

Table 7. SDIO Input Configuration (JU12)

SHUNT POSITION	SDIO PIN	EV KIT FUNCTION
1-2*	Connects to SDIO EV kit level translator circuitry	SDIO signal supplied by USB circuitry
1-3	Connects to ground	Maintains the ADC register's content
1-4	Connects to SDIO DCEP level translator circuitry	For future use
Not installed	Connects to header J10-5	SDIO signal supplied by an external source at header J10

**Default position.*

Table 8. $\overline{CS}$ Input Configuration (JU13)

SHUNT POSITION	$\overline{CS}$ PIN	EV KIT FUNCTION
1-2*	Connects to $\overline{CS}$ EV kit level translator circuitry	$\overline{CS}$ signal supplied by USB circuitry EV kit software
1-3	Connects to ground	Maintains the ADC register's content
1-4	Connects to $\overline{CS}$ DCEP level translator circuitry	For future use
Not installed	Connects to header J10-3	$\overline{CS}$ signal supplied by an external source at header J10

**Default position.*

Table 9 SHDN Configuration (JU9)

SHUNT POSITION	SHND PIN	EV KIT FUNCTION
1-2*	Connected to AVDD	Use ****When SHDN = 1 (IC bump B10)**** software GUI box controls
2-3	Connected to GND	Use ****When SHDN = 0 (IC bump B10)**** software GUI box controls

**Default position.*

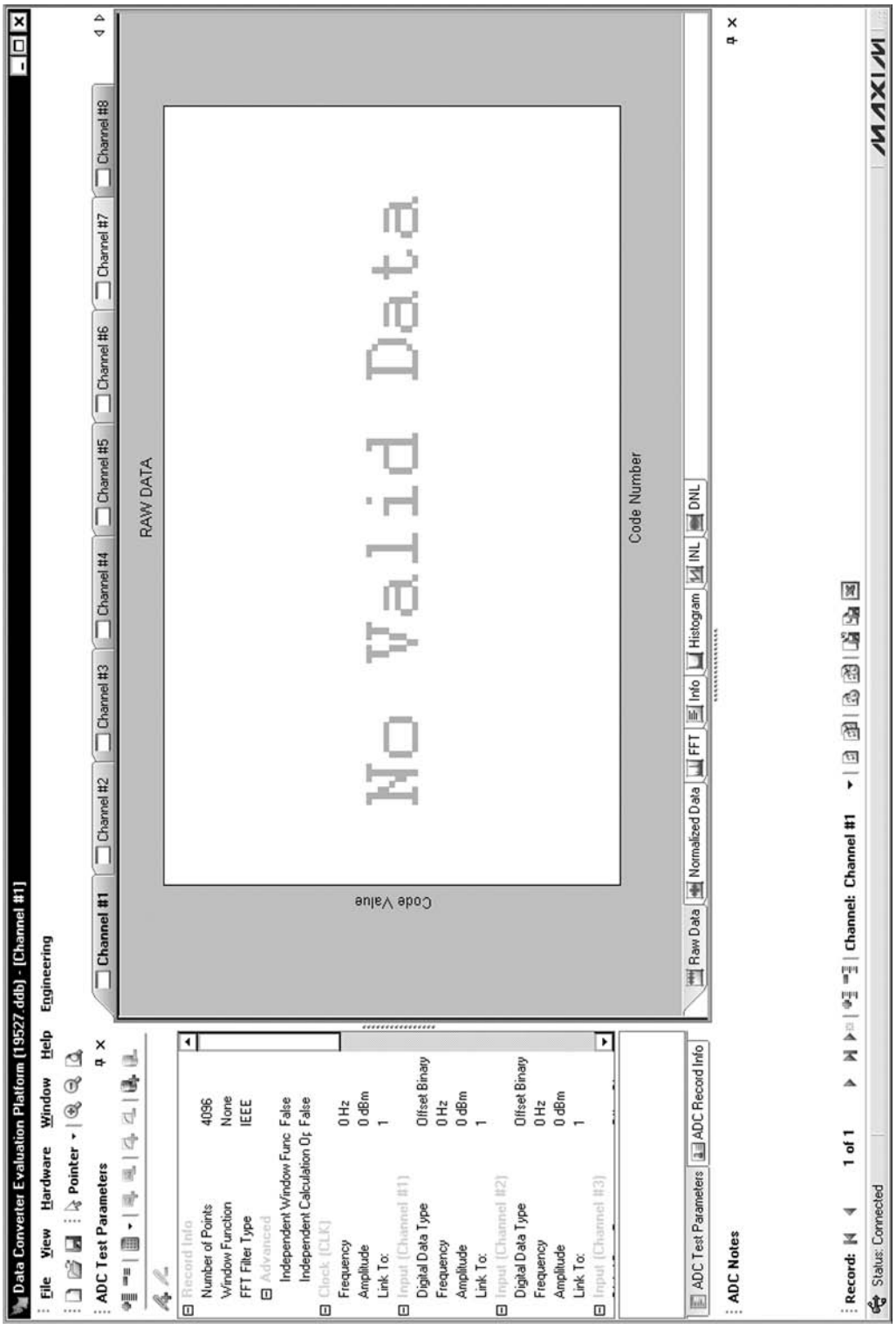

Figure 5. Device Module DCEP GUI Window

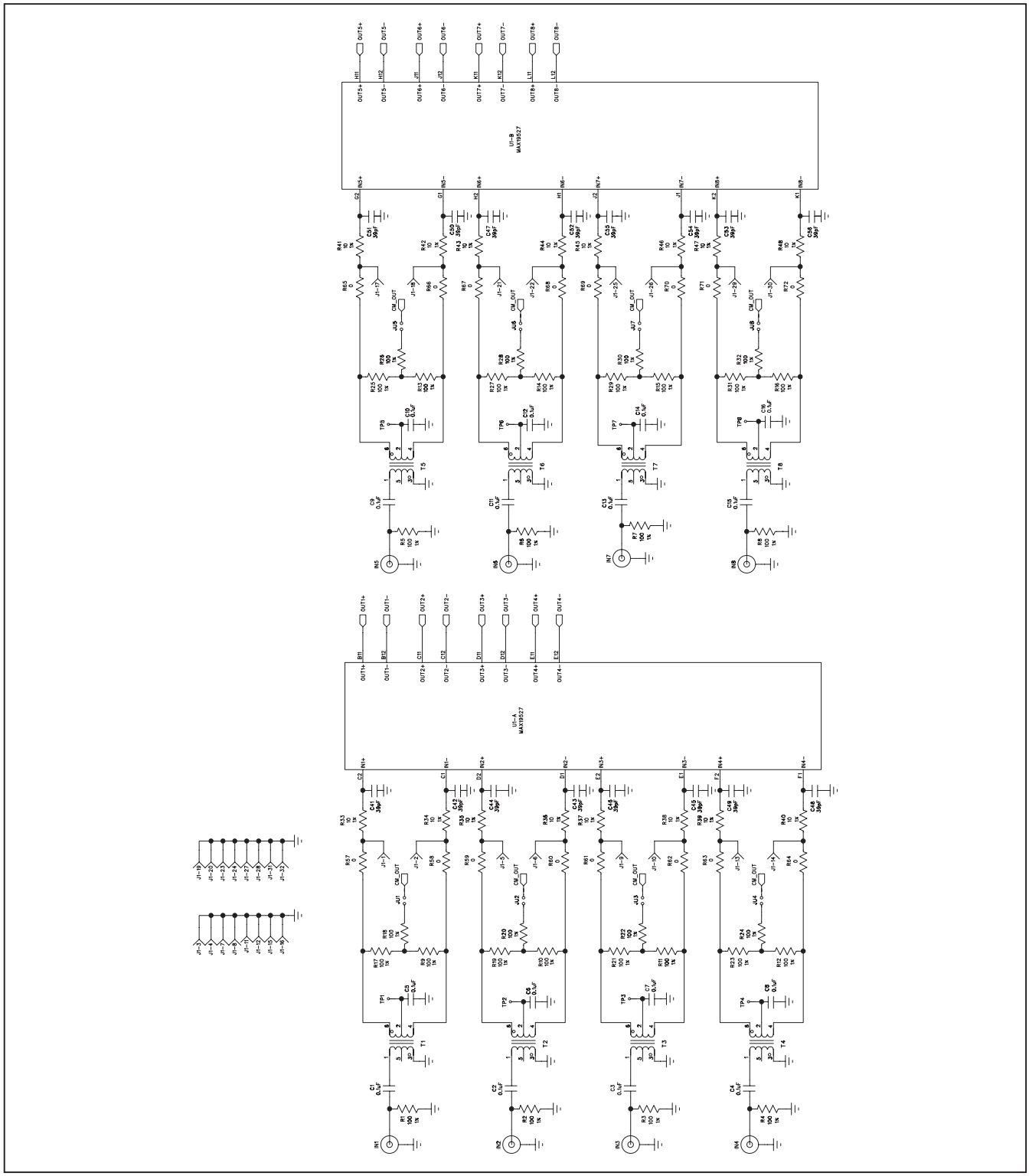

Figure 6a. MAX19527 EV Kit Schematic (Sheet 1 of 4)

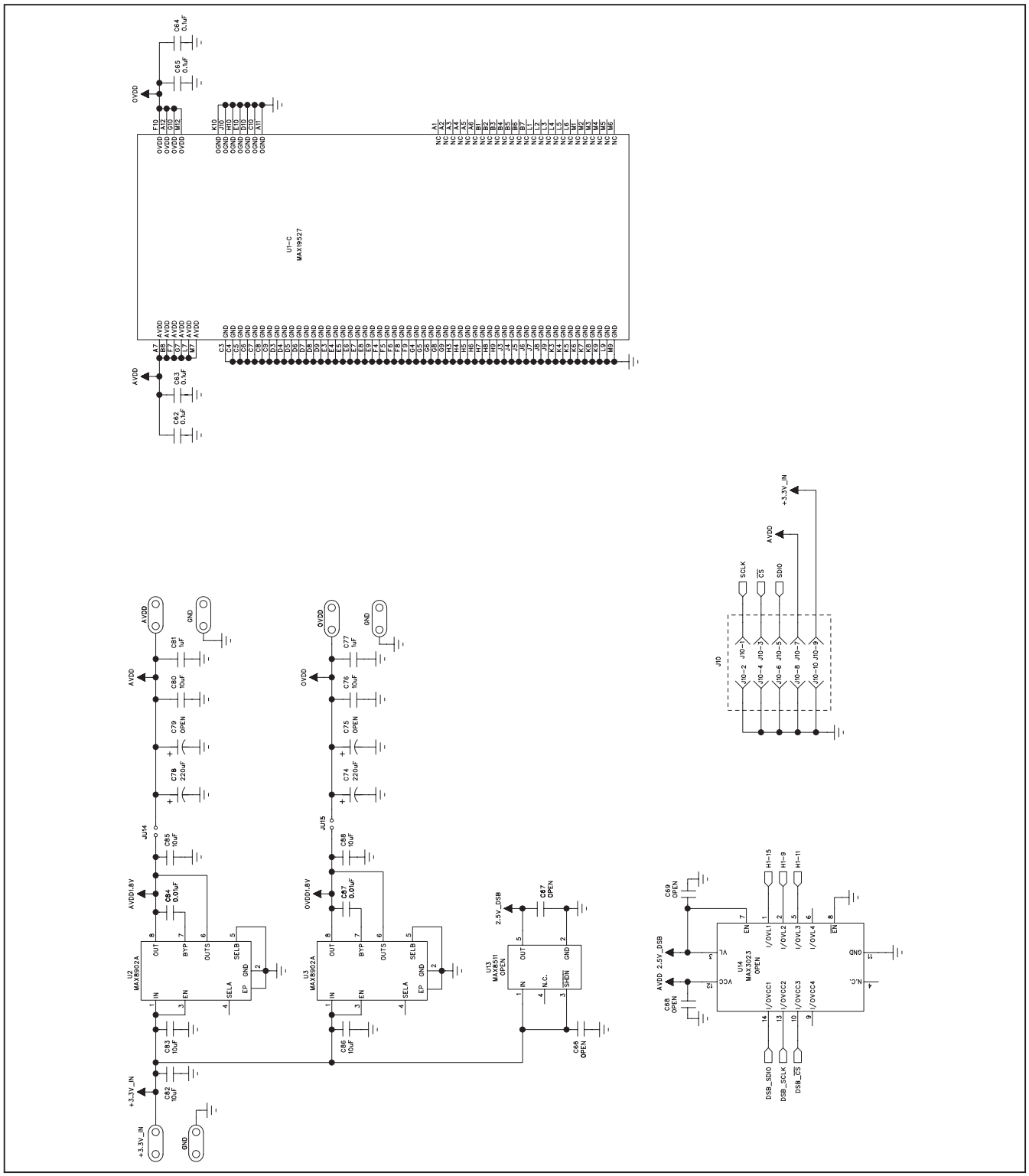

Figure 6b. MAX19527 EV Kit Schematic (Sheet 2 of 4)

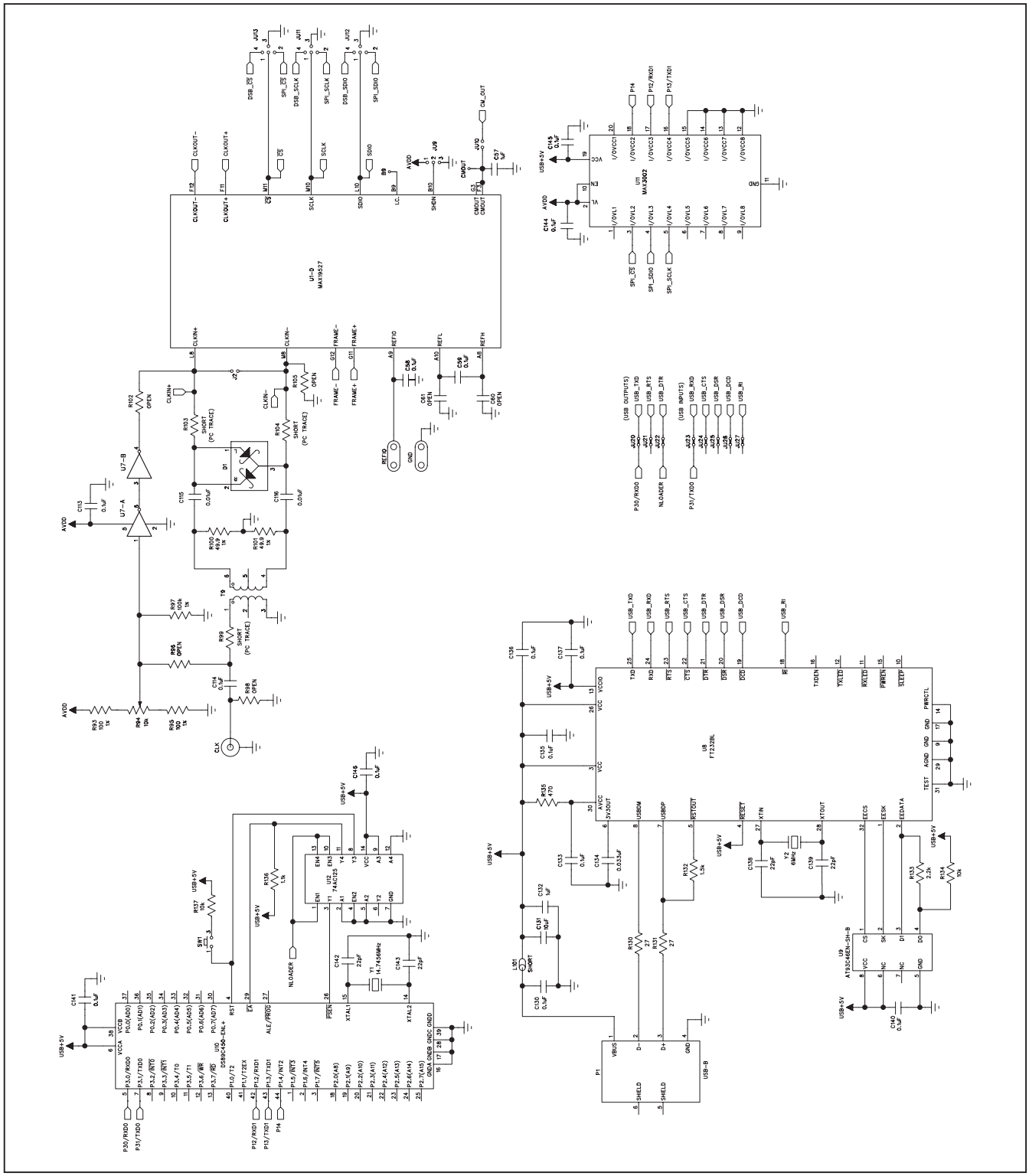

Figure 6c. MAX19527 EV Kit Schematic (Sheet 3 of 4)

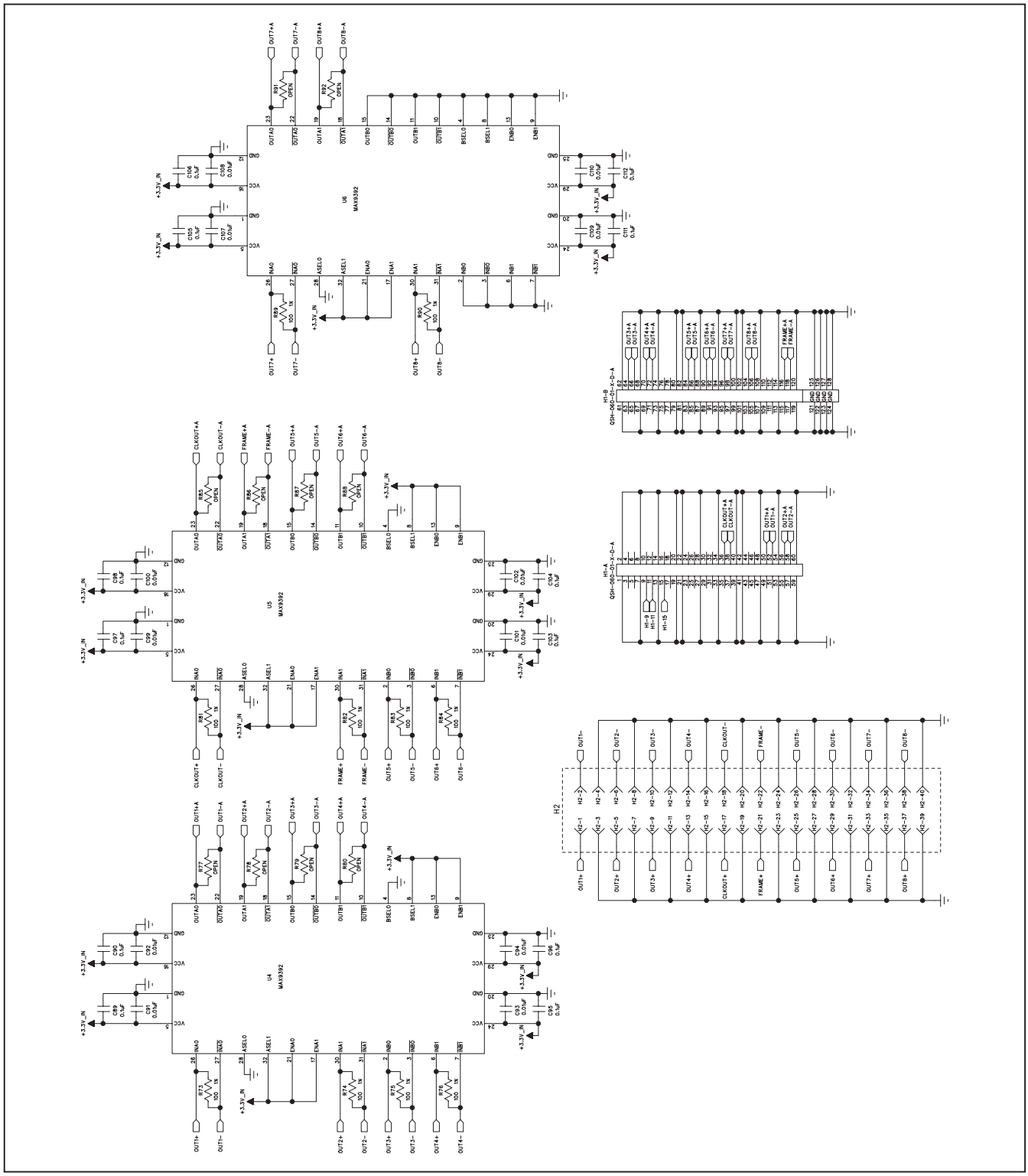

Figure 6d. MAX19527 EV Kit Schematic (Sheet 4 of 4)

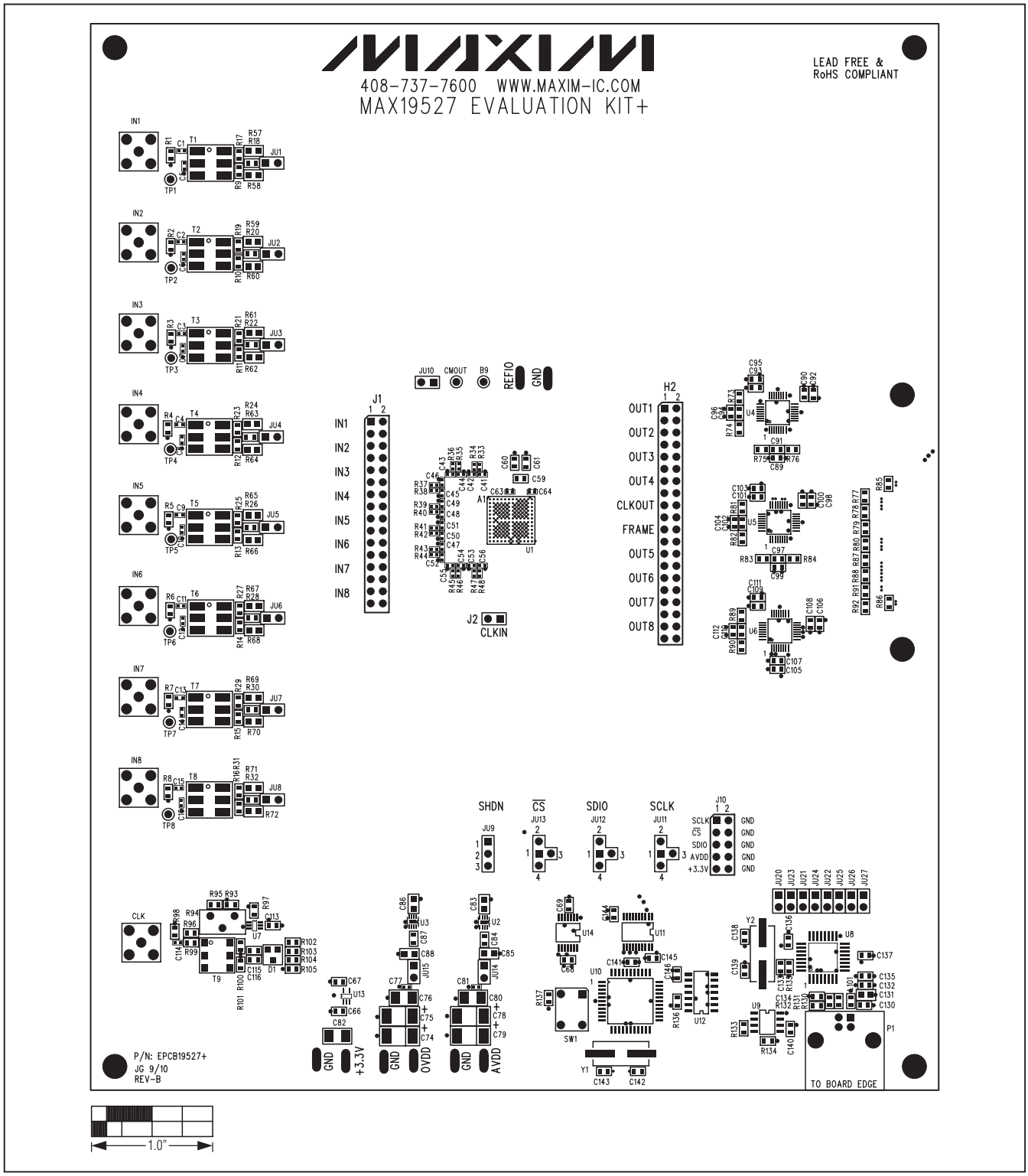

Figure 7. MAX19527 EV Kit Component Placement Guide—Component Side

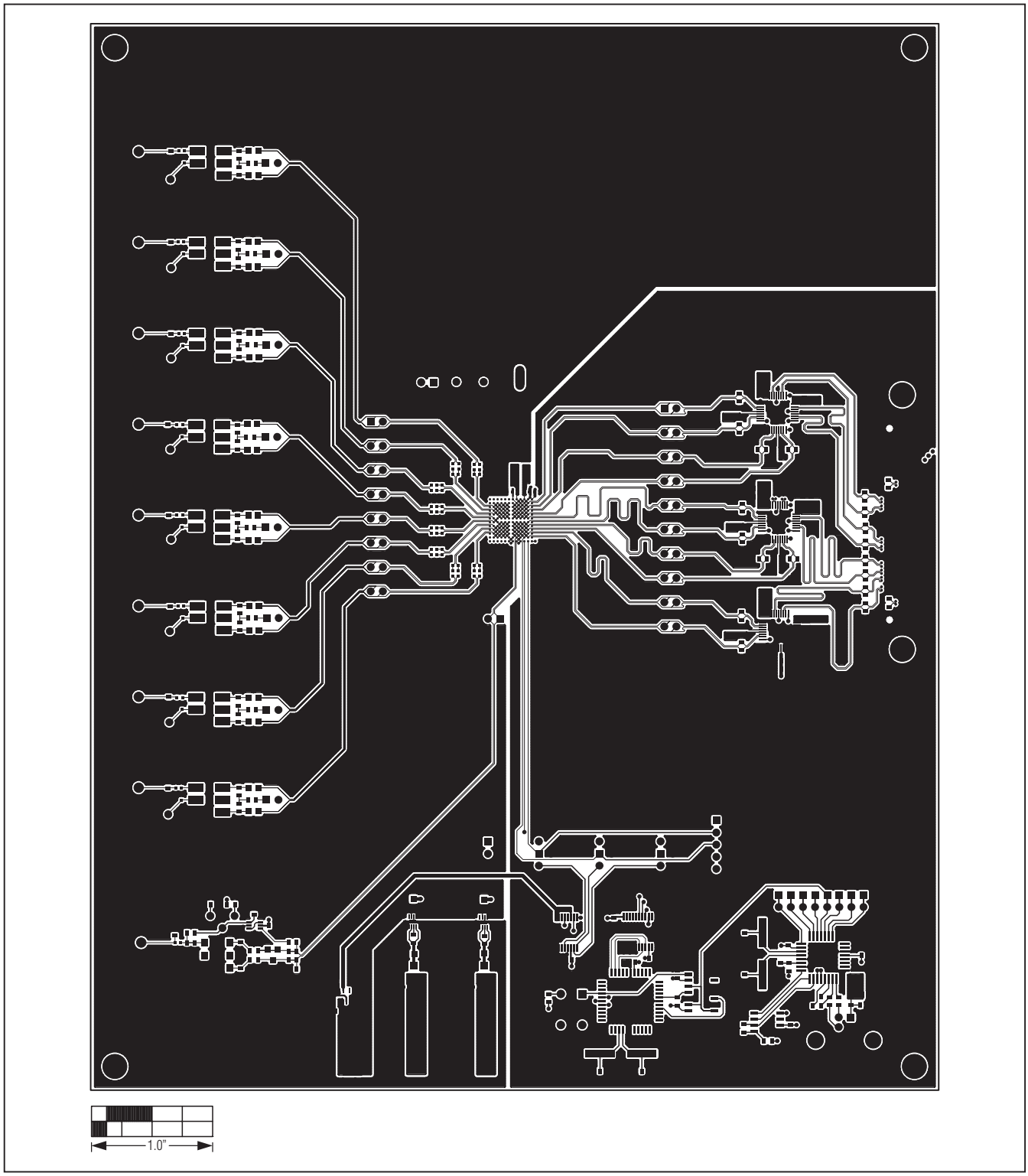

Figure 8. MAX19527 EV Kit PCB Layout—Component Side

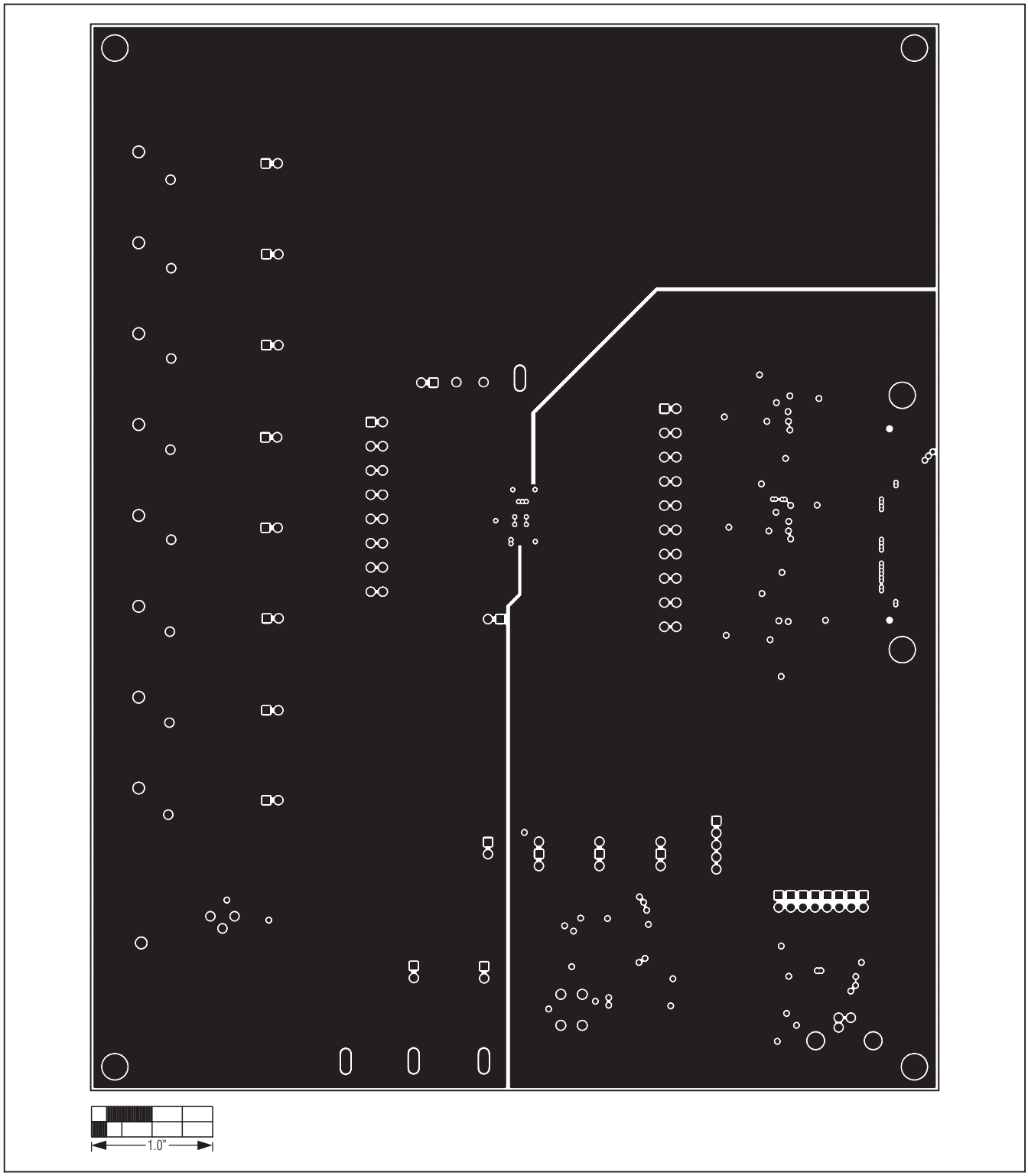

Figure 9. MAX19527 EV Kit PCB Layout (Inner Layer 2)—Ground Planes

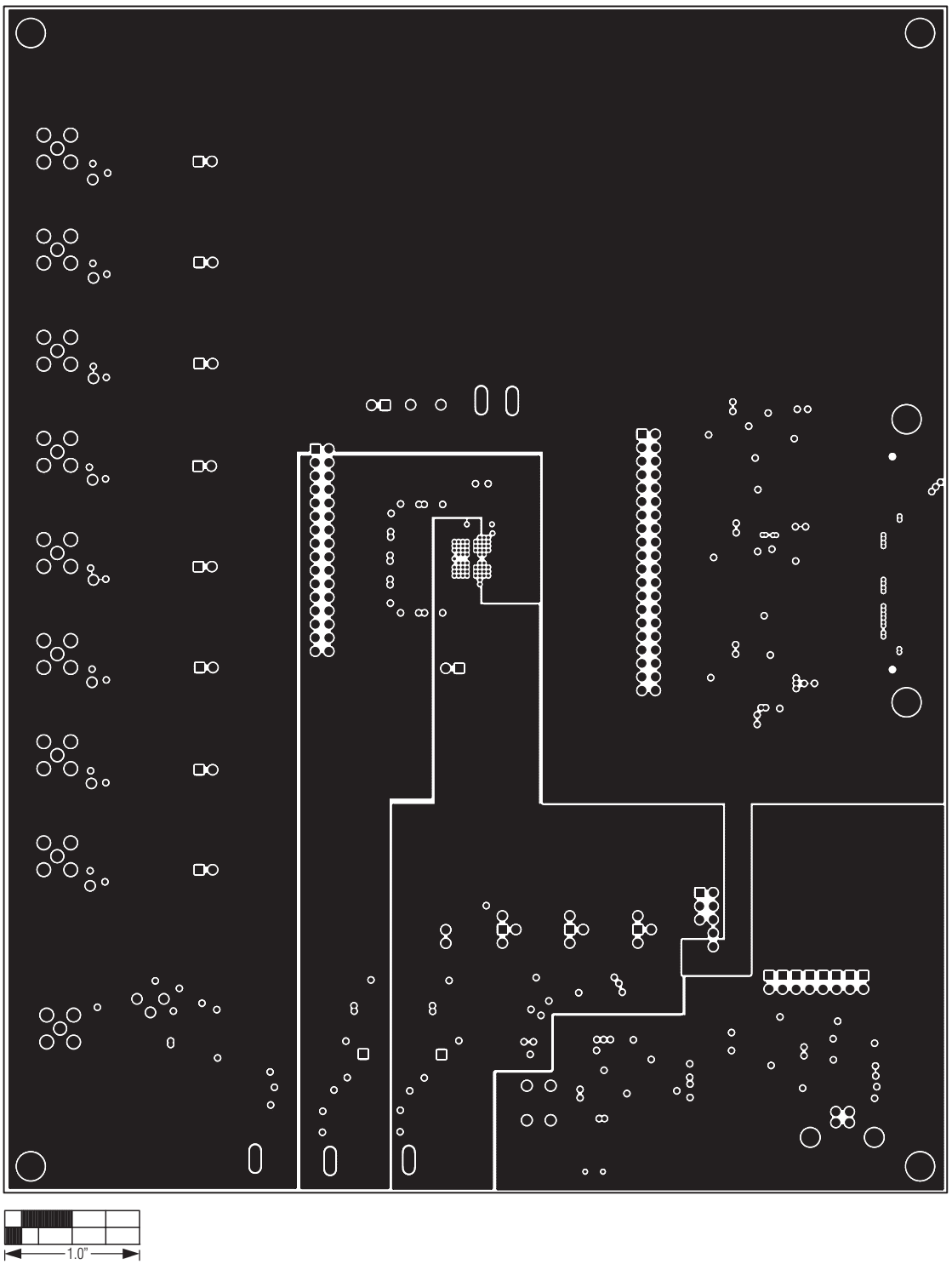

Figure 10. MAX19527 EV Kit PCB Layout (Inner Layer 3)—Power Planes

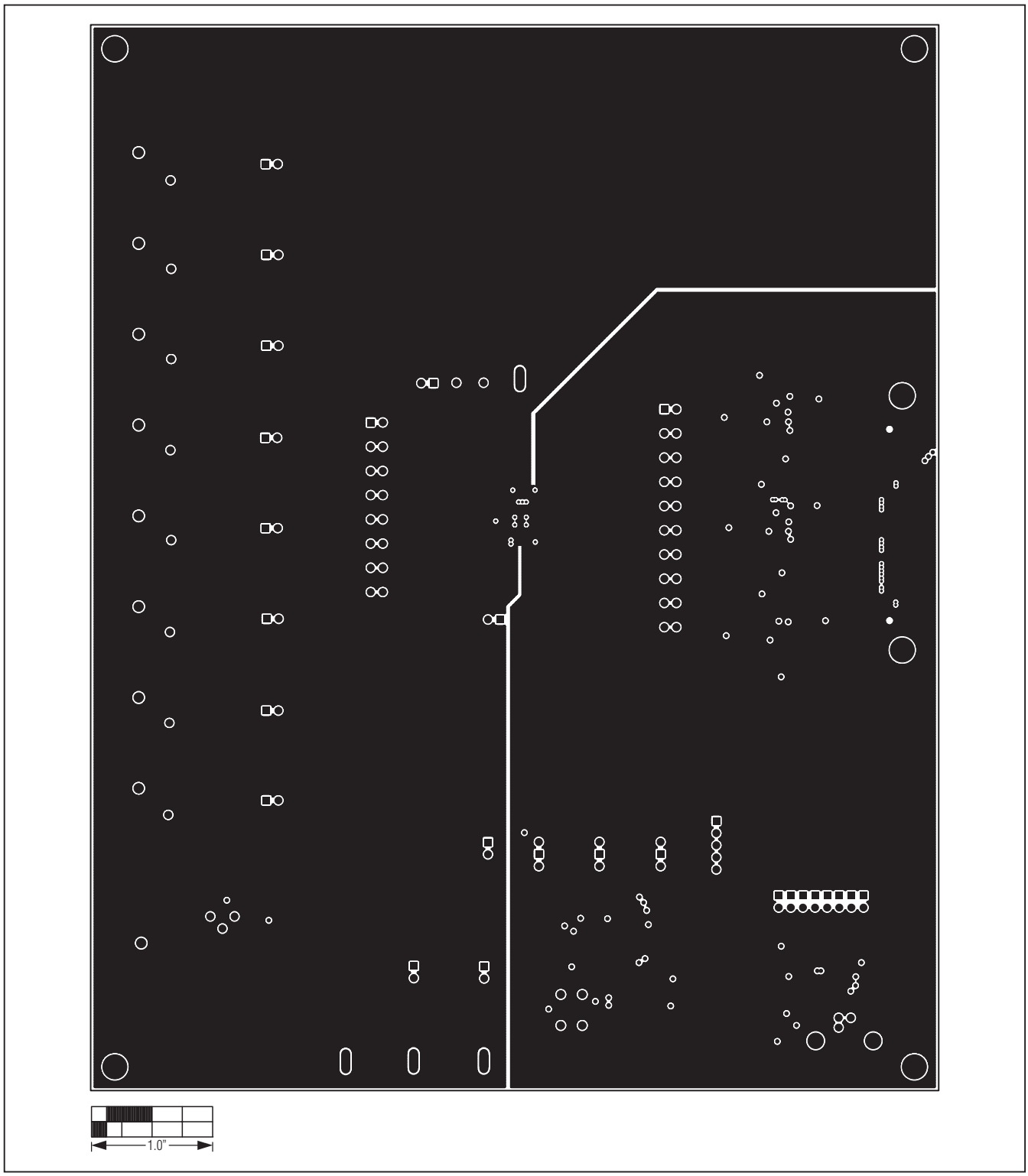

Figure 11. MAX19527 EV Kit PCB Layout (Inner Layer 4)—Ground Planes

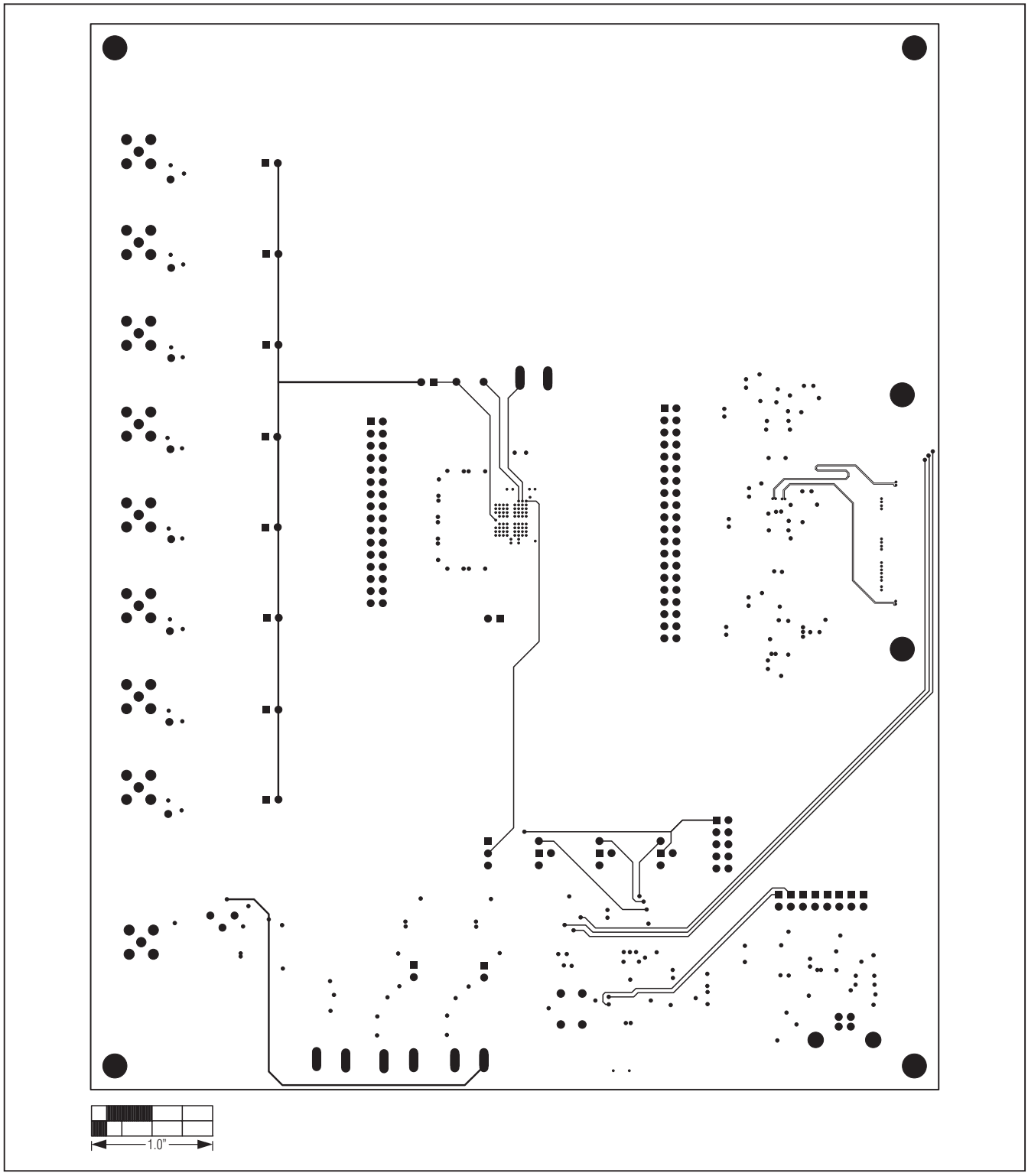

Figure 12. MAX19527 EV Kit PCB Layout (Inner Layer 5)—Routing Plane

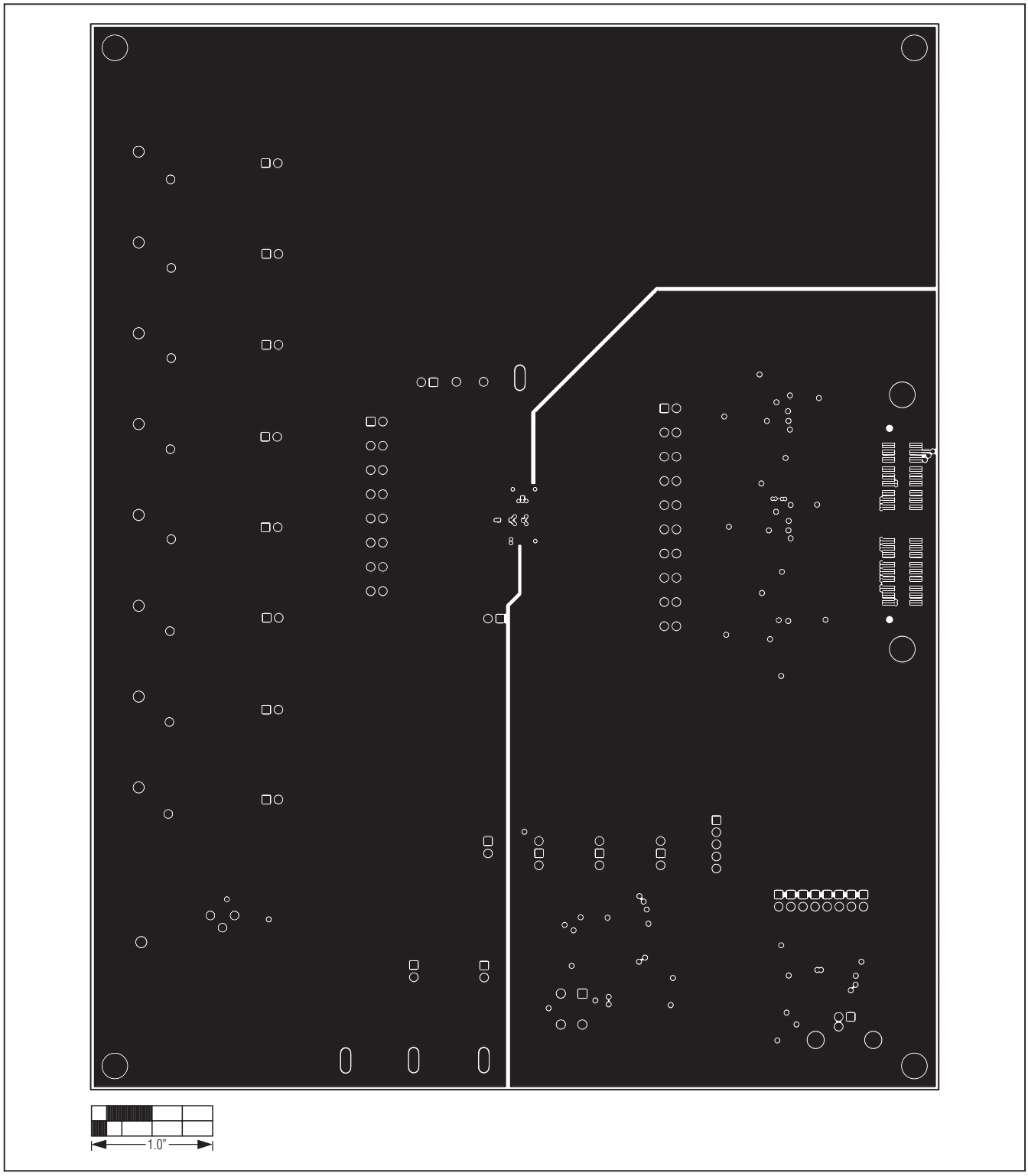

Figure 13. MAX19527 EV Kit PCB Layout—Solder Side

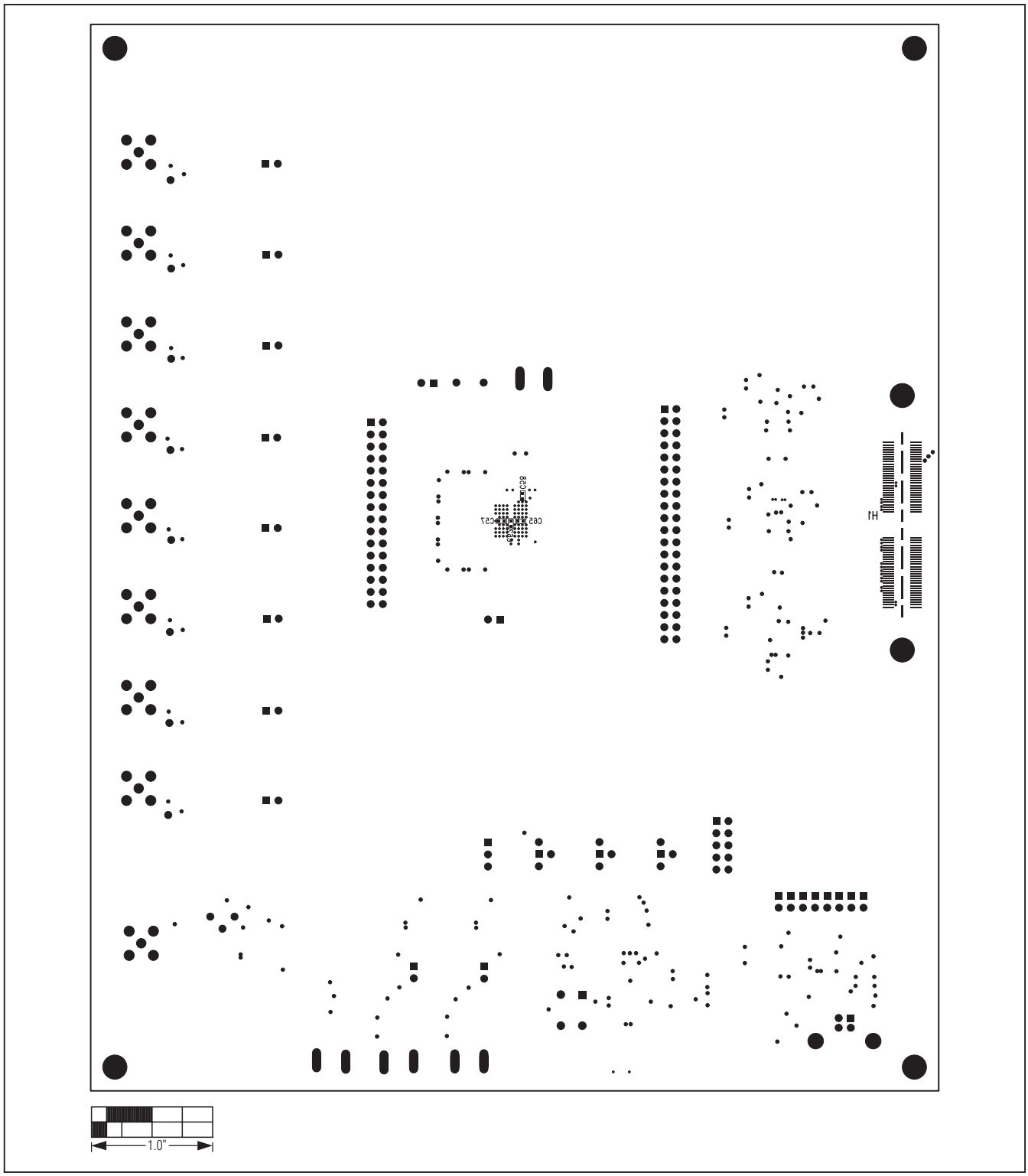

Figure 14. MAX19527 EV Kit PCB Component Placement Guide—Solder Side

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—