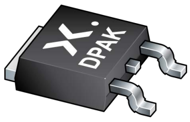


BUK92150-55A

N-channel TrenchMOS logic level FET

12 June 2014 — Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

3. Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

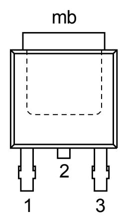
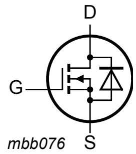
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	55	V
I_D	drain current	$V_{GS} = 5$ V; $T_{mb} = 25$ °C; Fig. 2; Fig. 3		-	-	11	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 1		-	-	36	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 5$ A; $T_j = 25$ °C		-	97	125	mΩ
		$V_{GS} = 5$ V; $I_D = 5$ A; $T_j = 175$ °C; Fig. 11; Fig. 12		-	-	280	mΩ
		$V_{GS} = 4.5$ V; $I_D = 5$ A; $T_j = 25$ °C		-	-	155	mΩ
		$V_{GS} = 5$ V; $I_D = 5$ A; $T_j = 25$ °C; Fig. 11; Fig. 12		-	120	140	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 5$ V; $I_D = 5$ A; $V_{DS} = 44$ V; $T_j = 25$ °C; Fig. 13		-	2.6	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 11 A; V_{sup} ≤ 55 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	16	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 DPAK (SOT428)	
2	D	Drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK92150-55A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428
BUK92150-55A/CD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK92150-55A	9215055A
BUK92150-55A/CD	

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C		-	55	V

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DGR}	drain-gate voltage	R_{GS} 20 kΩ		-	55	V
V_{GS}	gate-source voltage			-15	15	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	36	W
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 5 V; Fig. 2; Fig. 3		-	11	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Fig. 3		-	7.8	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Fig. 2		-	44	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	11	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	44	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 11 A; V_{sup} ≤ 55 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	16	mJ

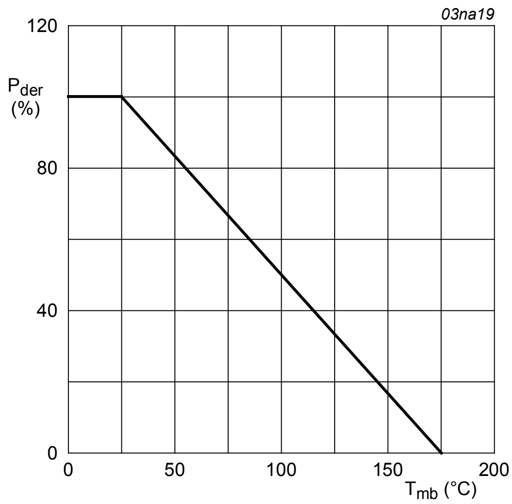


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

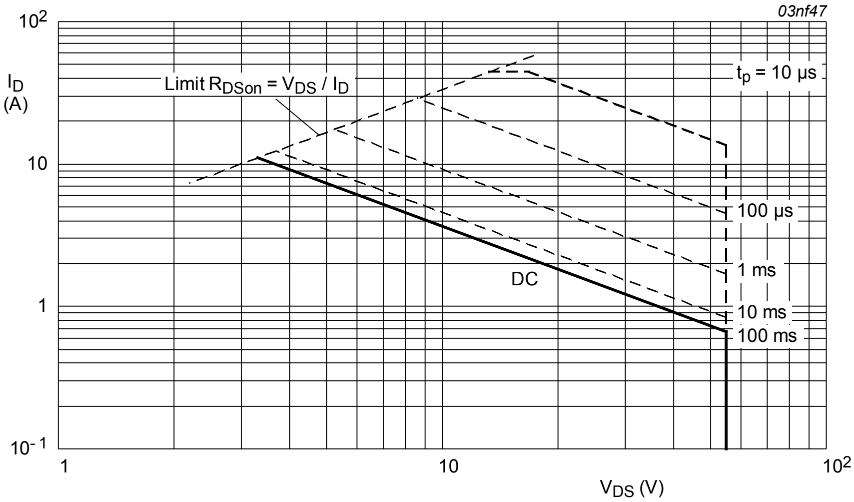


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25°C; I_{DM}$ is single pulse

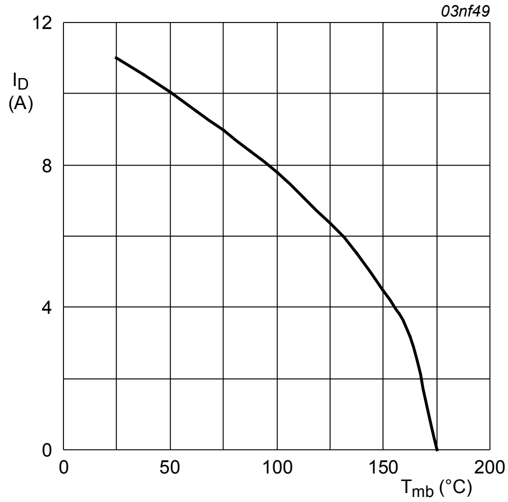


Fig. 3. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 4.5V I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\%$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	-	4.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient			-	71.4	-	K/W

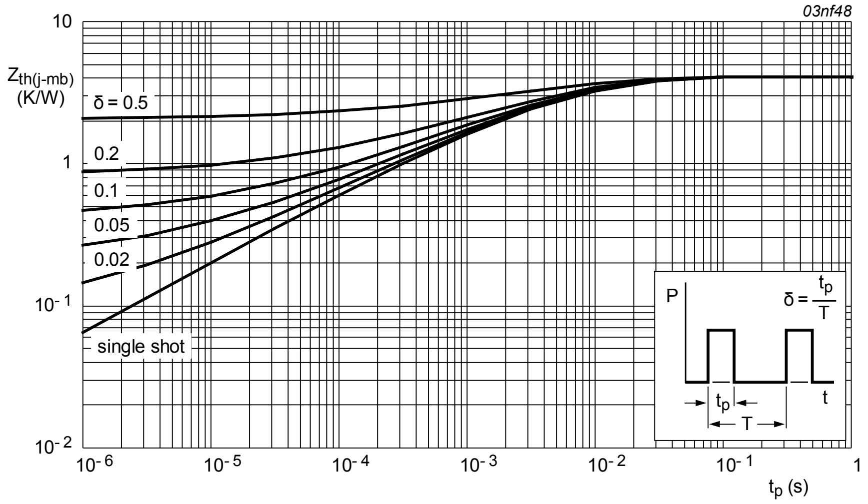


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C		55	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C		50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.3	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 10		1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 10		0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 55 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
		V_{DS} = 55 V; V_{GS} = 0 V; T_j = 25 °C		-	0.05	10	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C		-	97	125	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 175 °C; Fig. 11; Fig. 12		-	-	280	mΩ
		V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C		-	-	155	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; Fig. 11; Fig. 12		-	120	140	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 44 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 13		-	6	-	nC
Q_{GS}	gate-source charge			-	0.76	-	nC
Q_{GD}	gate-drain charge			-	2.6	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	240	338	pF
C_{oss}	output capacitance			-	50	65	pF
C_{rss}	reverse transfer capacitance			-	40	58	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 20 V; R_L = 3.3 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C		-	8	-	ns
t_r	rise time			-	57	-	ns
$t_{d(off)}$	turn-off delay time			-	16	-	ns
t_f	fall time			-	13	-	ns
L_D	internal drain inductance	measured from drain to centre of die; T_j = 25 °C		-	2.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad; T_j = 25 °C		-	7.5	-	nH
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C		-	24	-	ns
Q_r	recovered charge			-	26	-	nC

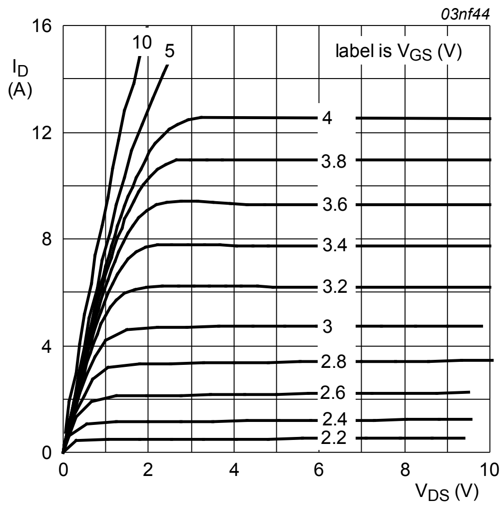


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

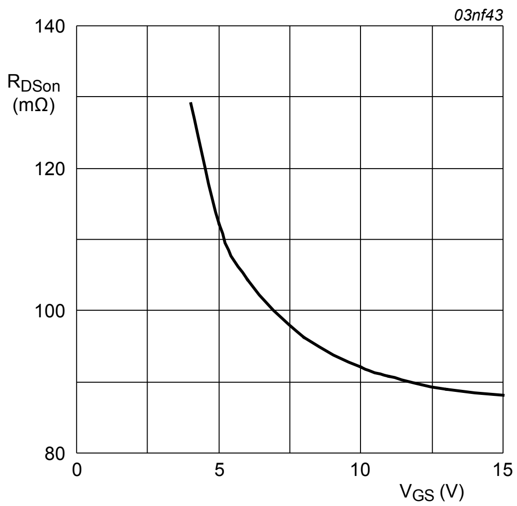
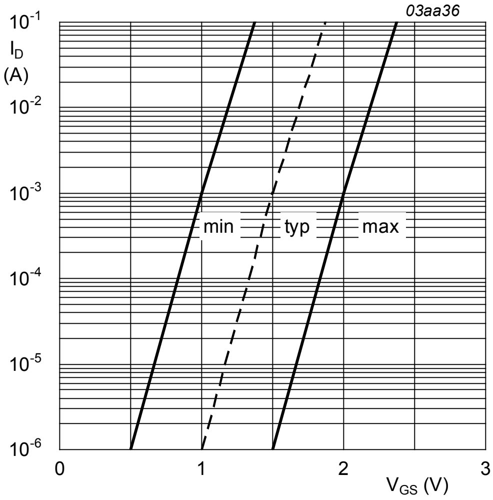


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C; I_D = 5A$



T_j = 25 °C; V_{DS} = 5 V

Fig. 7. Sub-threshold drain current as a function of gate-source voltage

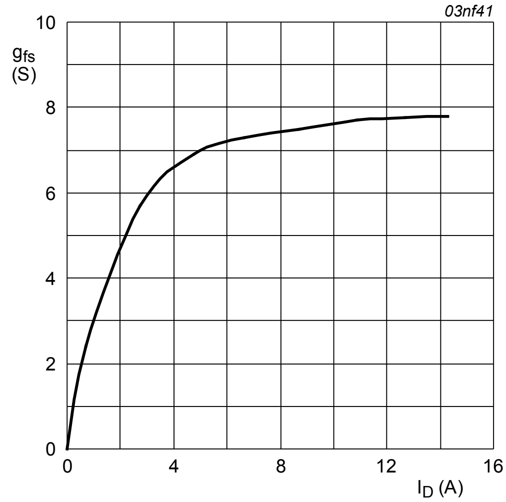


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25\ °C; V_{DS} = 25\ V$

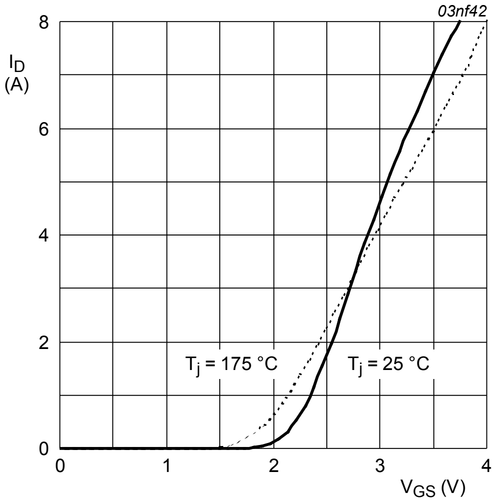


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 25V$

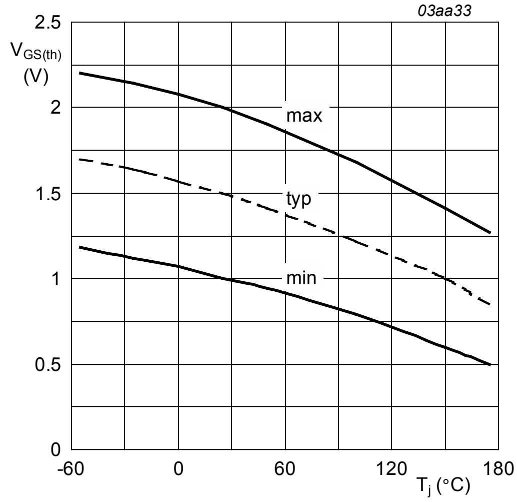


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1mA; V_{DS} = V_{GS}$

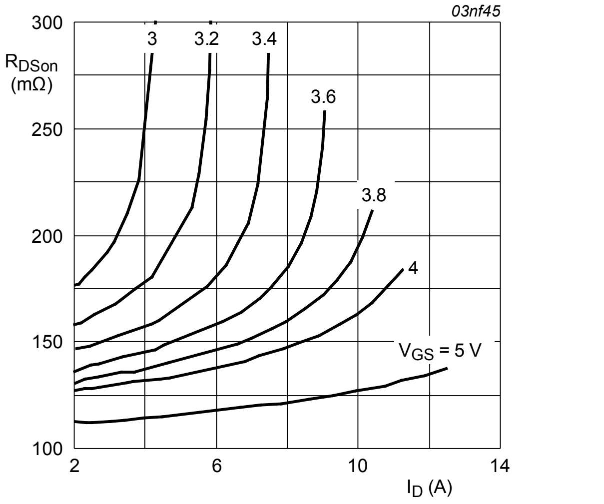


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25°C$$

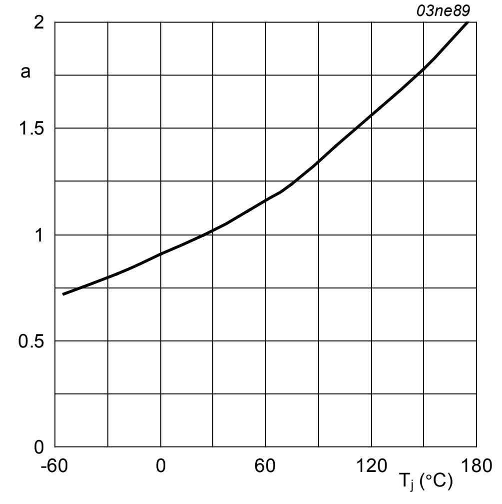


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

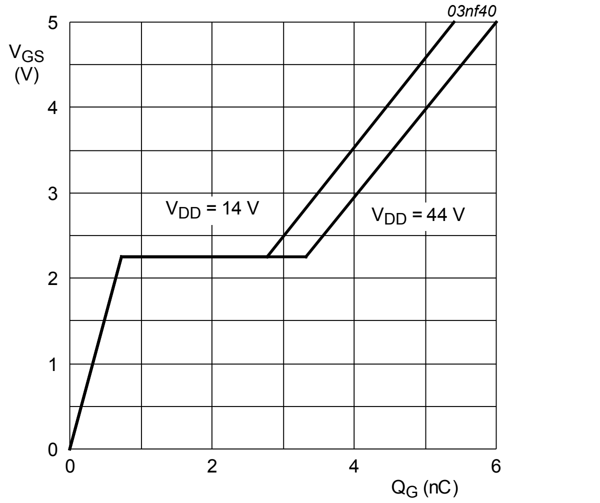


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25°C; I_D = 5A$$

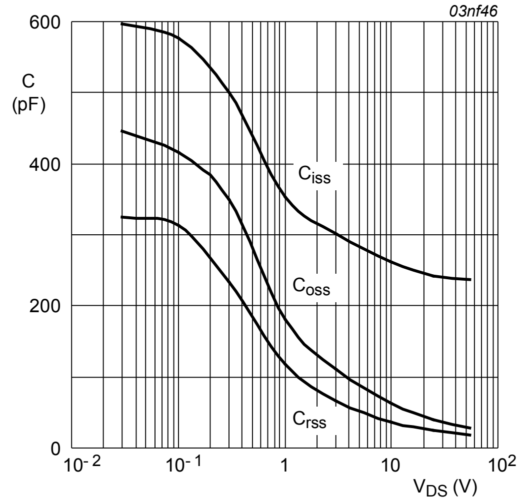


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

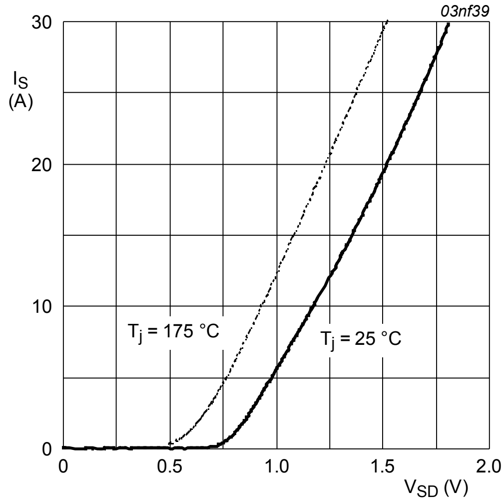
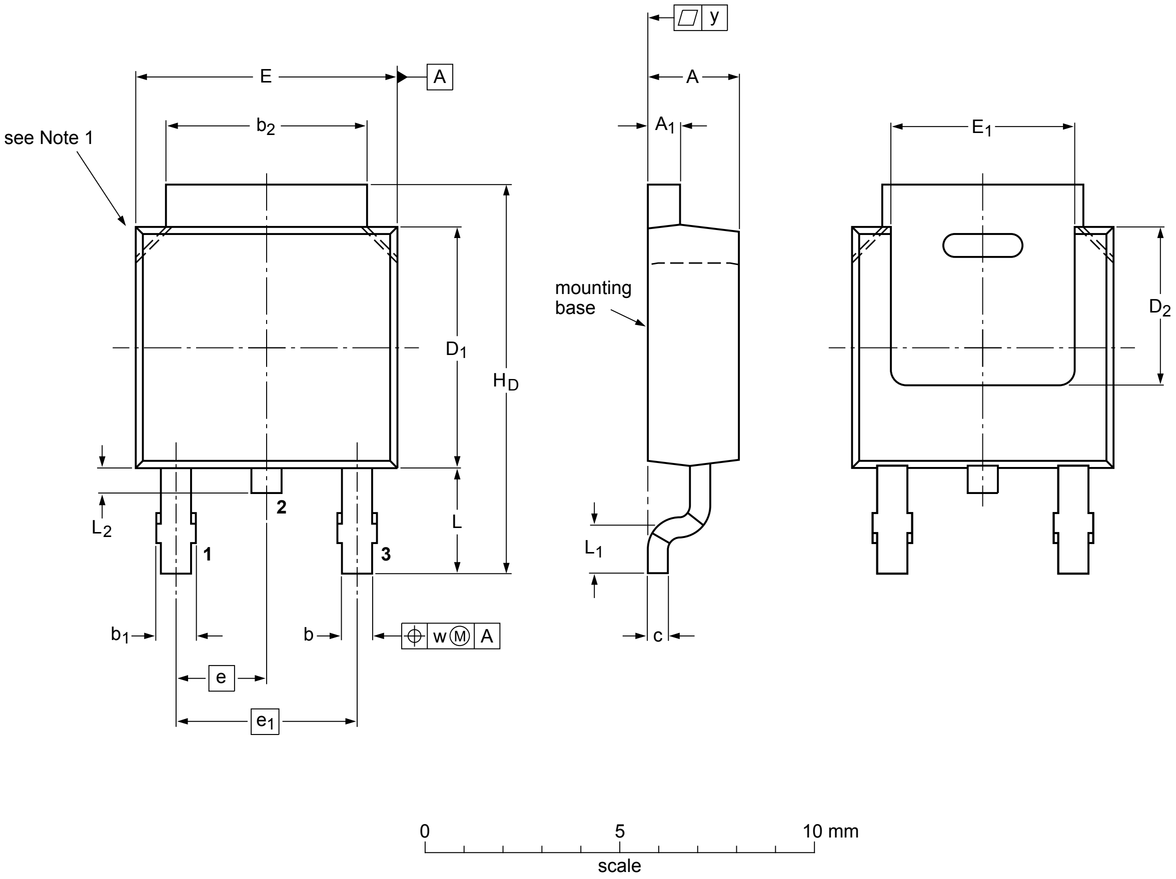


Fig. 15. Reverse diode current as a function of reverse diode voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_1	b_2	c	D_1	D_2	E	E_1	e	e_1	H_D	L	L_1	L_2	w	y
mm	max	2.38	0.93	0.89	1.1	5.46	0.56	6.22		6.73				10.4	2.95		0.9		0.2
	nom											2.285	4.57					0.2	
	min	2.22	0.46	0.71	0.9	5.00	0.20	5.98	4.0	6.47	4.45			9.6	2.55	0.5	0.5		

Note
1. Plastic body may have 45° chamfer.

sot428_po

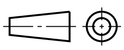
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-03-16~~ 14-06-10

Fig. 16. Package outline DPAK (SOT428)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

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Date of release: 12 June 2014