

N-channel TrenchMOS logic level FET Rev. 2 — 16 May 2012

**Product data sheet** 

#### 1. **Product profile**

### 1.1 General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated

### **1.3 Applications**

- 12V, 24V and 48V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications

### 1.4 Quick reference data

- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with Vgst(th) rating of greater than 0.5V at 175 °C
- Transmission control
- Ultra high performance power switching

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	80	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; T <sub>mb</sub> = 25 °C; see <u>Figure 1</u>	<u>[1]</u> -	-	120	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	357	W
Static charac	teristics					
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <u>Figure 11</u>	-	3.4	4.2	mΩ
Dynamic cha	racteristics					
$Q_{GD}$	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; V_{DS} = 64 \text{ V};$ see <u>Figure 13</u> ; see <u>Figure 14</u>	-	37.5	-	nC

[1] Continuous current is limited by package.

Quick reference data

Table 1.



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### 2. Pinning information

Table 2.	Pinning	j information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		-
2	D	drain	mb	
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

### 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK964R2-80E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

### 4. Marking

Table 4.   Marking codes	
Type number	Marking code
BUK964R2-80E	BUK964R2-80E

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### 5. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	80	V
V <sub>DGR</sub>	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	80	V
V <sub>GS</sub>	gate-source voltage	DC	-10	10	V
		Pulsed	-15	15	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; see <u>Figure 1</u>	<u>[1]</u> -	120	A
		$T_{mb}$ = 100 °C; $V_{GS}$ = 5 V; see <u>Figure 1</u>	<u>[1]</u> _	120	А
I <sub>DM</sub>	peak drain current	T <sub>mb</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs; see <u>Figure 4</u>	-	740	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	357	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-drai	n diode				
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	<u>[1]</u> _	120	А
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$	-	740	А
Avalanche r	uggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$\label{eq:ID} \begin{array}{l} I_D = 120 \text{ A}; \ V_{sup} \leq 80 \text{ V}; \ R_{GS} = 50 \ \Omega; \\ V_{GS} = 5 \text{ V}; \ T_{j(\text{init})} = 25 \ ^\circ\text{C}; \ \text{unclamped}; \\ \text{see} \ \overline{Figure \ 3} \end{array}$	[2][3]	485	mJ

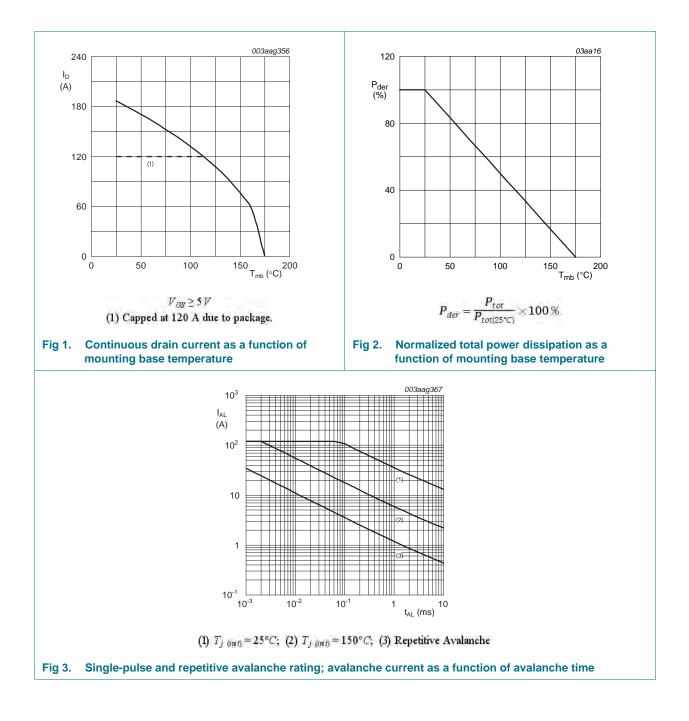
[1] Continuous current is limited by package.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

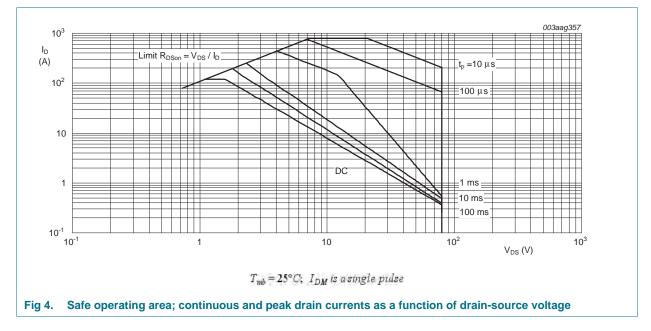
[3] Refer to application note AN10273 for further information.

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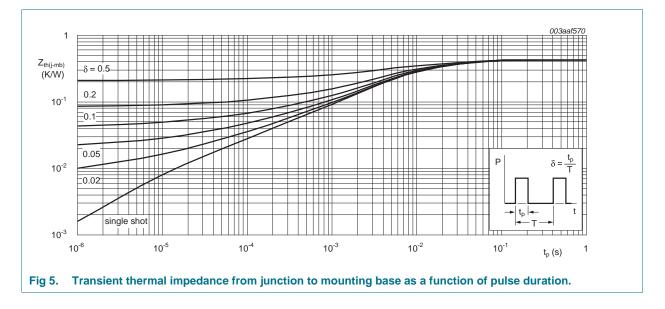
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### 6. Thermal characteristics

#### Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	see Figure 5	-	-	0.42	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



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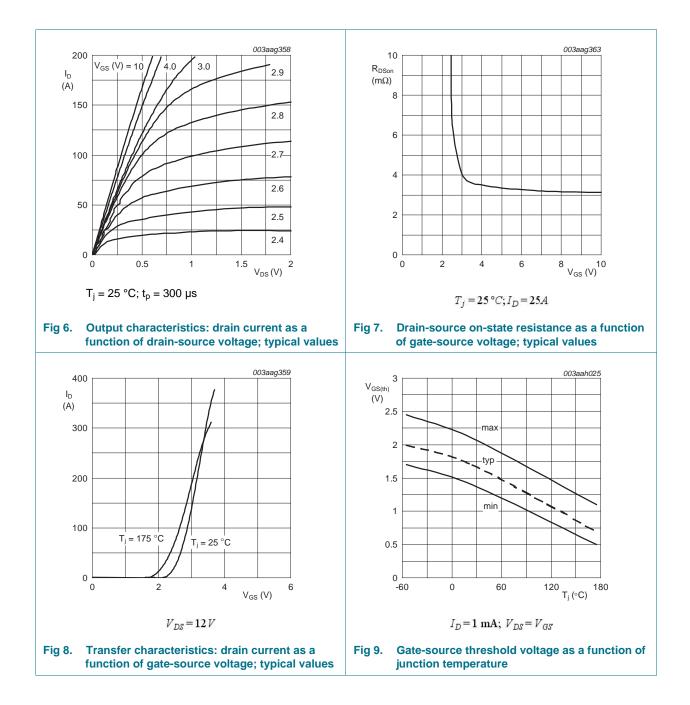
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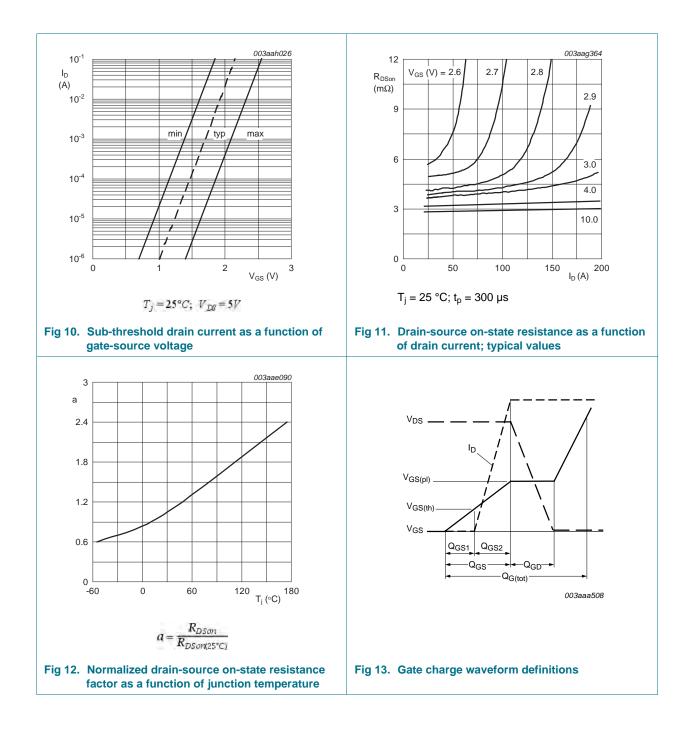
### 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V <sub>(BR)DSS</sub>	drain-source	$I_D = 250 \ \mu A; V_{GS} = 0 \ V; T_j = 25 \ ^{\circ}C$	80	-	-	V
	breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^{\circ}C$	72	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ see Figure 9; see Figure 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ see Figure 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ see Figure 9	0.5	-	-	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.08	1	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		$V_{GS}$ = -10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
Doon	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <u>Figure 11</u>	-	- 3.4 4	4.2	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <u>Figure 11</u>	-	3.2	4	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; see <u>Figure 12</u> ; see <u>Figure 11</u>	-	-	10.4	mΩ
Dynamic ch	aracteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 64 \text{ V}; V_{GS} = 5 \text{ V};$	-	123	-	nC
Q <sub>GS</sub>	gate-source charge	see <u>Figure 13</u> ; see <u>Figure 14</u>	-	26.6	-	nC
Q <sub>GD</sub>	gate-drain charge		-	37.5	-	nC
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz;$	-	12850	17130	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 15</u>	-	850	1020	pF
C <sub>rss</sub>	reverse transfer capacitance		-	420	580	pF
d(on)	turn-on delay time	$V_{DS} = 60 \text{ V}; \text{ R}_{L} = 2.4 \Omega; \text{ V}_{GS} = 5 \text{ V};$	-	70	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega$	-	109	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	203	-	ns
t <sub>f</sub>	fall time		-	115	-	ns
L <sub>D</sub>	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L <sub>S</sub>	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-drai	in diode					
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <u>Figure 16</u>	-	0.77	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_{S} = 20 \text{ A}; \text{ dI}_{S}/\text{dt} = -100 \text{ A}/\mu\text{s}; \text{ V}_{GS} = 0 \text{ V};$	-	61	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 25 V	-	139	_	nC

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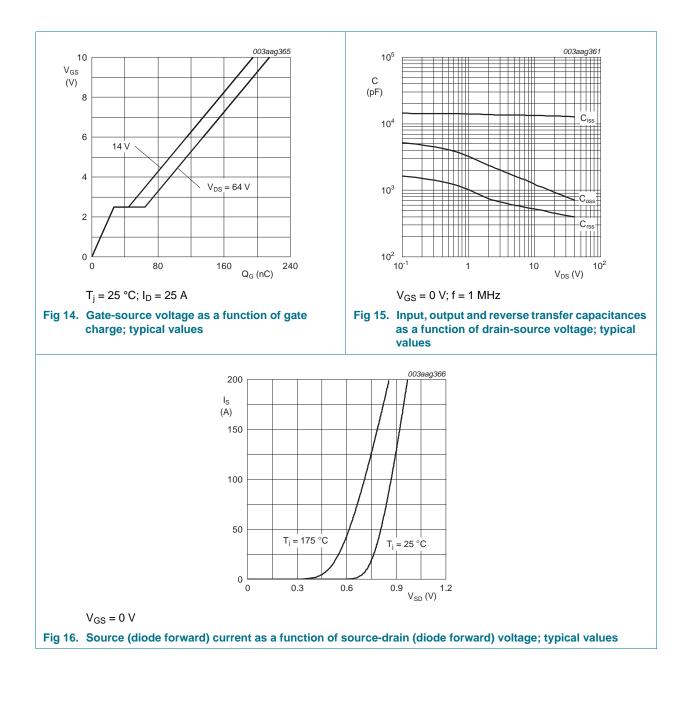
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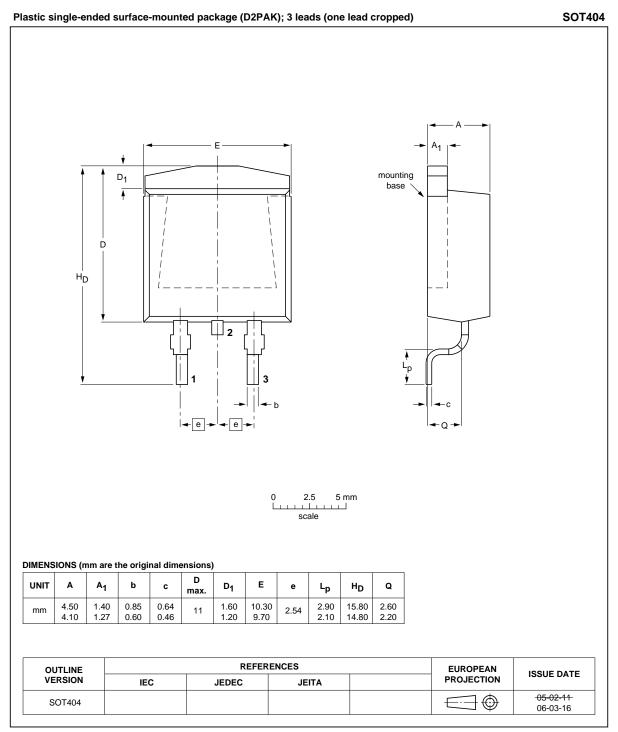
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### 8. Package outline



#### Fig 17. Package outline SOT404 (D2PAK)

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### 9. Revision history

Table 8. Revision I	nistory			
Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK964R2-80E v.2	20120516	Product data sheet	-	BUK964R2-80E v.1
Modifications:	<ul> <li>Status change</li> </ul>	ed from objective to product.		
	<ul> <li>Various chang</li> </ul>	ges to content.		
BUK964R2-80E v.1	20120404	Objective data sheet	-	-

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### **10. Legal information**

### **10.1 Data sheet status**

Document status[1] [2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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