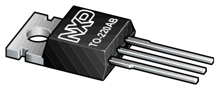

BUK953R2-40B

N-channel TrenchMOS logic level FET

17 April 2014 Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

3. Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2; Fig. 3	[1]	-	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	300	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	2.4	2.8	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; Fig. 11; Fig. 12		-	2.7	3.2	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 5 V; I_D = 25 A; V_{DS} = 32 V; T_j = 25 °C; Fig. 13		-	37	-	nC

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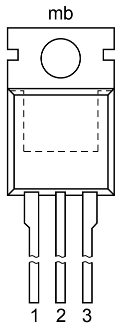
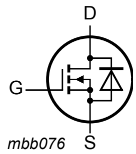
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	1.2	J

[1] All individual parts of device must be ≤ 175 °C to achieve maximum current rating.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 TO-220AB (SOT78A)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK953R2-40B	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage			-15	15	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	300	W
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 5 V; Fig. 2; Fig. 3	[1]	-	222	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Fig. 2	[2]	-	100	A
		T_{mb} = 25 °C; V_{GS} = 5 V; Fig. 2; Fig. 3	[2]	-	100	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Fig. 3		-	888	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	222	A
			[2]	-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C		-	888	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \leq 40$ V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	1.2	J

[1] Current is limited by power dissipation chip rating.
[2] All individual parts of device must be ≤ 175 °C to achieve maximum current rating.

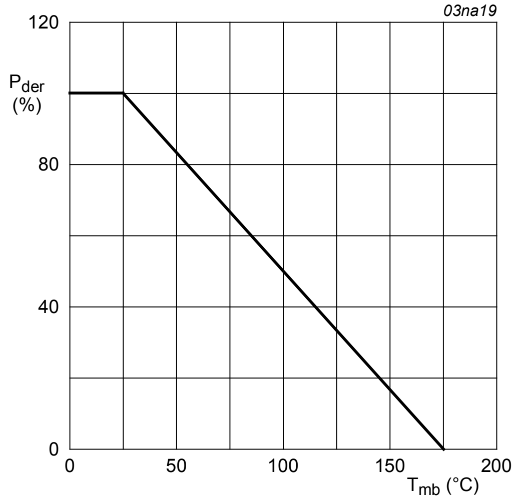


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\,\%$$

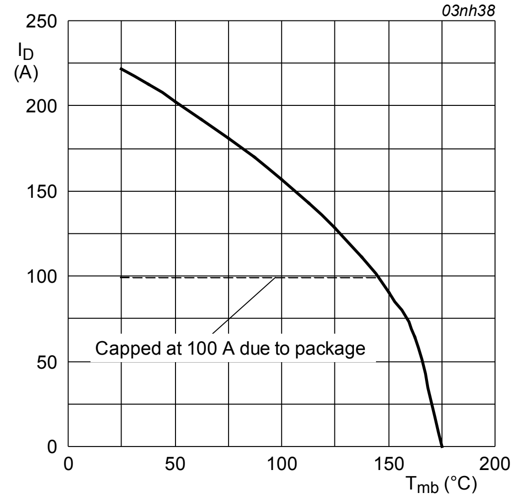


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 5V$$

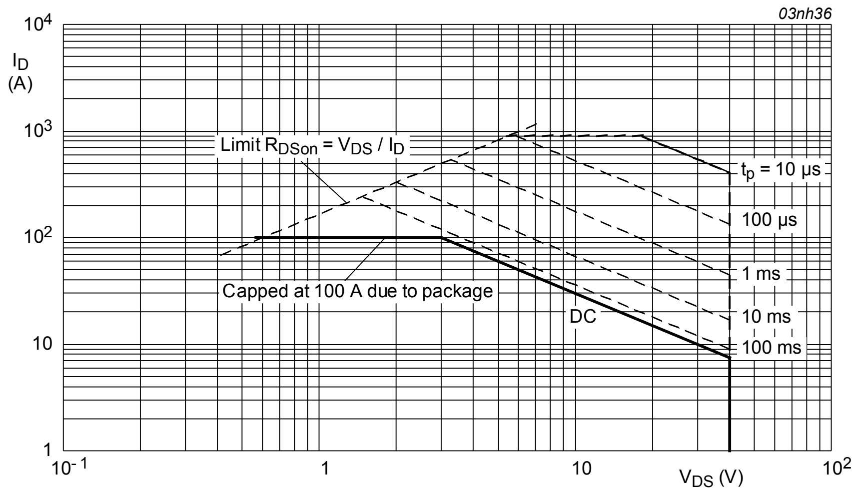


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25^{\circ}C; I_{DM} \text{ is single pulse}$$

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	-	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air		-	60	-	K/W

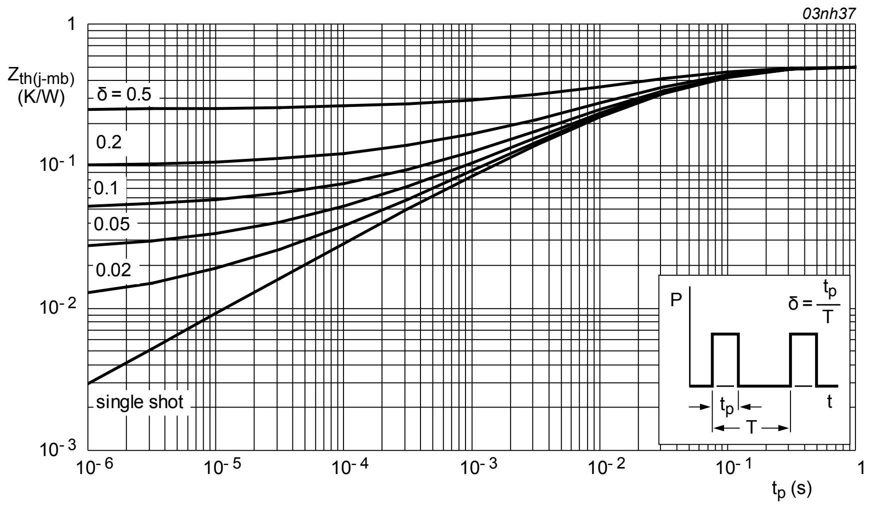


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 10		1.1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 10		0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.02	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{GSS}	gate leakage current	V_{GS} = 15 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -15 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	2.4	2.8	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C		-	-	3.5	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; Fig. 11; Fig. 12		-	-	6	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; Fig. 11; Fig. 12		-	2.7	3.2	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 13		-	94	-	nC
Q_{GS}	gate-source charge			-	17	-	nC
Q_{GD}	gate-drain charge			-	37	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	7877	10502	pF
C_{oss}	output capacitance			-	1397	1676	pF
C_{rss}	reverse transfer capacitance			-	608	833	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C		-	68	-	ns
t_r	rise time			-	268	-	ns
$t_{d(off)}$	turn-off delay time			-	257	-	ns
t_f	fall time			-	192	-	ns
L_D	internal drain inductance	from drain lead 6 mm from package to center of die; T_j = 25 °C		-	4.5	-	nH
		from contact screw on mounting base to center of die; T_j = 25 °C		-	3.5	-	nH
L_S	internal source inductance	from source lead to source bond pad; T_j = 25 °C		-	7.5	-	nH
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 40 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 20 V; T_j = 25 °C		-	70	-	ns
Q_r	recovered charge			-	127	-	nC

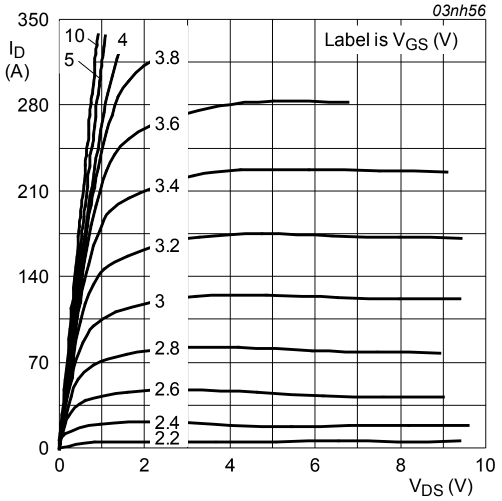


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

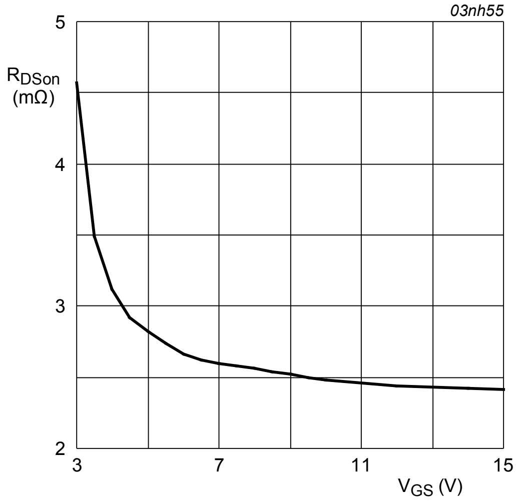


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C; I_D = 25A$

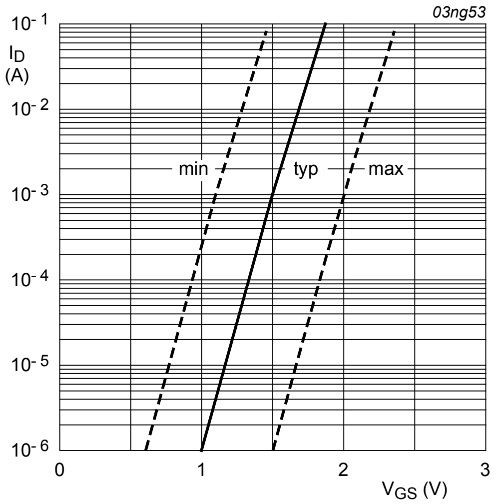


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25°C; V_{DS} = V_{GS}$

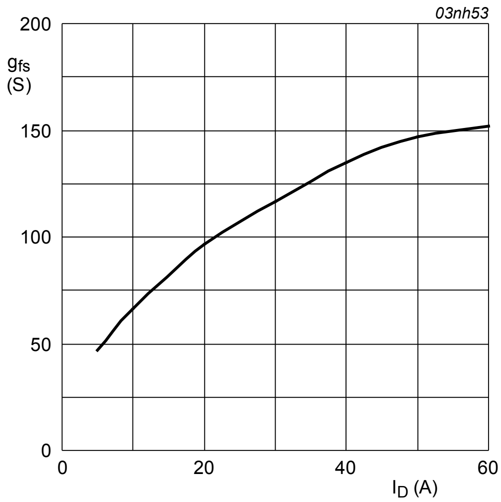


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25°C; V_{DS} = 25V$

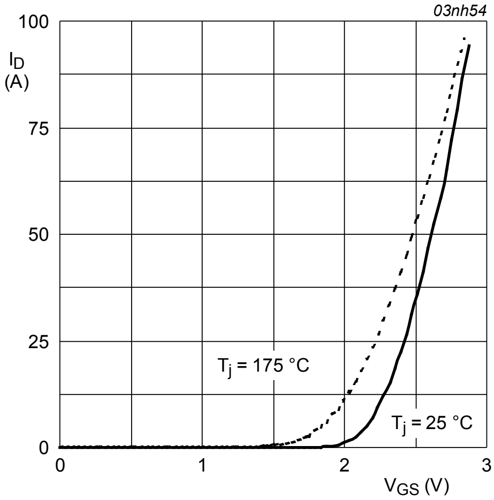


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 25V$

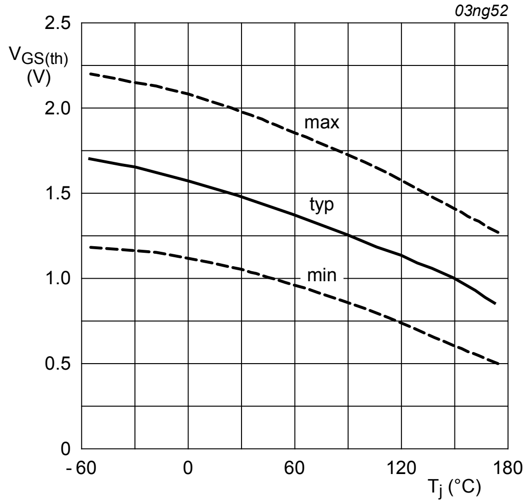


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1mA; V_{DS} = V_{GS}$

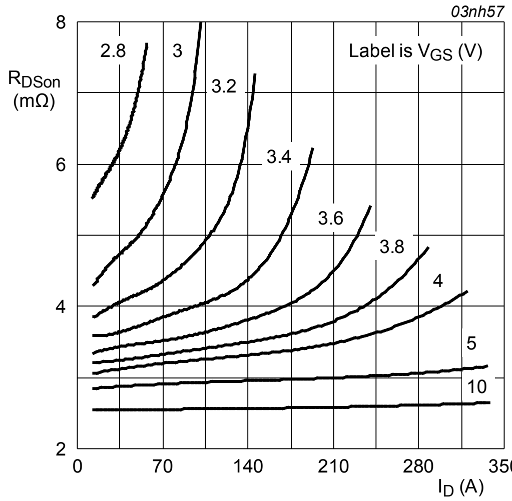


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

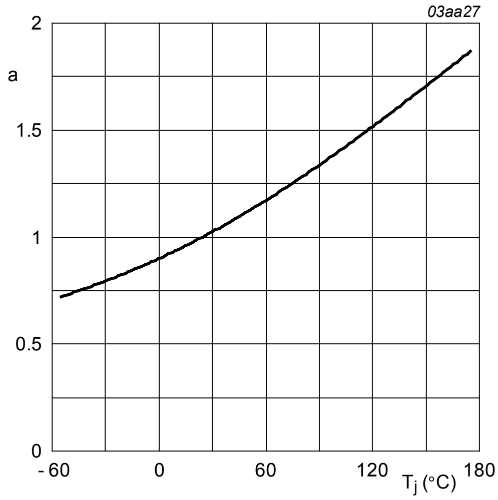


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

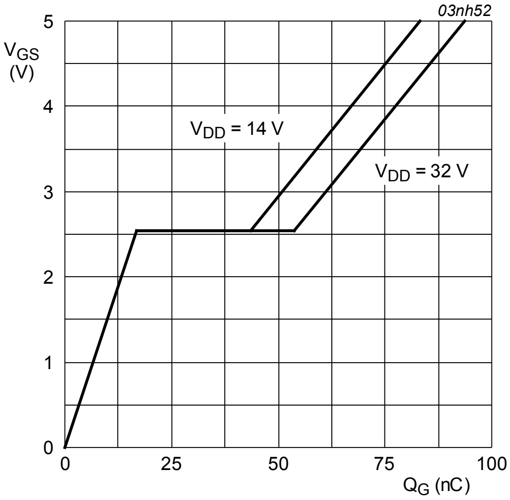


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C; V_{DS} = 25V$

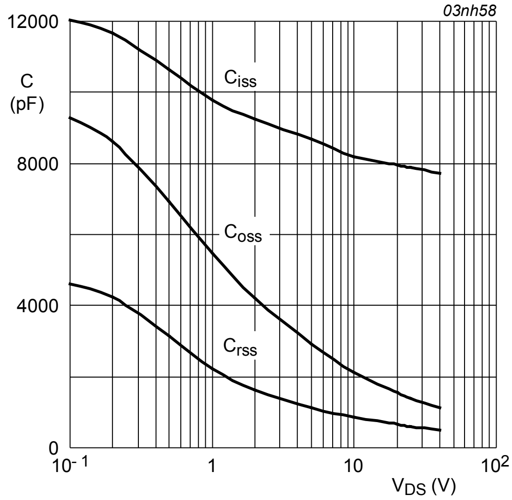


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

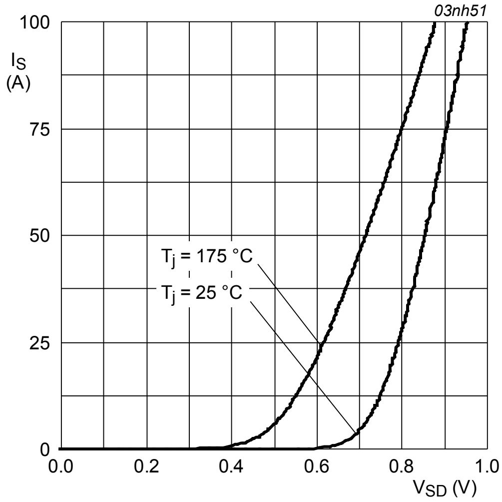
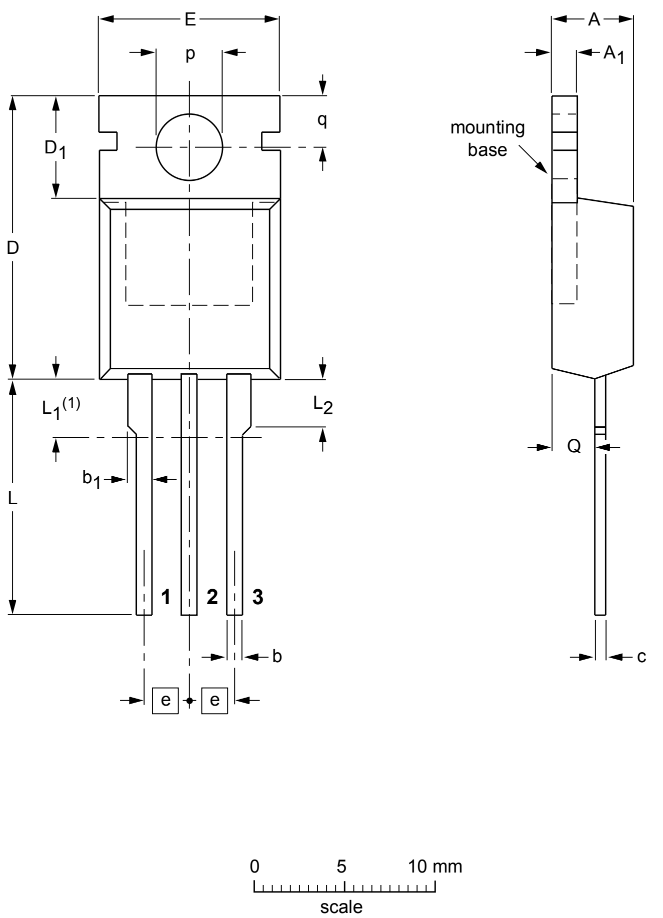


Fig. 15. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

10. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1[(1)]	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.6	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78A		3-lead TO-220AB	SC-46			~~03-01-22~~ 05-03-14

Fig. 16. Package outline TO-220AB (SOT78A)

11. Legal information

11.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 17 April 2014