

EARTH LEAKAGE CURRENT DETECTOR Earth Leakage Current Detector IC

BD95820F-LB BD95820N-LB

General Description

This product guarantees long time support in Industrial market.
BD95820F-LB/BD95820N-LB integrates leakage detector and amplifier. Especially, it is suitable for high sensitivity and a high-speed operation use, and since the operating temperature range is wide, it can be used for various uses.

Features

- Long Time Support a Product for Industrial Applications
- Small Temperature Fluctuation and High Input Sensitivity
- Wide Operating Temperature Range

Applications

- Earth leakage circuit breaker
- Earth leakage circuit relay
- Industrial Equipment

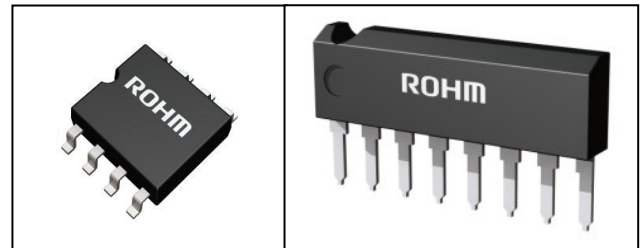
Key Specifications

- Operating Supply Voltage Range : 12V to 22V
- Operating Temperature Range : -20°C to +95°C
- Supply Current : 330µA (typ)
- Trip Voltage : 6.9mV to 8.9mV
- Output Current(T_A=-20°C) : -200µA (min)

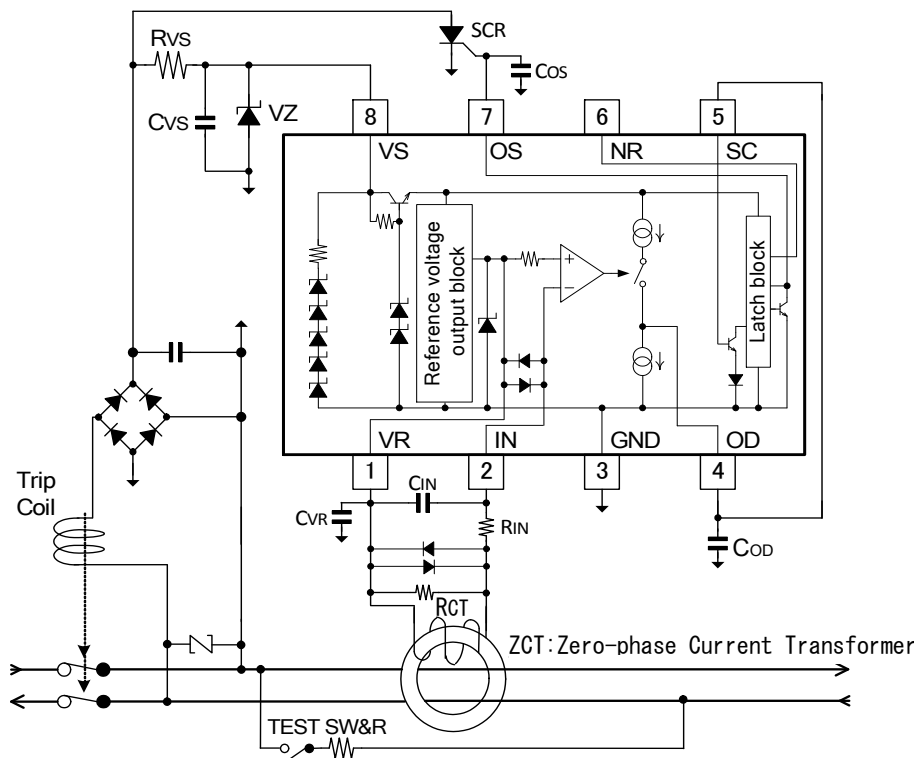
Packages

SOP8
SIP8

W(Typ) x D(Typ) x H(Max)
5.00mm x 6.20mm x 1.71mm
19.30mm x 10.50mm x 3.00mm



Typical Application Circuit



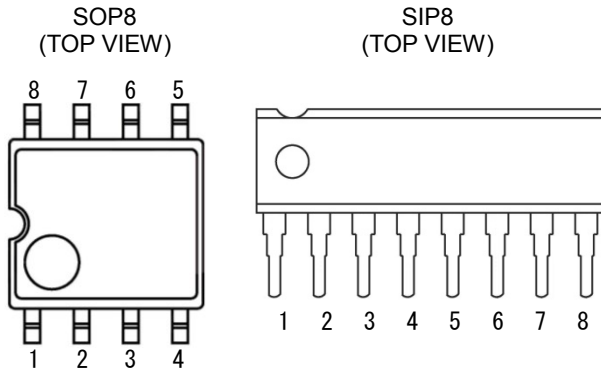
Recommended Value Range

- 0.01µF ≤ C_{OD} ≤ 0.1µF
- 0.01µF ≤ C_{IN} ≤ 0.1µF
- 0.01µF ≤ C_{VR} ≤ 1µF
- 0.01µF ≤ C_{OS} ≤ 1µF
- 0.1µF ≤ C_{VS} ≤ 10µF
- 100Ω ≤ R_{IN} ≤ 5kΩ
- 100Ω ≤ R_{CT} ≤ 5kΩ
- 39kΩ ≤ R_{VS} ≤ 150kΩ
- 100µs ≤ t_r (Note 1) ≤ 20ms
- 100µs ≤ t_f (Note 2) ≤ 20ms

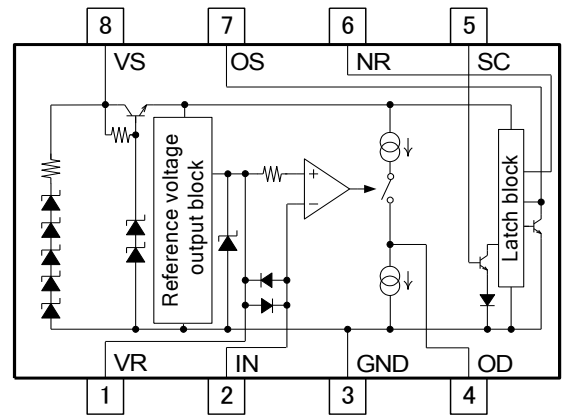
(Note 1) Time to change into 90% from 10% in the process when the power supply voltage rises to 12V from 0V.
(Note 2) Time to change into 90% from 10% in the process when the power supply voltage falls from 12V to 0V.

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configurations



Block Diagrams



Pin Descriptions

| Pin No. | Symbol | Function |
|---------|--------|----------------------------|
| 1 | VR | Reference voltage |
| 2 | IN | Input |
| 3 | GND | Ground |
| 4 | OD | Output of input comparator |
| 5 | SC | Input of latch circuit |
| 6 | NR | Noise absorption |
| 7 | OS | Output |
| 8 | VS | Power supply |

Absolute Maximum Ratings (TA=25°C)

| Parameter | Symbol | Rating | Unit |
|------------------------------|--------------|---------------------|------|
| Supply current (Note 3) | IS | 8 | mA |
| IN-VR current | IIN-VR | ±250 | mA |
| VR pin current | IVR | 30 | mA |
| IN terminal current | IIN | 30 | mA |
| SC terminal current | ISC | 5 | mA |
| Power Supply voltage | VS | 36 | V |
| Input terminal voltage | VVR/IN | 17 | V |
| OD/SC/NR/OS terminal voltage | VOD/SC/NR/OS | 8 | V |
| Power dissipation | PD | 0.68(SOP8) (Note 4) | W |
| | | 1.12(SIP8) (Note 5) | |
| Storage temperature | Tstg | -55 to +150 | °C |

(Note 3) The power-supply voltage is limited by the internal clamping circuit.

(Note 4) Mounted on 70mm x 70mm x 1.6mm glass epoxy board. Reduce 5.5mW per 1°C above 25°C.

(Note 5) PD is a value in the package unit. Reduce 9.0mW per 1°C above 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Ratings

| Parameter | Symbol | Limits | Unit |
|-----------------------|-----------|------------|------|
| Supply voltage | V_S | 12 to 22 | V |
| Operating temperature | T_{opr} | -20 to +95 | °C |

Electrical Characteristics

(Unless otherwise specified, $V_S=12V$, $GND=0V$, $T_A=25^\circ C$, Full range: $-20^\circ C$ to $+95^\circ C$)

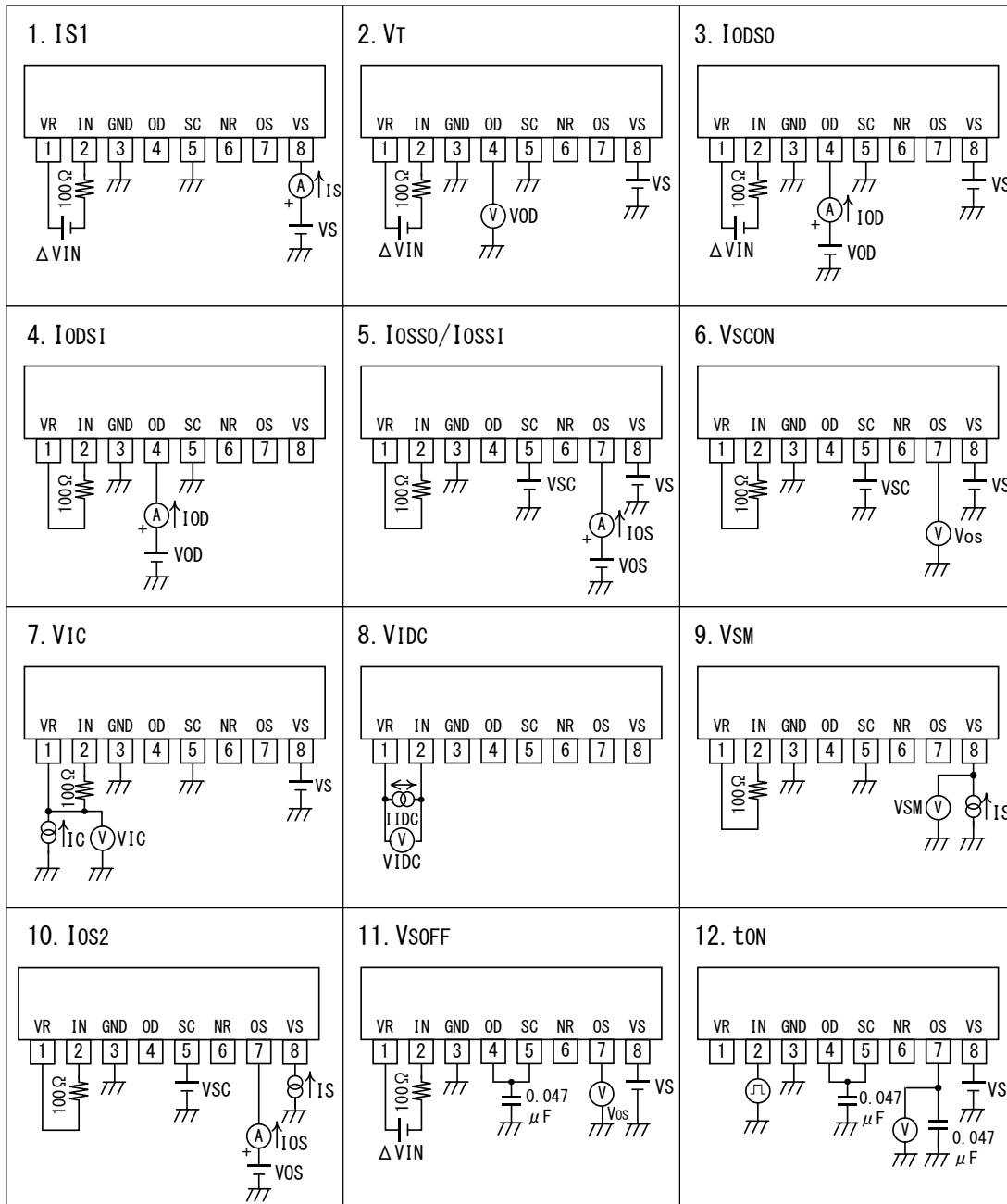
| Parameter | Symbol | Temperature range | Limits | | | Unit | Conditions |
|--------------------------------------|------------|-------------------|--------|-------|-------|---------|---|
| | | | Min | Typ | Max | | |
| Supply current | I_{S1} | $-20^\circ C$ | - | - | 520 | μA | $\Delta V_{IN}=V_{VR}-V_{IN}=30mV$ |
| | | $25^\circ C$ | - | 330 | 500 | | |
| | | $95^\circ C$ | - | - | 460 | | |
| Trip voltage | V_T | Full range | 4.92 | 7.50 | 11.06 | mV | $V_T=\Delta V_{IN}=V_{VR}-V_{IN}$ |
| OD Source current | I_{ODSO} | $25^\circ C$ | -27.2 | -20.6 | -14.0 | μA | $\Delta V_{IN}=V_{VR}-V_{IN}=30mV$, $V_{OD}=1.2V$ |
| OD Sink current | I_{ODSI} | $25^\circ C$ | 16.7 | 26.0 | 35.3 | μA | $V_{OD}=0.8V$, $\Delta V_{IN}=V_{VR}-V_{IN}=0mV$ |
| OS Source current | I_{OSSO} | $-20^\circ C$ | -200 | - | - | μA | $V_{SC}=2.0V$, $V_{OS}=0.8V$ |
| | | $25^\circ C$ | -100 | - | - | | |
| | | $95^\circ C$ | -75 | - | - | | |
| OS Sink current | I_{OSSI} | Full range | 200 | - | - | μA | $V_{SC}=0.2V$, $V_{OS}=0.2V$ |
| SC ON voltage | V_{SCON} | $25^\circ C$ | 1.00 | 1.24 | 1.48 | V | |
| Input clamp voltage | V_{IC} | Full range | 4.2 | 5.5 | 6.7 | V | $I_{IC}=20mA$ |
| Differential input clamp voltage | V_{IDC} | Full range | 0.6 | 1.0 | 1.4 | V | $I_{IDC}=100mA$ |
| Maximum current voltage | V_{SM} | $25^\circ C$ | 26 | 29 | 32 | V | $I_S=7mA$ |
| Supply current 2 ^(Note 6) | I_{OS2} | Full range | -100 | - | - | μA | $I_S=900\mu A$, $V_{SC}=2.0V$ $V_{OS}=0.8V$ |
| Latch OFF Supply Voltage | V_{SOFF} | $25^\circ C$ | 2.7 | 3.7 | 4.7 | V | |
| Operating time ^(Note 7) | t_{ON} | $25^\circ C$ | 1.8 | 2.9 | 4.0 | ms | |

(Note 6) Supply current 2 is OS source current value when the power supply current($I_S=900\mu A$) is given.

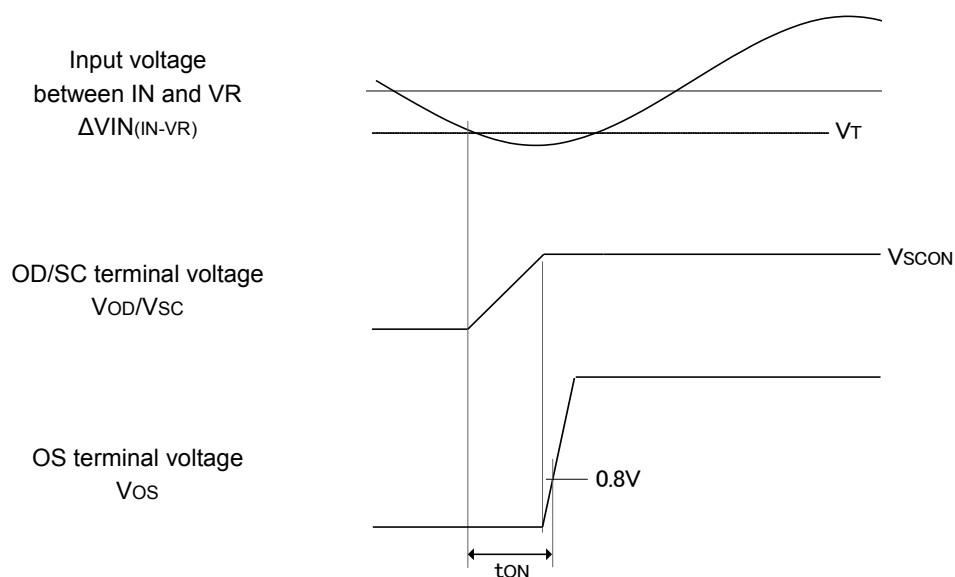
(Note 7) Operating time is time until output voltage reaches 0.8V after detecting the leakage signal.

Conditions : Capacitor(0.047 μF) is connected between OD(OS) and GND.

Test circuits



Timing Chart



Application Hint

1. Input Resistance R_{IN}

Larger bias current flow through the input terminal "IN" in power-up state. This larger current generates undesirable voltage between the input terminals via input resistance. The input resistance should be less than $5k\Omega$ so that this terminal voltage is restrained under the trip voltage and the voltage never cause any malfunction.

Even in normal operation, the offset voltage caused via input resistance and bias current might produce undesirable trip voltage shift. The input resistance should be designed with sufficient margin against this shift.

Typical Performance Curves(reference data)

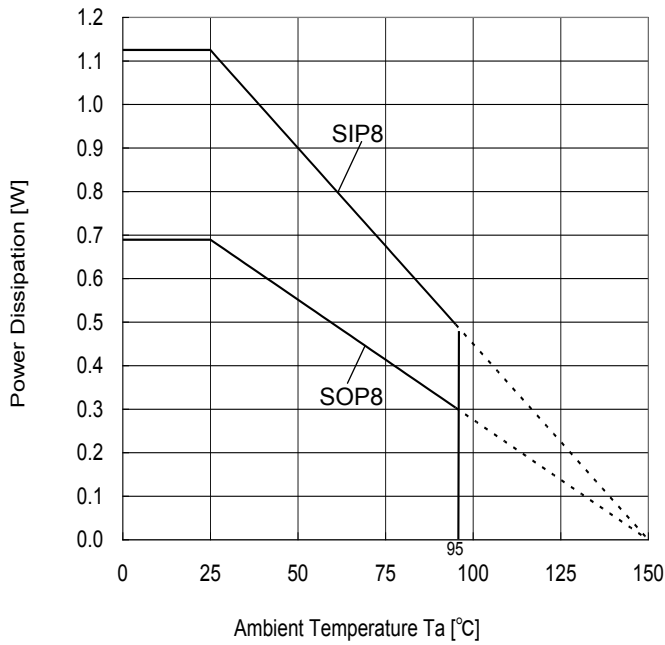


Figure 1
Derating curve

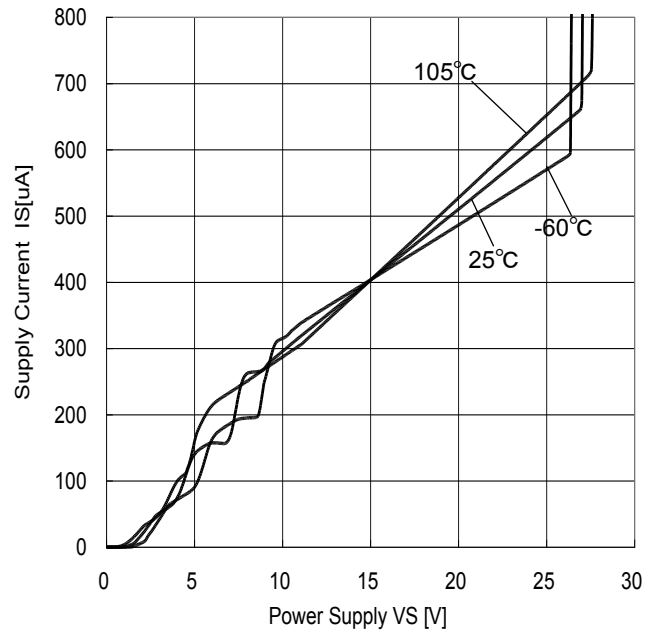


Figure 2
Circuit current - Supply voltage

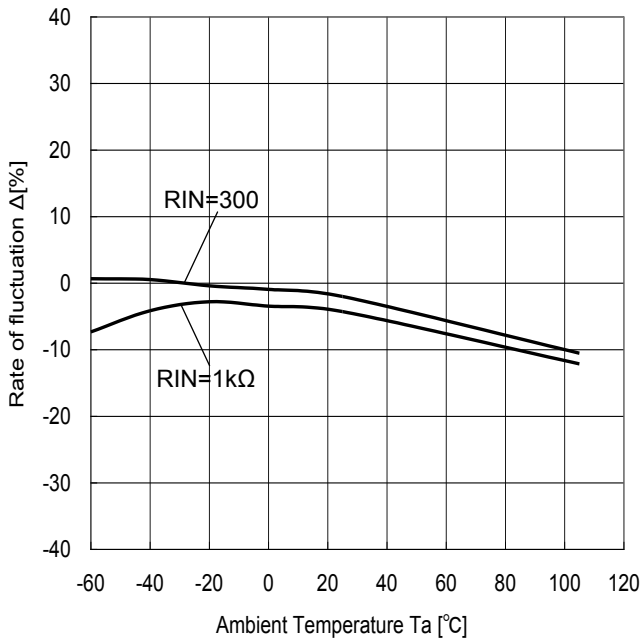


Figure 3
Trip voltage fluctuation rate
- Ambient temperature

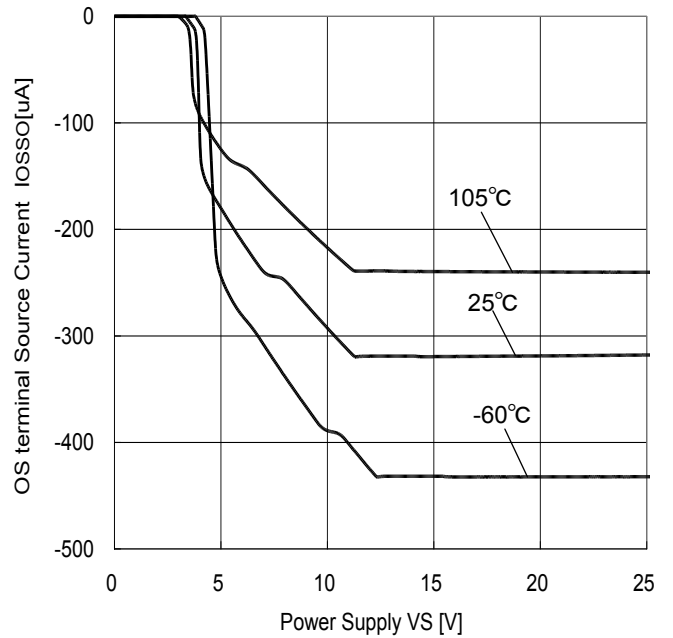


Figure 4
OS terminal source current - Supply voltage

Typical Performance Curves(reference data) - continued

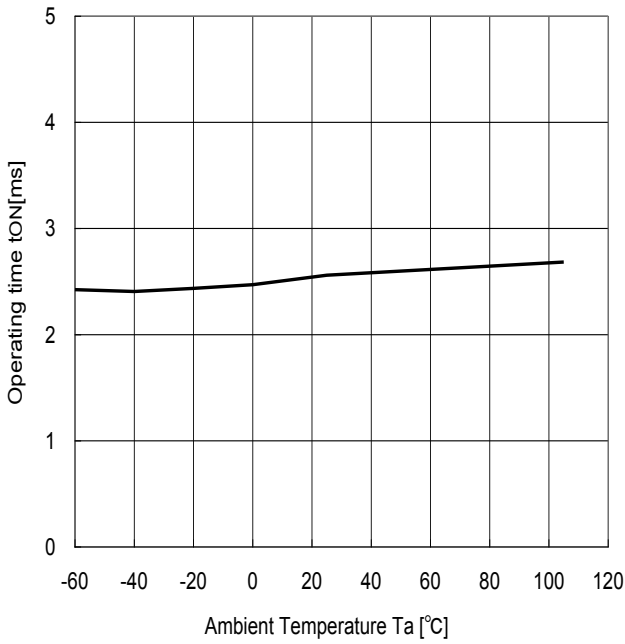


Figure 5
Operating time - Ambient temperature

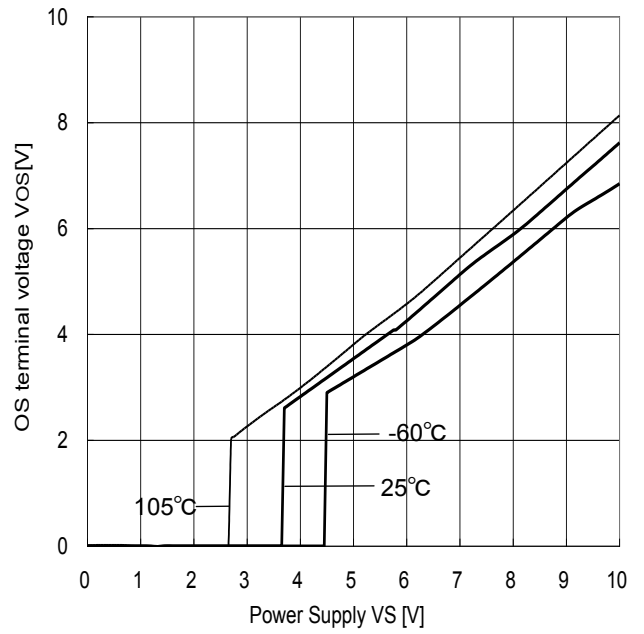


Figure 6
Latch OFF supply voltage - Ambient temperature

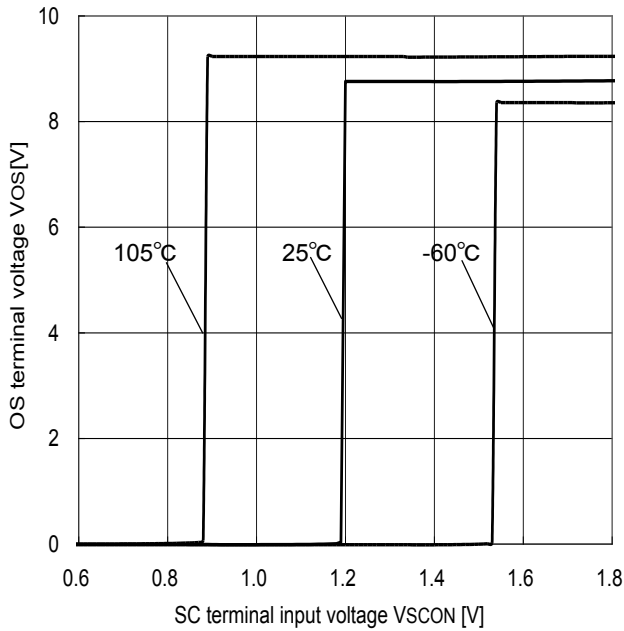


Figure 7
SC ON voltage - Ambient temperature

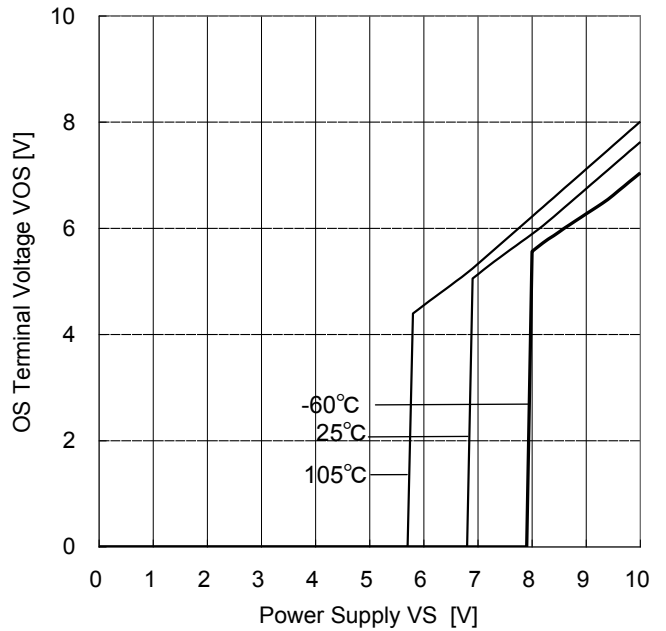


Figure 8
Latch ON supply voltage - Ambient temperature

Power Dissipation

Power dissipation(total loss) indicates the power that can be consumed by IC at $T_A=25^{\circ}\text{C}$ (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol $\theta_{JA}^{\circ}\text{C/W}$. The temperature of IC inside the package can be estimated by this thermal resistance. Figure 9(a) shows the model of thermal resistance of the package. Thermal resistance θ_{JA} , ambient temperature T_A , junction temperature T_{Jmax} , and power dissipation P_D can be calculated by the equation below.

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad ^{\circ}\text{C/W}$$

Derating curve in Figure 9(b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{JA} . Thermal resistance θ_{JA} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 10(a) show a derating curve for an example of BD95820F-LB, BD95820N-LB .

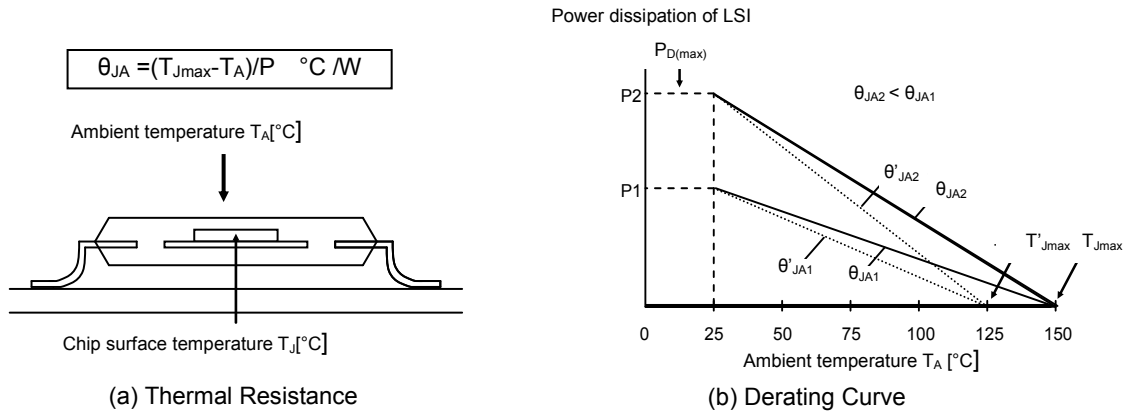
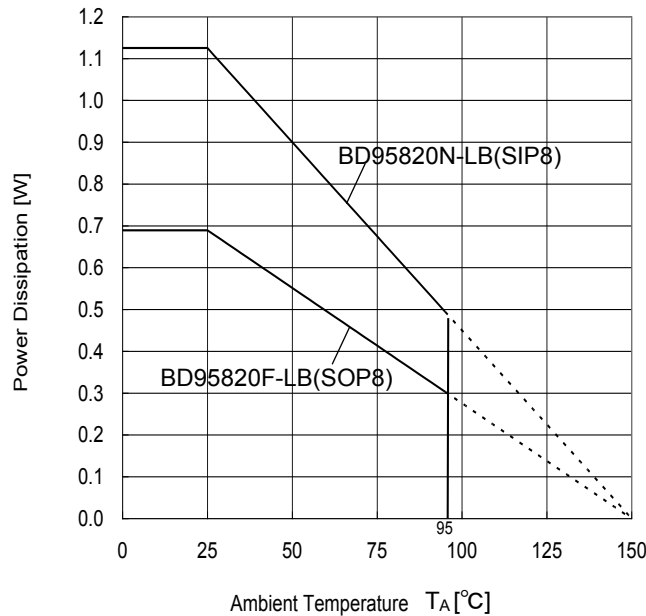


Figure 9. Thermal resistance and derating



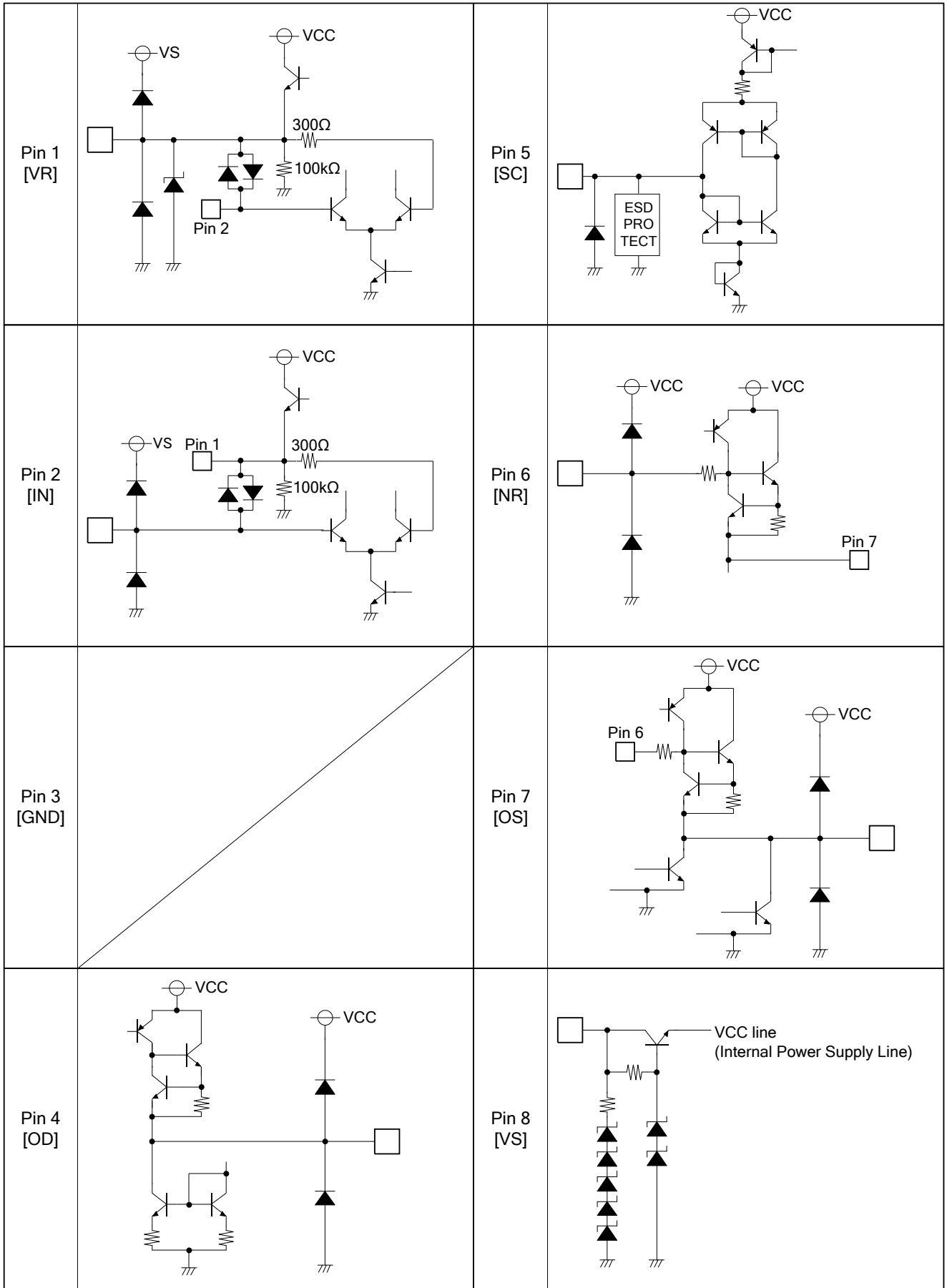
(a) BD95820F-LB · BD95820N-LB

| | Derating curve slope | UNIT |
|-------------------|----------------------|-------|
| BD95820F-LB(SOP8) | 5.5 | mW/°C |
| BD95820N-LB(SIP8) | 9.0 | |

When using the unit above $T_A=25^{\circ}\text{C}$, subtract the value above per degree $^{\circ}\text{C}$
 BD95820F-LB : Permissible dissipation is a value when glass epoxy board 70mm×70mm×1.6mm (cooper foil area below 3%) is mounted.
 BD95820N-LB : Permissible dissipation is a value in the package unit.

Figure 10. Derating curve

I/O equivalence circuit



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
 When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

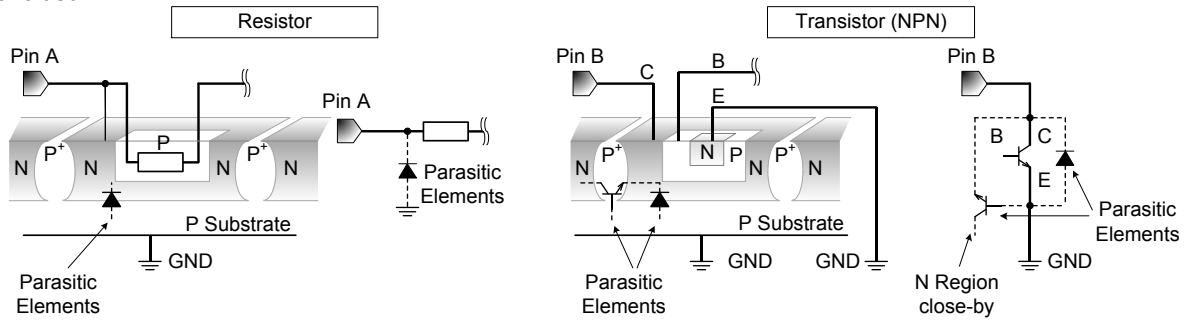
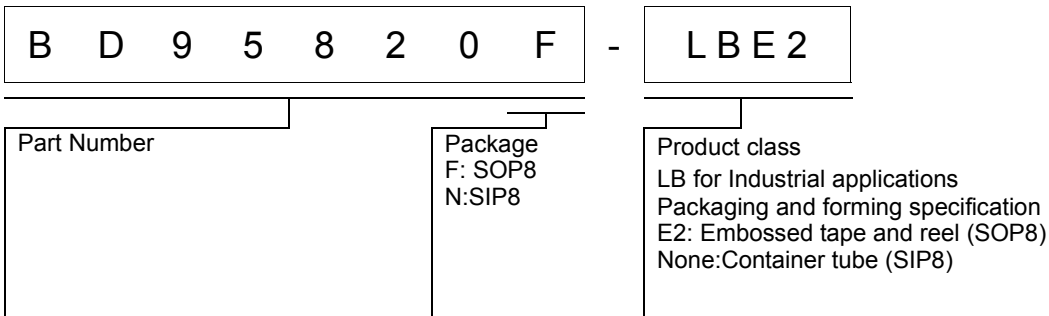
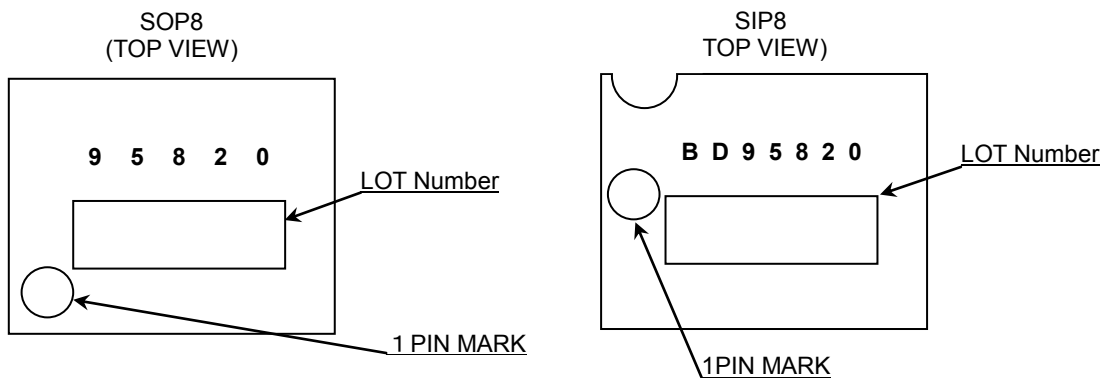


Figure 11. Example of monolithic IC structure

Ordering Information

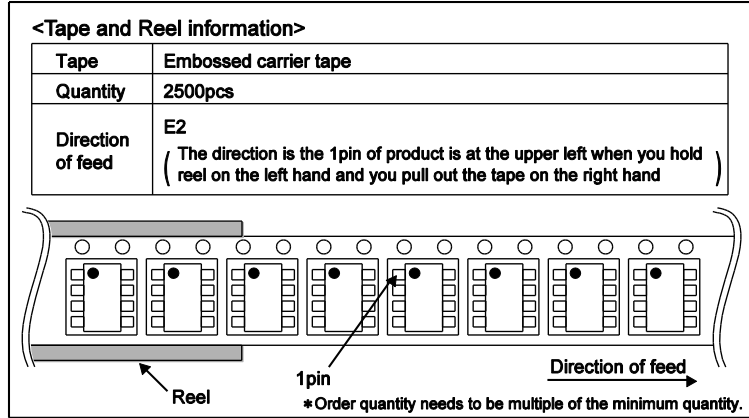
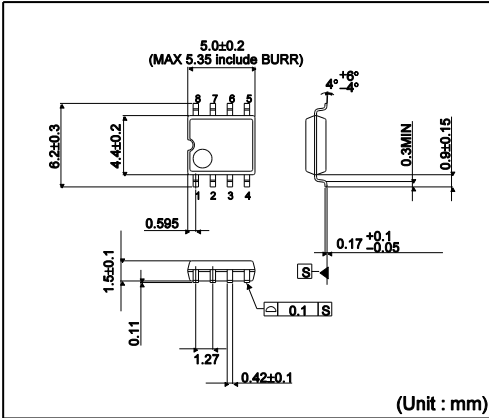


Marking Diagrams

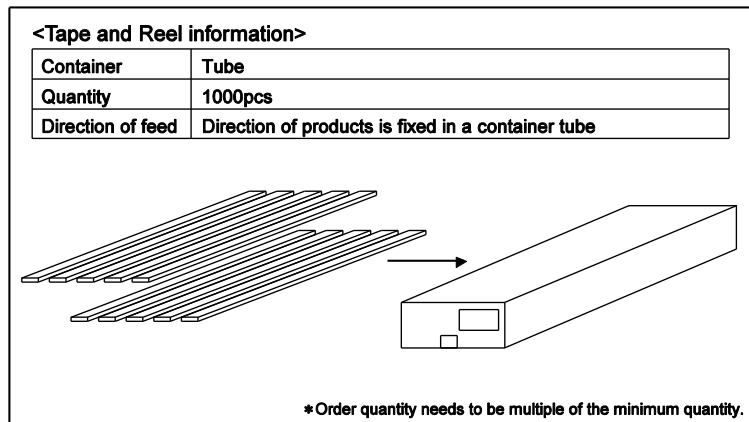
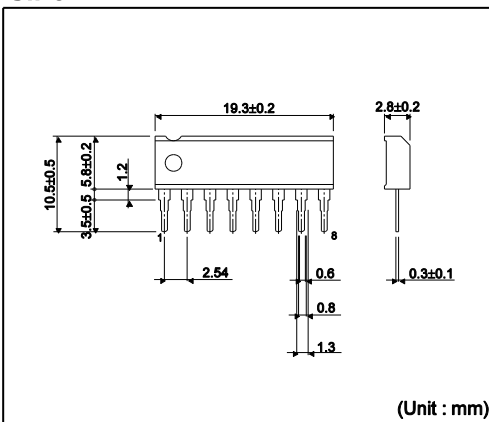


Physical Dimension Tape and Reel Information

SOP8



SIP8



Revision History

| Date | Revision | Changes |
|-------------|----------|--|
| 13.Jun.2014 | 001 | New Release |
| 29.Sep.2014 | 002 | Page.1 Typical Application Circuit $R_{IN} \leq 3k\Omega \rightarrow R_{IN} \leq 5k\Omega$ Page.10 Operational Notes 13.Input Resistance R_{IN} |
| 28.Sep.2015 | 003 | Page.1 Key Specifications: Trip Voltage 4.92mV to 11.06mV \rightarrow 6.9mV to 8.9mV Typical Application Circuit: Add the Recommended External Parts Value Page.2 Absolute Maximum Ratings: Add the sentence of Caution Page.3 Electrical Characteristics: Trip Voltage 4.92mV to 11.06mV \rightarrow 6.9mV to 8.9mV Page.5 Application Hint: Add 1. Input Resistance R_{IN} (Moved from Operational Notes 13) |

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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