BCW72LT1G, SBCW72LT1G

General Purpose Transistor

NPN Silicon

Features

- AEC−Q101 Qualified and PPAP Capable
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

ON Semiconductor®

SOT−23
(TO−236)
CASE 318−08
STYLE 6

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	45	Vdc
Collector – Base Voltage	V_{CBO}	50	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	100	mAdc

THERMAL CHARACTERISTICS

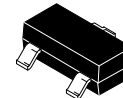| Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board, (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. FR−5 = 1.0 x 0.75 x 0.062 in.
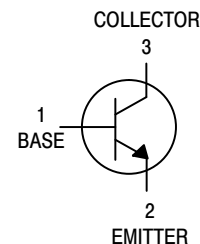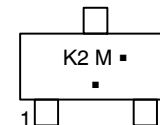2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

COLLECTOR
3

1
BASE

2
EMITTER

MARKING DIAGRAM

K2 M ▪

1

K2 = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping[†]
BCW72LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel
SBCW72LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (I_C = 2.0 mAdc, V_{EB} = 0)	$V_{(BR)CEO}$	45	–	–	Vdc
Collector – Emitter Breakdown Voltage (I_C = 2.0 mAdc, V_{EB} = 0)	$V_{(BR)CES}$	45	–	–	Vdc
Collector – Base Breakdown Voltage (I_C = 10 µAdc, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Emitter – Base Breakdown Voltage (I_E = 10 µAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0) (V_{CB} = 20 Vdc, I_E = 0, T_A = 100°C)	I_{CBO}	– –	– –	100 10	nAdc µAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	200	–	450	–
Collector – Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0.5 mAdc) (I_C = 50 mAdc, I_B = 2.5 mAdc)	$V_{CE(sat)}$	– –	– 0.21	0.25 –	Vdc
Base – Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 2.5 mAdc)	$V_{BE(sat)}$	–	0.85	–	Vdc
Base – Emitter On Voltage (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	0.6	–	0.75	Vdc
SMALL – SIGNAL CHARACTERISTICS					
Current – Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	–	300	–	MHz
Output Capacitance (I_E = 0, V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{obo}	–	–	4.0	pF
Input Capacitance (I_E = 0, V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{ibo}	–	9.0	–	pF
Noise Figure (I_C = 0.2 mAdc, V_{CE} = 5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)	NF	–	–	10	dB

EQUIVALENT SWITCHING TIME TEST CIRCUITS
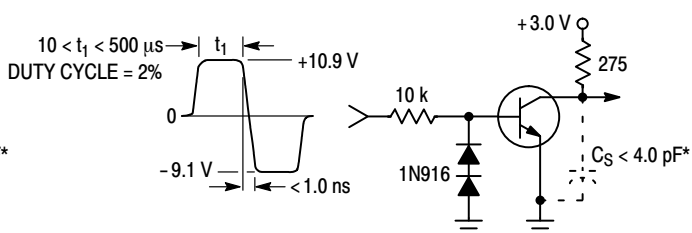
*Total shunt capacitance of test jig and connectors

Figure 1. Turn–On Time

Figure 2. Turn–Off Time

BCW72LT1G, SBCW72LT1G

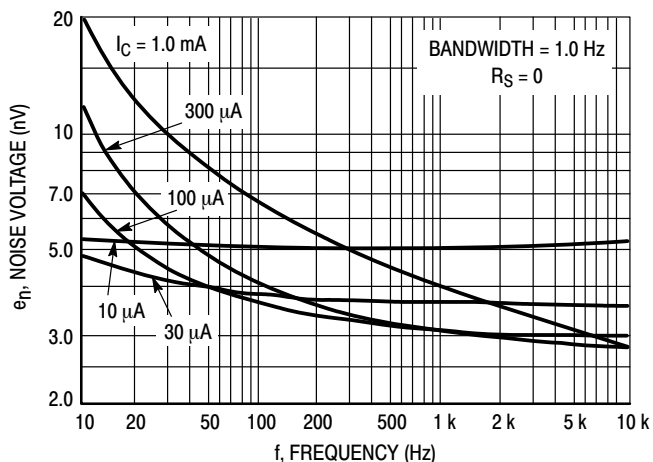## TYPICAL NOISE CHARACTERISTICS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

Figure 3. Noise Voltage

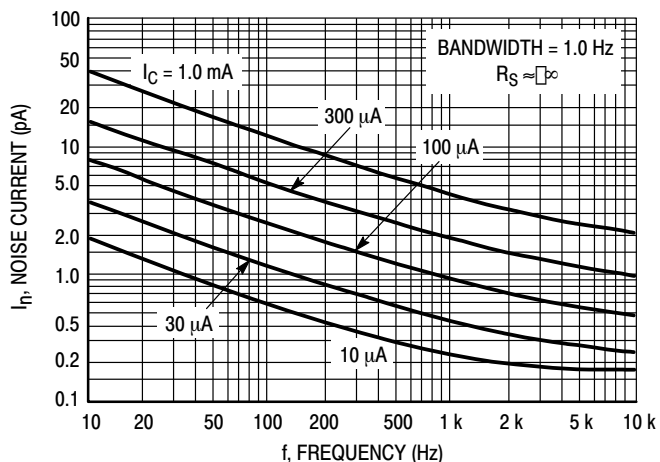

Figure 4. Noise Current

NOISE FIGURE CONTOURS

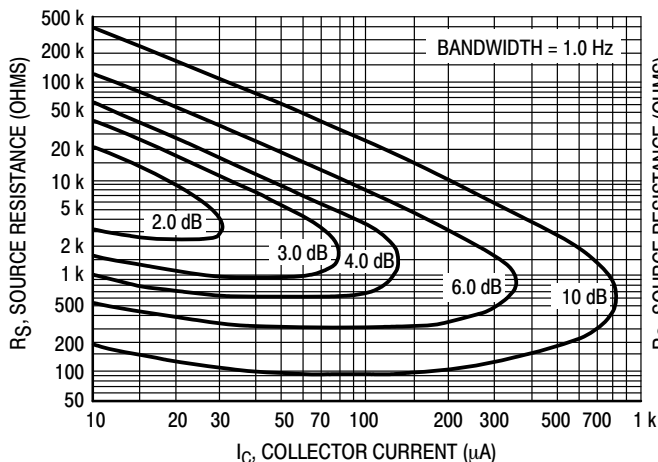(V_{CE} = 5.0 Vdc, T_A = 25°C)

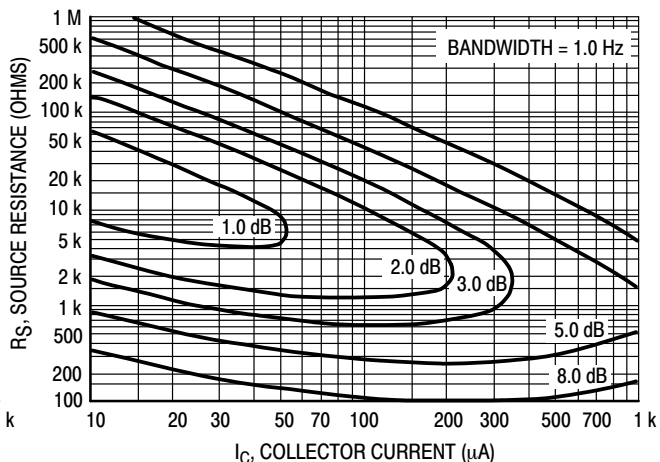
Figure 5. Narrow Band, 100 Hz
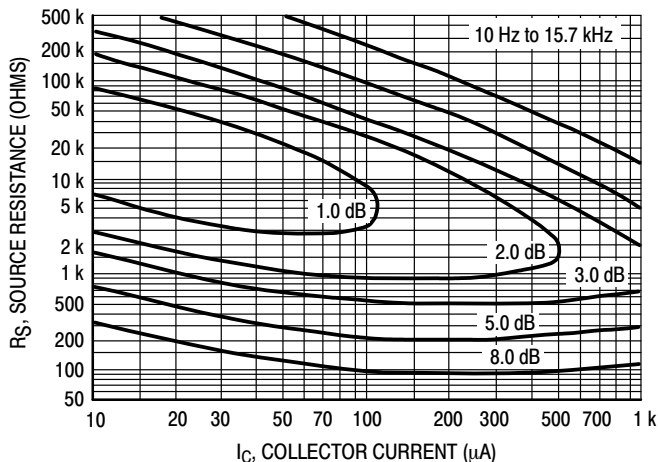

Figure 6. Narrow Band, 1.0 kHz

Figure 7. Wideband

Noise Figure is defined as:

$$NF = 20 \log_{10} \left(\frac{e_n{}^2 + 4KTR_S + I_n{}^2 R_S{}^2}{4KTR_S} \right)^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)
I_n = Noise Current of the Transistor referred to the input. (Figure 4)
K = Boltzman's Constant (1.38×10^{-23} j/°K)
T = Temperature of the Source Resistance (°K)
R_S = Source Resistance (Ohms)

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TYPICAL STATIC CHARACTERISTICS
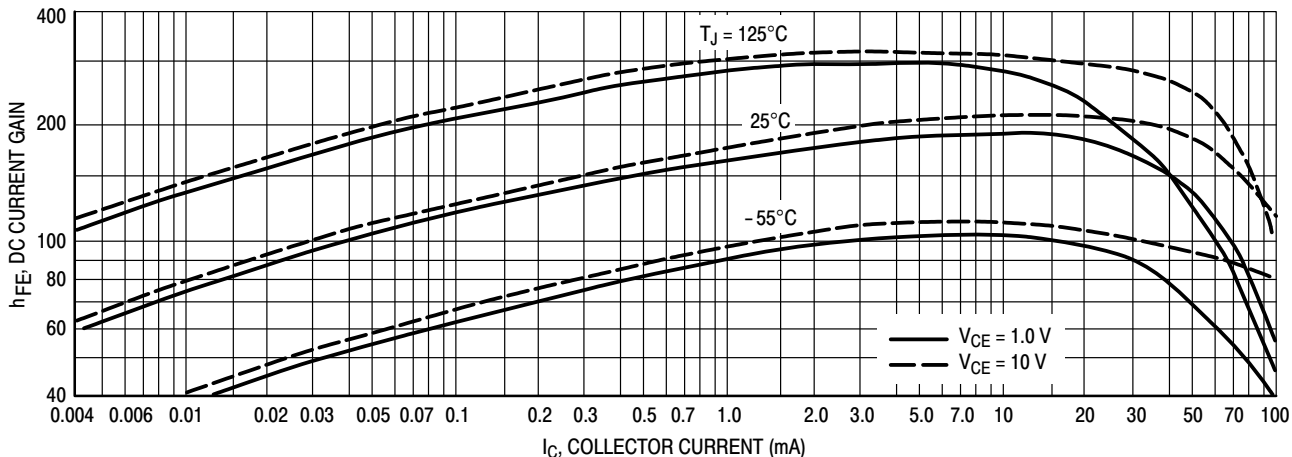
Figure 8. DC Current Gain
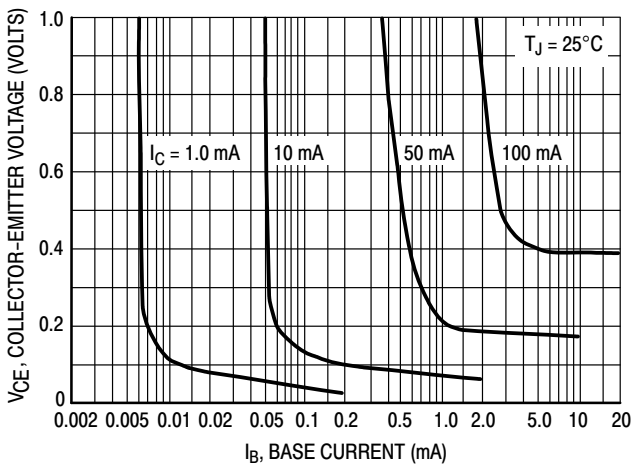
Figure 9. Collector Saturation Region
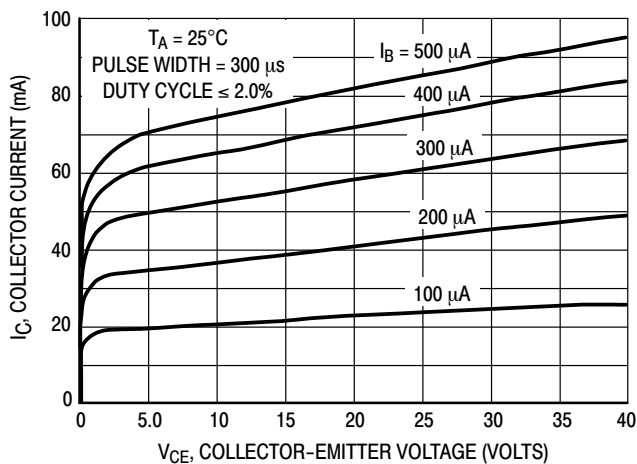
Figure 10. Collector Characteristics
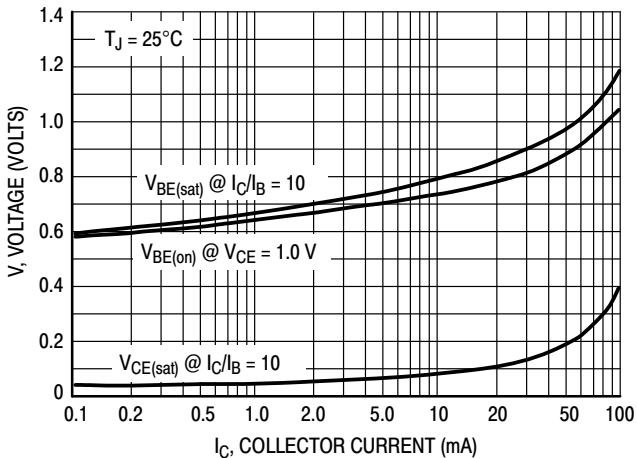
Figure 11. "On" Voltages
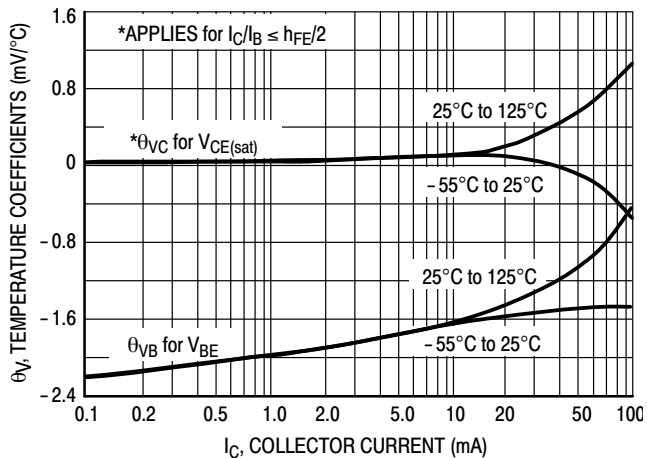
Figure 12. Temperature Coefficients

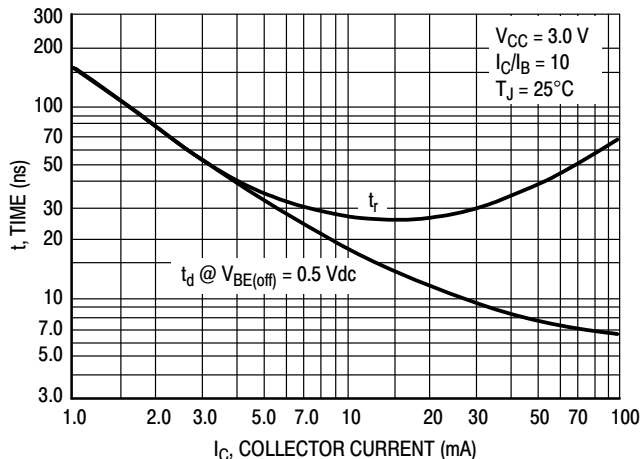# BCW72LT1G, SBCW72LT1G

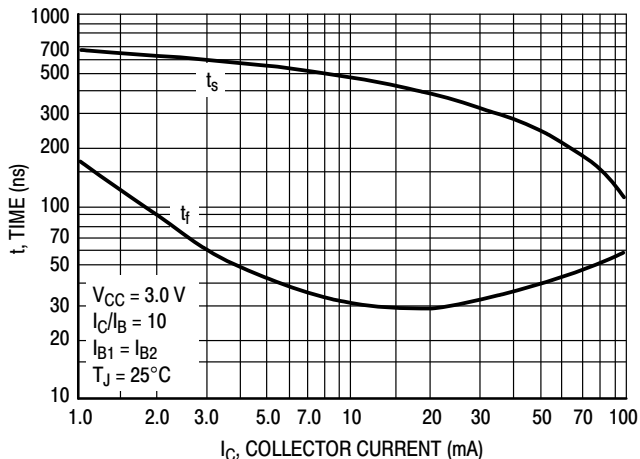## TYPICAL DYNAMIC CHARACTERISTICS

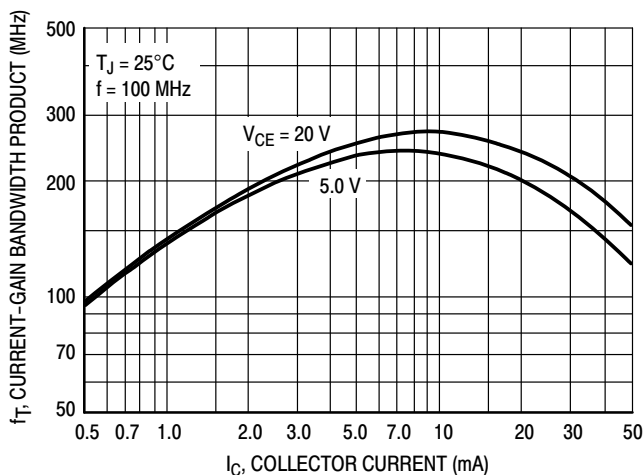Figure 13. Turn−On Time

Figure 14. Turn−Off Time

Figure 15. Current−Gain — Bandwidth Product
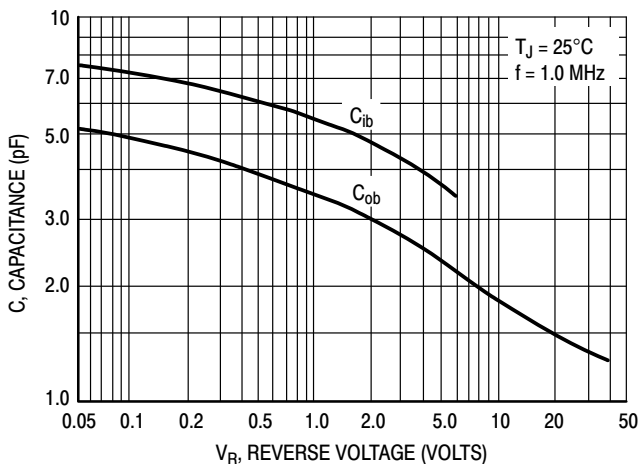
Figure 16. Capacitance
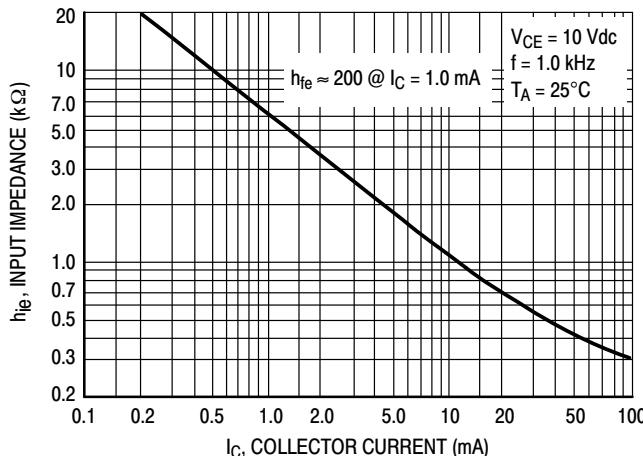
Figure 17. Input Impedance
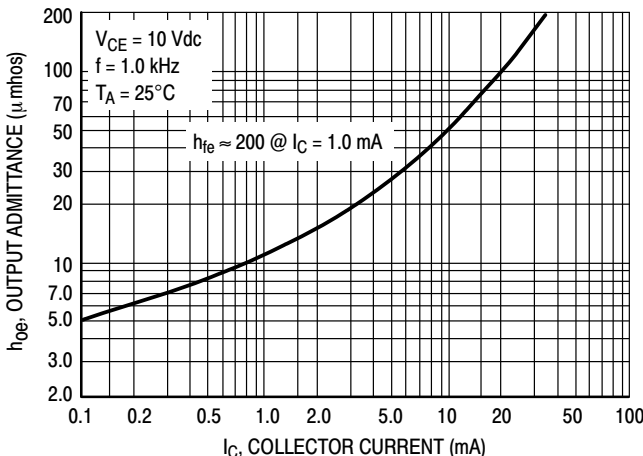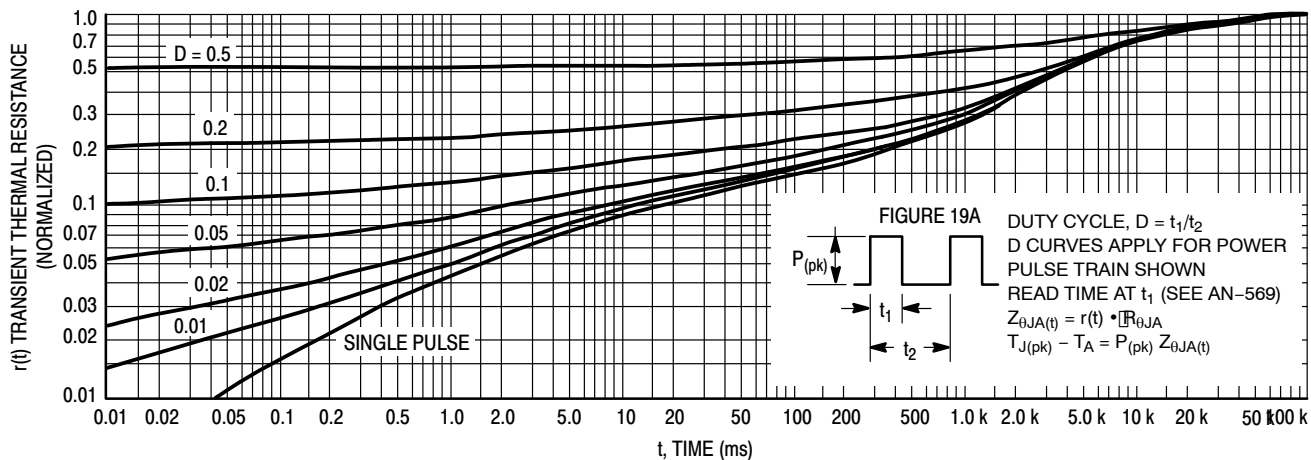
Figure 18. Output Admittance
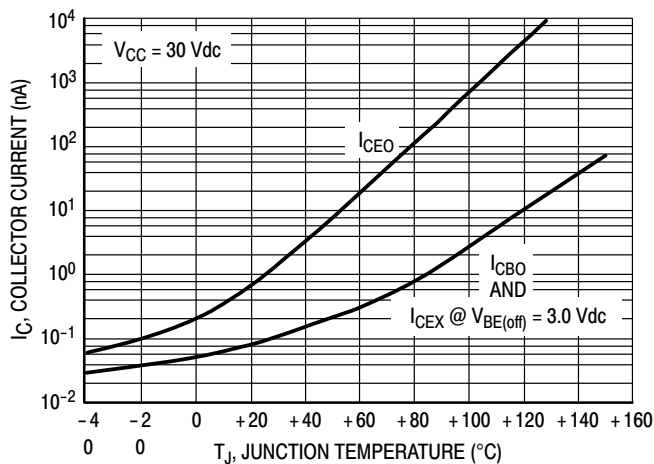
Figure 19. Thermal Response

Figure 19A.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 19A. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 19 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 19 by the steady state value $R_{\theta JA}$.

Example:
The MPS3904 is dissipating 2.0 watts peak under the following conditions:
$t_1 = 1.0$ ms, $t_2 = 5.0$ ms. (D = 0.2)
Using Figure 19 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore
$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88°C$.
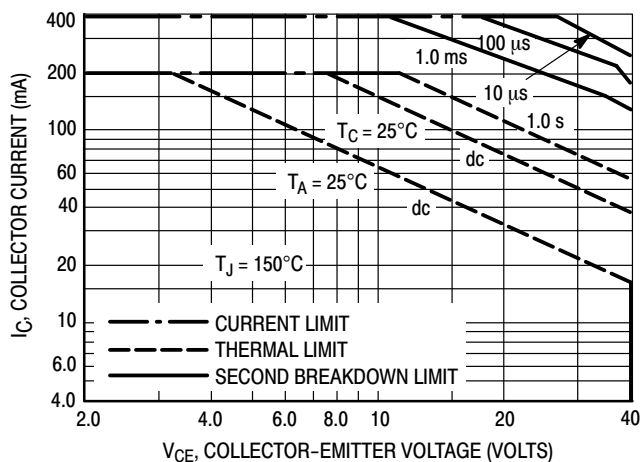
For more information, see AN–569.

Figure 20.

The safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 20 is based upon $T_{J(pk)} = 150°C$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 19. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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PACKAGE DIMENSIONS
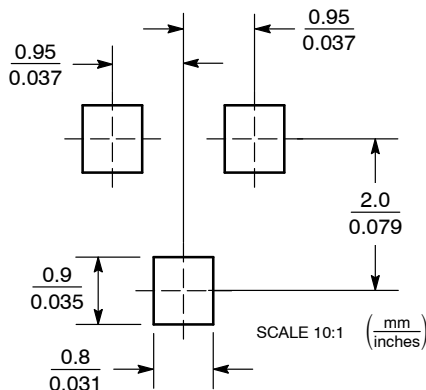
SOT−23 (TO−236)
CASE 318−08
ISSUE AP
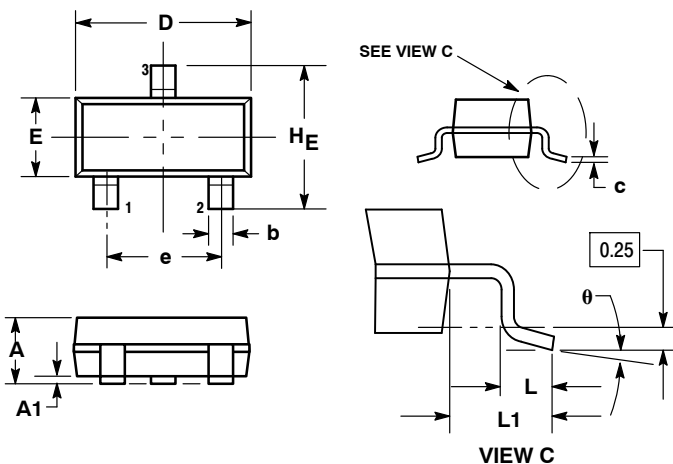
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H$_E$	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SEE VIEW C

VIEW C

SOLDERING FOOTPRINT

$\frac{0.95}{0.037}$

$\frac{0.95}{0.037}$

$\frac{2.0}{0.079}$

$\frac{0.9}{0.035}$

$\frac{0.8}{0.031}$

SCALE 10:1 $\left(\frac{mm}{inches}\right)$

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