BLF578

Power LDMOS transistor

Rev. 4 — 1 December 2016

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 1200 W LDMOS power transistor for broadcast applications and industrial applications in the HF to 500 MHz band.

Table 1. Application information

Mode of operation	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	108	50	1000	26	75
pulsed RF	225	50	1200	24	71

1.2 Features and benefits

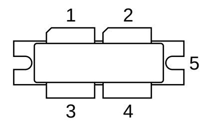
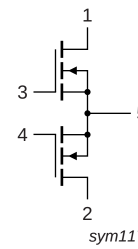
- Typical pulsed performance at frequency of 225 MHz, a supply voltage of 50 V and an I_{Dq} of 40 mA, a t_p of 100 μs with δ of 20 %:
  - Output power = 1200 W
  - Power gain = 24 dB
  - Efficiency = 71 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (10 MHz to 500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF578	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		–0.5	+11	V
I_D	drain current		-	88	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

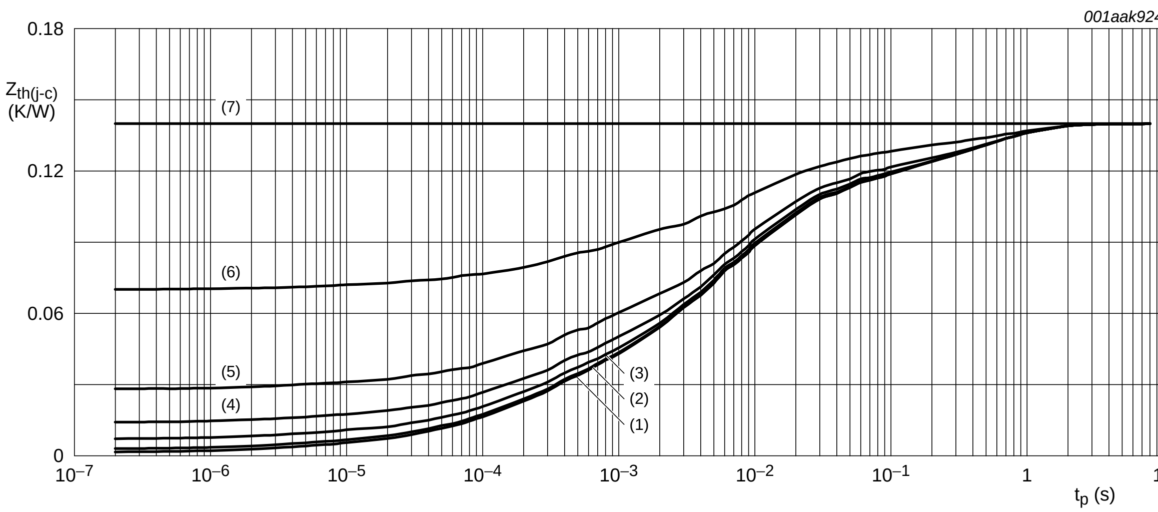
Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 150 °C	[1][2]	0.14	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_j = 150 °C; t_p = 100 μs; δ = 20 %	[3]	0.04	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

[3] See Figure 1.



(1) δ = 1 %

(2) δ = 2 %

(3) δ = 5 %

(4) δ = 10 %

(5) δ = 20 %

(6) δ = 50 %

(7) δ = 100 % (DC)

Fig 1. Transient thermal impedance from junction to case as function of pulse duration

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.5 mA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 500 mA	1.25	1.7	2.25	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 20 mA	0.8	1.3	1.8	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA

Table 6. DC characteristics *...continued*

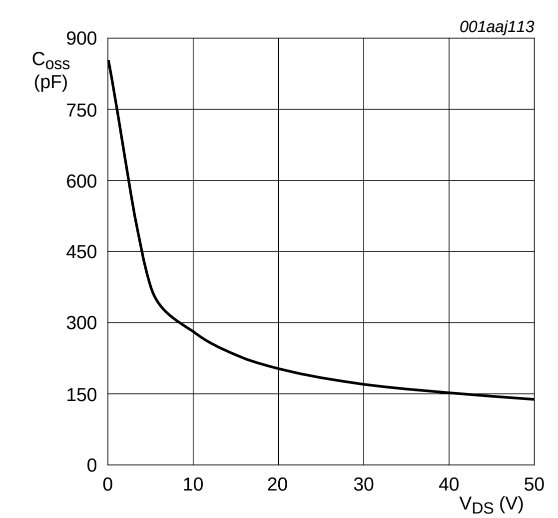
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	58	70	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 16.66 A	-	0.07	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	3	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	403	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	138	-	pF

Table 7. RF characteristics

Mode of operation: pulsed RF; t_p = 100 μs; δ = 20 %; f = 225 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 40 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 1200 W	23	24	25.4	dB
RL_{in}	input return loss	P_L = 1200 W	14	17.5	-	dB
η_D	drain efficiency	P_L = 1200 W	68	71	-	%



V_{GS} = 0 V; f = 1 MHz.

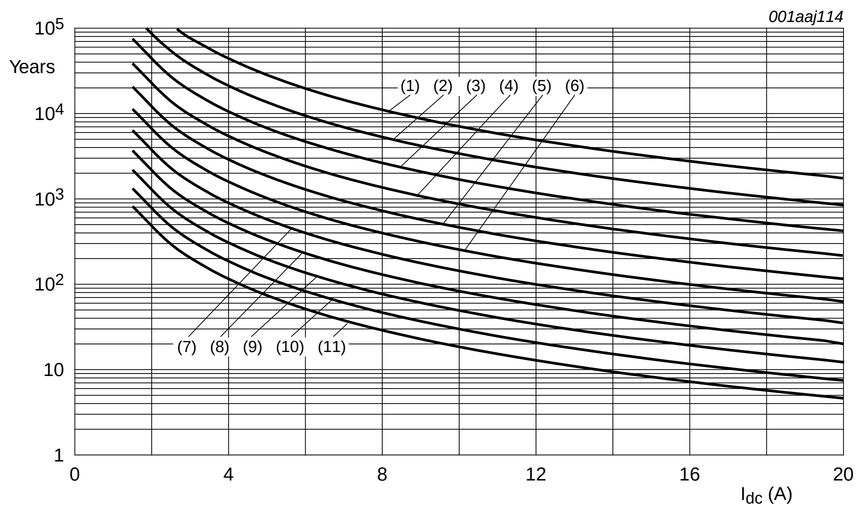
Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

6.1 Ruggedness in class-AB operation

The BLF578 is capable of withstanding a load mismatch corresponding to VSWR = 13 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 40 mA; P_L = 1200 W pulsed; f = 225 MHz.

7. Application information

7.1 Reliability



TTF (0.1 % failure fraction).

The reliability at pulsed conditions can be calculated as follows: TTF (0.1 %) × 1/ δ.

(1) T_j = 100 °C

(2) T_j = 110 °C

(3) T_j = 120 °C

(4) T_j = 130 °C

(5) T_j = 140 °C

(6) T_j = 150 °C

(7) T_j = 160 °C

(8) T_j = 170 °C

(9) T_j = 180 °C

(10) T_j = 190 °C

(11) T_j = 200 °C

Fig 3. BLF578 electromigration (I_D, total device)

8. Test information

8.1 Impedance information

Table 8. Typical impedance

Simulated Z_S and Z_L test circuit impedances.

f	Z_S	Z_L
MHz	Ω	Ω
225	3.2 + j2.6	3.7 – j0.2

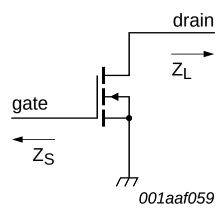
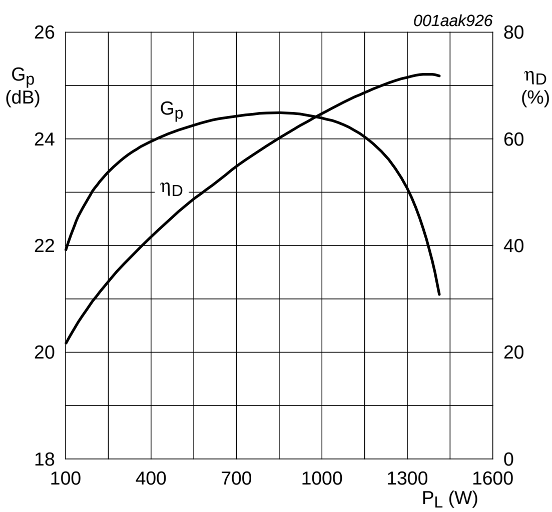


Fig 4. Definition of transistor impedance

8.2 RF performance

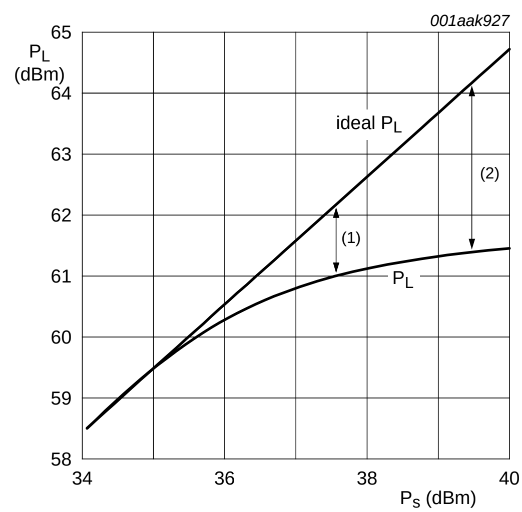
The following figures are measured in a class-AB production test circuit.

8.2.1 1-Tone CW pulsed



V_{DS} = 50 V; I_{Dq} = 40 mA; f = 225 MHz; t_p = 100 μs; δ = 20 %.

Fig 5. Power gain and drain efficiency as function of load power; typical values

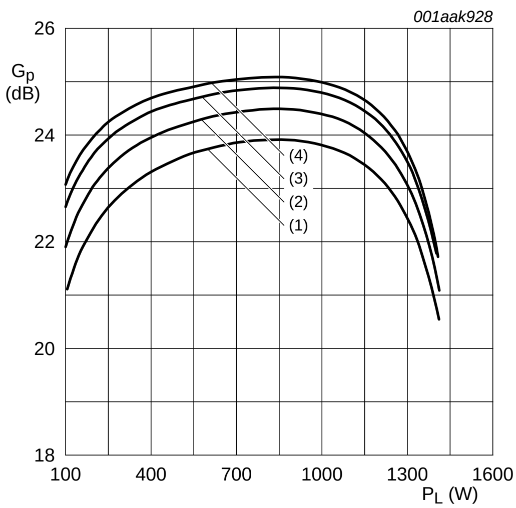


V_{DS} = 50 V; I_{Dq} = 40 mA; f = 225 MHz; t_p = 100 μs; δ = 20 %.

(1) $P_{L(1dB)}$ = 61.0 dBm (1260 W)

(2) $P_{L(3dB)}$ = 61.4 dBm (1400 W)

Fig 6. Load Power as function of source power; typical values



V_{DS} = 50 V; f = 225 MHz; t_p = 100 μs; δ = 20 %.

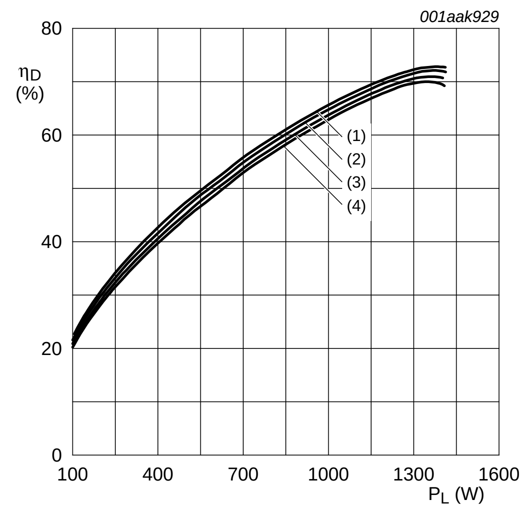
(1) I_{Dq} = 0 mA

(2) I_{Dq} = 40 mA

(3) I_{Dq} = 80 mA

(4) I_{Dq} = 160 mA

Fig 7. Power gain as a function of load power; typical values



V_{DS} = 50 V; f = 225 MHz; t_p = 100 μs; δ = 20 %.

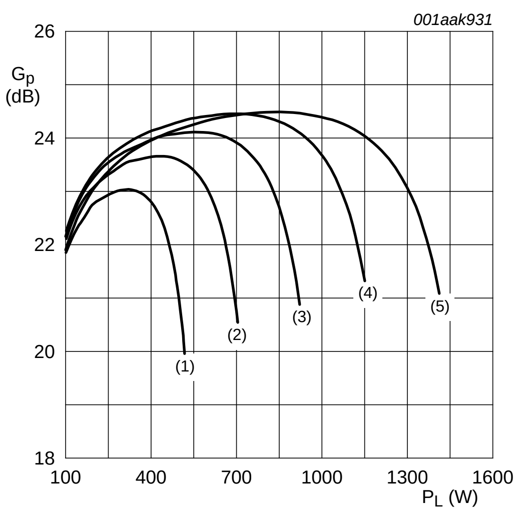
(1) I_{Dq} = 0 mA

(2) I_{Dq} = 40 mA

(3) I_{Dq} = 80 mA

(4) I_{Dq} = 160 mA

Fig 8. Drain efficiency as a function of load power; typical values



I_{Dq} = 40 mA; f = 225 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 30 V

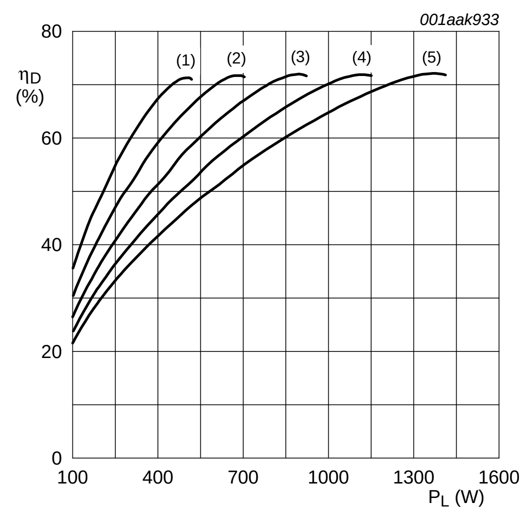
(2) V_{DS} = 35 V

(3) V_{DS} = 40 V

(4) V_{DS} = 45 V

(5) V_{DS} = 50 V

Fig 9. Power gain as a function of load power; typical values



I_{Dq} = 40 mA; f = 225 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 30 V

(2) V_{DS} = 35 V

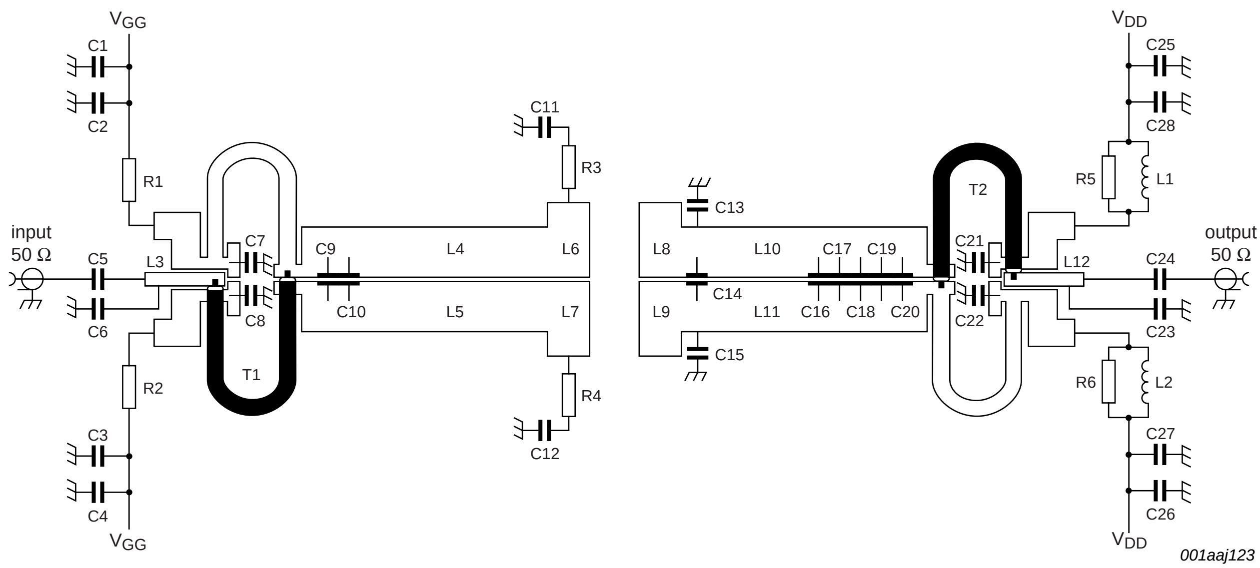
(3) V_{DS} = 40 V

(4) V_{DS} = 45 V

(5) V_{DS} = 50 V

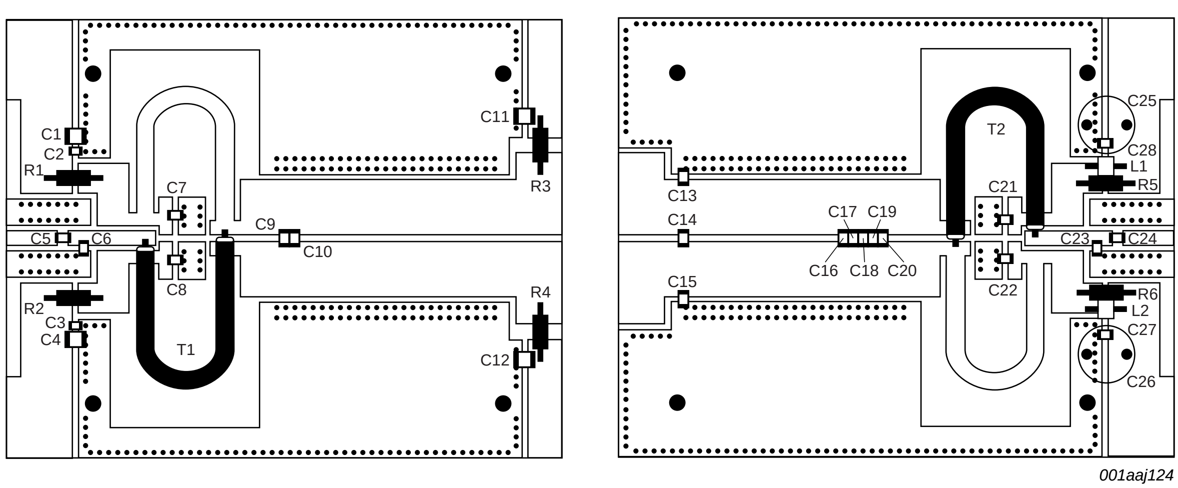
Fig 10. Drain efficiency as a function of load power; typical values

8.3 Test circuit



See Table 9 for a list of components.

Fig 11. Class-AB common-source production test circuit



See Table 9 for a list of components.

Fig 12. Component layout for class-AB production test circuit

Table 9. List of components

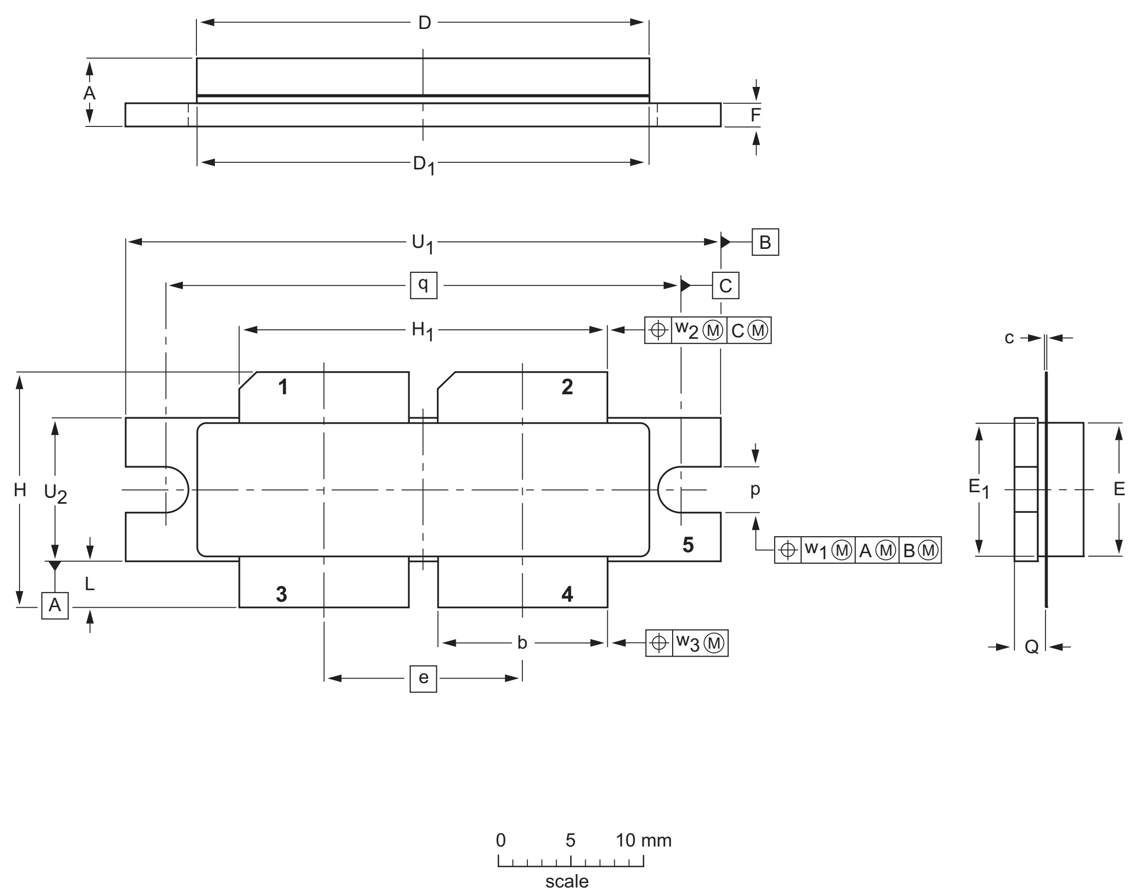
For production test circuit, see Figure 11 and Figure 12.
Printed-Circuit Board (PCB): Rogers 5880; ε_r = 2.2 F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 μm.

Component	Description	Value	Remarks
C1, C2, C11, C12	multilayer ceramic chip capacitor	4.7 μF	TDK4532X7R1E475Mt020U
C2, C3, C27, C28	multilayer ceramic chip capacitor	100 nF	Murata X7R 250 V
C5, C7, C8, C21, C22	multilayer ceramic chip capacitor	1 nF [1]	
C6	multilayer ceramic chip capacitor	30 pF [1]	
C9, C10, C13, C15	multilayer ceramic chip capacitor	62 pF [1]	
C14	multilayer ceramic chip capacitor	36 pF [1]	
C16, C17	multilayer ceramic chip capacitor	24 pF [1]	
C18	multilayer ceramic chip capacitor	30 pF [1]	
C19	multilayer ceramic chip capacitor	27 pF [1]	
C20	multilayer ceramic chip capacitor	9.1 pF [1]	
C23	multilayer ceramic chip capacitor	13 pF [1]	
C24	multilayer ceramic chip capacitor	16 pF [1]	
C25, C26	electrolytic capacitor	220 μF; 63 V	
L1, L2	3 turns 1 mm copper wire	D = 2 mm; length = 3 mm	
L3, L12	stripline	-	(L × W) 15 mm × 2.4 mm
L4, L5, L10, L11	stripline	-	(L × W) 47 mm × 10 mm
L6, L7, L8, L9	stripline	-	(L × W) 8 mm × 15 mm
R1, R2	metal film resistor	2 Ω; 0.6 W	
R3, R4	metal film resistor	20 Ω; 0.6 W	
R5, R6	metal film resistor	1 Ω; 0.6 W	
T1, T2	semi rigid coax	50 Ω; 58 mm	EZ-141-AL-TP-M17

[1] American Technical Ceramics type 100B or capacitor of same quality.

9. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 13. Package outline SOT539A

10. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [1]

[1] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
TTF	Time To Failure
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF578 v.4	20161201	Product data sheet	-	BLF578_3
Modifications:	• Section 10 on page 11: updated Handling information			
BLF578_3	20150901	Product data sheet	-	BLF578_2
BLF578_2	20100204	Product data sheet	-	BLF578_1
BLF578_1	20081211	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contents

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