BAT30F3

Small signal Schottky diode

Features

- very low conduction losses
- negligible switching losses
- low capacitance diode
- Flip Chip, 2-bump package

Complies with the following standards

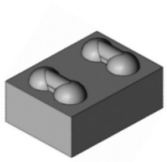
- IEC 61000-4-2 level 1:
  - ±2kV (air discharge)
  - ±2kV (contact discharge)

Description

The BAT30F3 is a Schottky diode in a 2-bump, Flip-Chip package.

This device is specially suited for switching mode applications needing a low forward voltage drop diode.

The electrical parameters are guaranteed across the operating temperature range (- 30 °C to 85 °C).



Flip Chip (2 bumps)

Figure 1. Pin configuration (bump side)

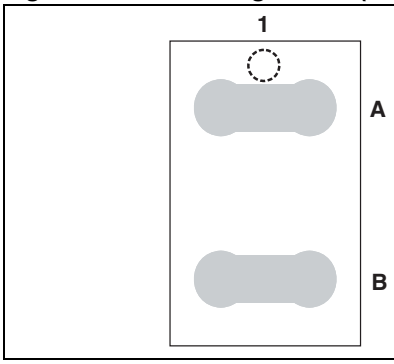
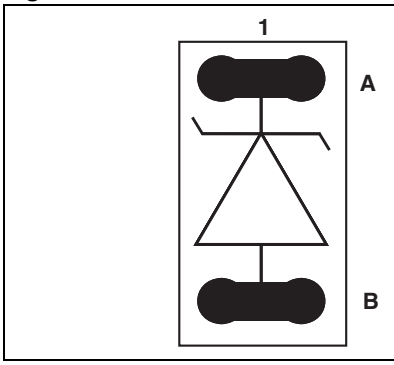


Figure 2. Schematic



1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	Peak pulse voltage: IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge	 ±2 ±2	kV
V_{RRM}	Repetitive peak reverse voltage	20	V
T_{stg}	Storage temperature range(1)	-55 to +150	°C
T_{op}	Operating junction temperature range	-30 to +85	°C

1. $\frac{dPtot}{dTj} < \frac{1}{Rth(j-a)}$ condition to avoid thermal runaway for a diode on its own heatsink

Table 2. Electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_R(1)	Reverse leakage current	25 °C	V_R = 6 V	-	-	2	µA
			V_R = 20 V	-	-	6	
		55 °C	V_R = 6 V	-	-	20	
			V_R = 20 V	-	-	55	
		85 °C	V_R = 6 V	-	-	145	
			V_R = 20 V	-	-	360	
V_F	Forward voltage drop	25 °C	I_F = 0.1 mA	-	-	200	mV
			I_F = 1 mA	-	-	270	
			I_F = 10 mA	-	-	340	
			I_F = 100 mA	-	-	440	
			I_F = 200 mA	-	-	500	
			I_F = 300 mA	-	-	560	
		- 30 °C	I_F = 0.1 mA	-	-	300	
			I_F = 1 mA	-	-	355	
			I_F = 10 mA	-	-	415	
			I_F = 100 mA	-	-	495	
			I_F = 200 mA	-	-	545	
			I_F = 300 mA	-	-	600	

1. Pulse test: t_p = 5 ms, δ < 2%

Figure 3. Leakage current versus reverse applied voltage (typical values)

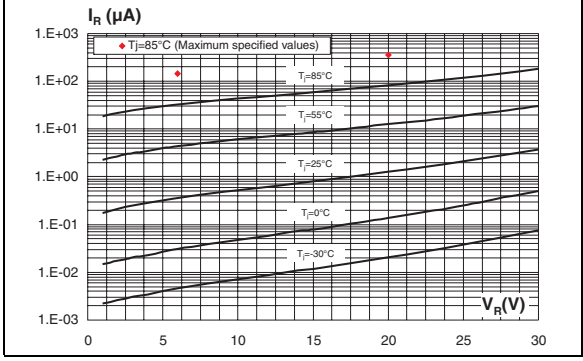


Figure 4. Forward voltage drop versus forward current (typical values, positive temperatures)

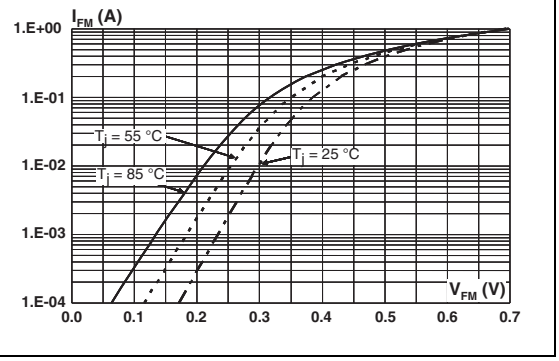


Figure 5. Forward voltage drop versus forward current (typical values, negative temperatures)

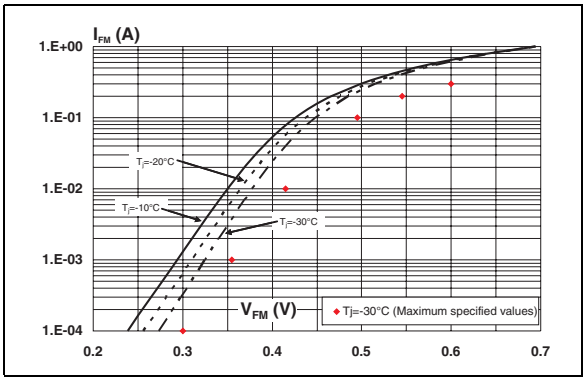
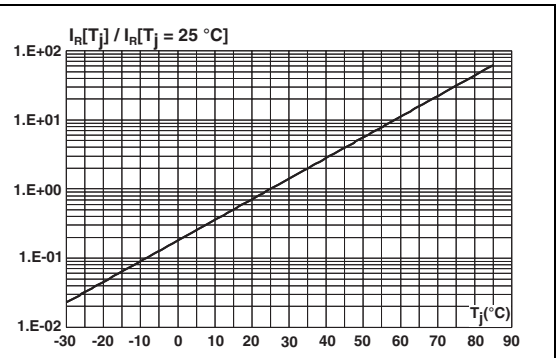
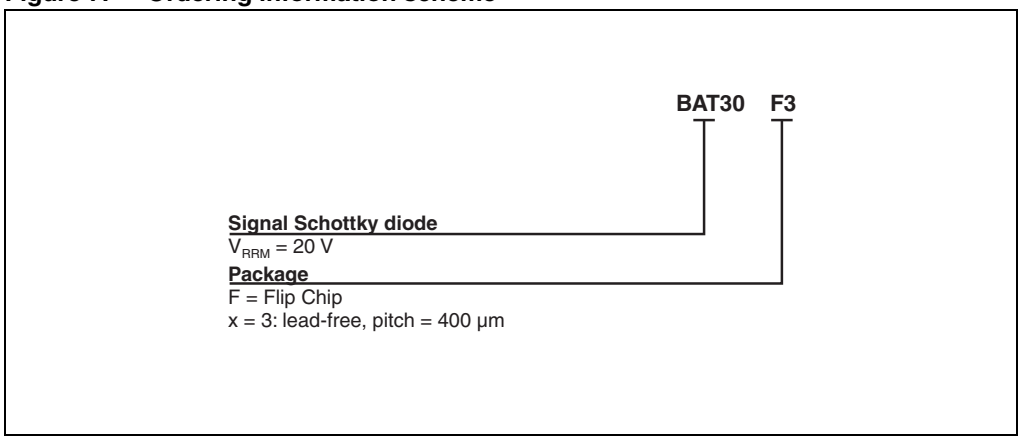


Figure 6. Relative variation of reverse leakage current versus junction temperature (typical values)



2 Ordering information scheme

Figure 7. Ordering information scheme



3 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 8. Package dimensions (dimensions in mm)

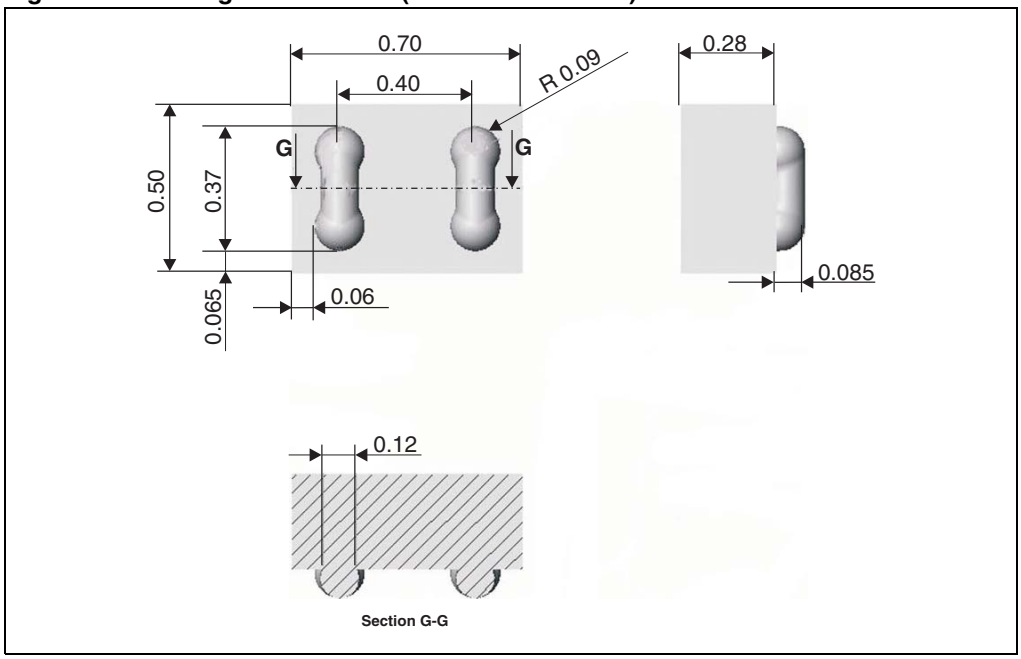
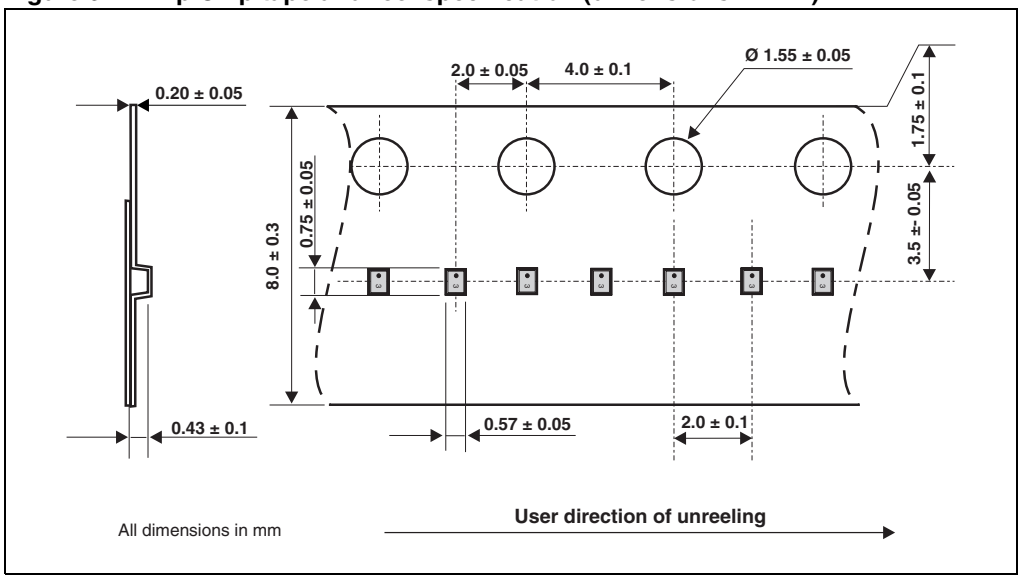


Figure 9. Flip Chip tape and reel specification (dimensions in mm)



4 PCB recommendations

4.1 Design

For optimum electrical performance and highly reliable solder joints, STMicroelectronics recommends the PCB design recommendations listed in *Table 3*.

Table 3. PCB design recommendations for solder bar pitch 400 µm

For NSMD PCB non solder mask defined	Oblong pad: 370 x 180 µm – Micro via SSBU allowed – Micro via SBU to be avoided – Micro via SBU filled (under qualification)
	Track: – Only one track per pad – Maximum track width = 100 µm Track layout must be symmetrical to the die axis (to homogenize stress and welding attraction during reflow assembly)
For SMD PCB solder mask defined	Oblong pad: – Micro via SSBU allowed – Micro via SBU to be avoided – Micro via SBU filled (under qualification)
PCB Pad Finishing	Cu – Ni (2-6 µm) - Au (0.2 µm max)

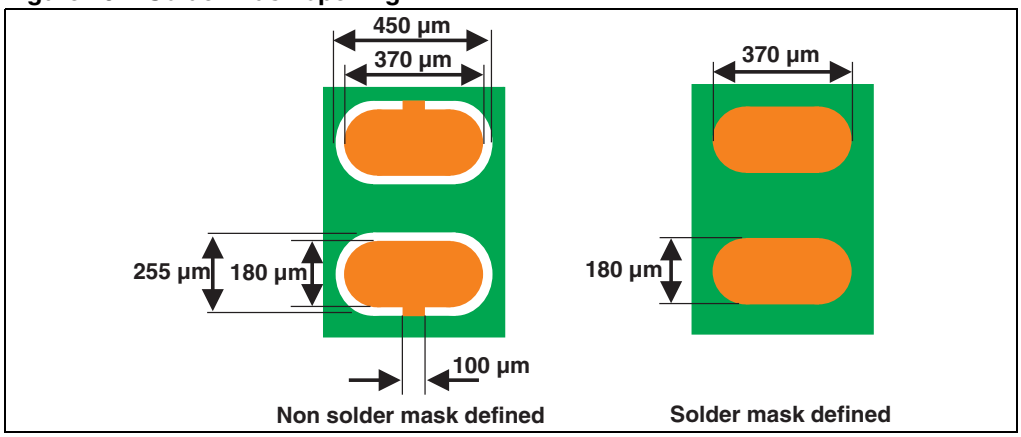
Note: A gold layer finishing on the PCB pad that is too thick (0.2 µm maximum) is not recommended (low joint reliability).

To optimize the natural self centering effect of CSP on the PCB, PCB pad positioning and size have to be properly designed (see *Figure 10*)

Micro vias

An alternative to routing on the top surface is to route out on buried layers. To achieve this, the pads are connected to the lower layers using micro vias. Only SSBU via technology is approved.

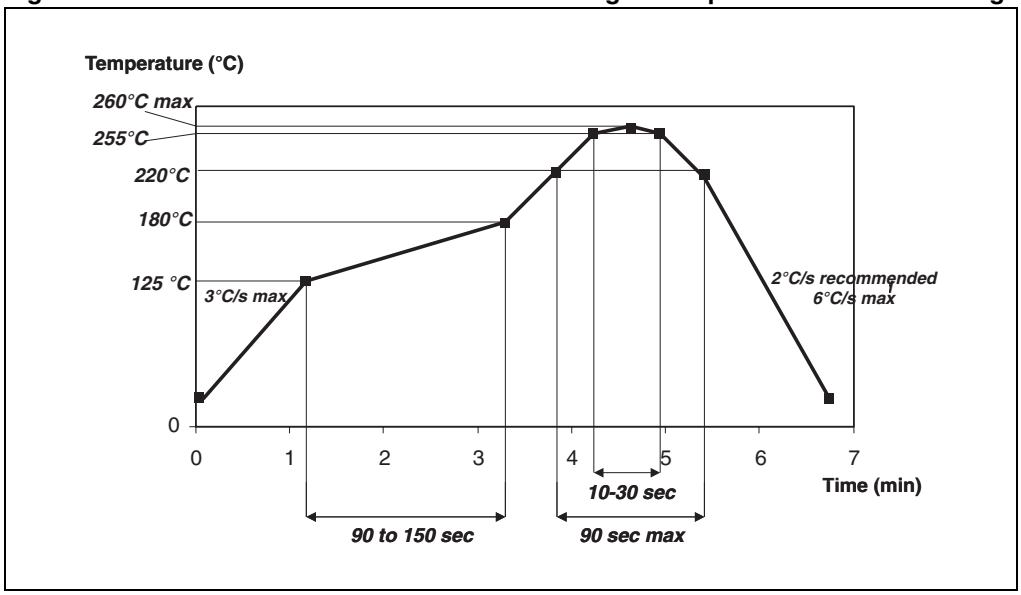
Figure 10. Solder mask opening



4.2 Assembly

For chip scale package mounting on the PCB, STMicroelectronics recommends the use of a solder stencil aperture of 330 x 330 µm maximum and a typical stencil thickness of 75 or 80 µm. Chip scale packages are fully compatible with the use of near eutectic 95.5 Sn, 4 Ag, 0.5 Cu solder paste with no-clean flux. ST's recommendations for chip scale package board mounting are illustrated on the soldering reflow profile shown in *Figure 11*.

Figure 11. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Dwell time in the soldering zone (with temperature higher than 220 °C) has to be kept as short as possible to prevent component and substrate damage. Peak temperature must not exceed 260 °C. Controlled atmosphere (N2 or N2H2) is recommended during the whole reflow, especially above 150 °C.

Chip scale packages are able to withstand three times the previous recommended reflow profile in order to be compatible with a double reflow when SMDs are mounted on both sides of the PCB and one additional repair.

A maximum of three soldering reflows are allowed for these lead-free packages (with repair step included).

The use of a no-clean flux is highly recommended to avoid any cleaning operation. To prevent any bump cracks, ultrasonic cleaning methods are not recommended.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
BAT30F3	3	Flip Chip	0.3 mg	15000	Tape and reel 7”

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
14-Dec-2009	1	Initial release.
21-Oct-2010	2	Updated dot graphic in *Figure 1*.

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