



AP7341

#### 300mA HIGH PSRR LOW NOISE LDO WITH ENABLE

### **Description**

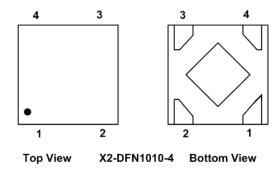
The AP7341 is a low dropout regulator with high output voltage accuracy, low R<sub>DSON</sub>, high PSRR, low output noise and low quiescent current. This regulator is based on a CMOS process.

The AP7341 includes a voltage reference, error amplifier, current limit circuit and an enable input to turn it on and off. With the integrated resistor network fixed output voltage versions can be delivered.

With its low power consumption and line and load transient response the AP7341 is well suited for low power handheld communication equipment.

The AP7341 is packaged in an X2-DFN1010-4 package and allows for smallest footprint and dense PCB layout.

### **Pin Assignments**



PIN1 - V<sub>OUT</sub>, PIN2 - GND, PIN3 - EN, PIN4 - V<sub>IN</sub>

#### **Features**

- Low V<sub>IN</sub> and Wide V<sub>IN</sub> Range: 1.7V to 5.25V
- Guarantee Output Current,150mA
- V<sub>OUT</sub> Accuracy ±1%
- Ripple Rejection 75dB at 1kHz
- Low Output Noise, 60µVrms from 10Hz to 100kHz
- Quiescent Current as Low as 35µA
- V<sub>OUT</sub> Fixed 1.1V to 3.3V
- Totally Lead-Free & and Fully RoHS Compliant (Note 1)
- Halogen and Antimony Free, Green Device (Note 2)

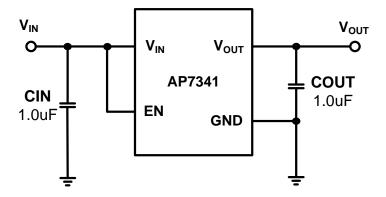
### **Applications**

- Smart Phone/Pad
- RF Supply
- Cameras
- Portable Video
- Portable Media Player
- Wireless Adapter
- Wireless Communication

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

# **Typical Applications Circuit**



**Figure 1 Typical Application Circuit** 



### **Pin Descriptions**

Pin Number	X2-DFN1010-4	Function
1	VOUT	Power Output pin
2	GND	Ground
3	EN	Enable pin. This pin should be driven either high or low and must not be floating. Driving this pin high enables the regulator, while pulling it low puts the regulator into shutdown mode
4	VIN	Power Input pin
_		In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation, then connect this area to GND or leave it open. However do not use it as GND electrode function alone.

## Absolute Maximum Ratings (Note 4) (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
$V_{IN}$	Input Voltage	6.0	V
V <sub>CE</sub>	Input Voltage EN	6.0	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>IN</sub> +0.3	V
l <sub>out</sub>	Output Current	400	mA
P <sub>D</sub>	Power Dissipation	400	mW
T <sub>A</sub>	Operating Temperature	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C

e: 4. a). Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# Recommended Operating Conditions (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V <sub>IN</sub>	Input Voltage	1.7	5.25	V
louт	Output Current	0	300	mA
T <sub>A</sub>	Operating Ambient Temperature	-40	+85	°C

b). Ratings apply to ambient temperature at 25°C. The JEDEC High-K board design used to derive this data was a 2 inch x 2 inch multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

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# $\textbf{Electrical Characteristics} \ (@T_A = +25^{\circ}C, \ V_{EN} = V_{OUT} + 1.0V, \ C_{IN} = C_{OUT} = 1.0 \mu F, \ I_{OUT} = 1.0 mA, \ unless \ otherwise \ specified.)$

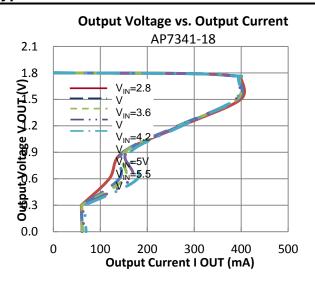
Parameter	Conditions		Min	Тур	Max	Units
Input Voltage	$T_A = -40$ °C to +85°C		1.7	_	5.25	V
	\\ \(\/ - \ \) \(\/ \ \)	T <sub>A</sub> = +25°C	-1	_	1	
Output Voltage Accuracy (Note 11)	$V_{IN} = (V_{OUT-Nom} + 1.0V)$ to 5.25V, $I_{OUT} = 1$ mA to 150mA	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	-1.5	_	+1.5	%
Line Regulation (dV <sub>OUT</sub> /dV <sub>IN</sub> /V <sub>OUT</sub> )	V <sub>IN</sub> = (V <sub>OUT-Nom</sub> +1.0V) to 5.25V, I	OUT = 1.0mA	_	0.02	0.1	%/V
Load Regulation (dV <sub>OUT</sub> /V <sub>OUT</sub> )	V <sub>IN</sub> = V <sub>OUT-Nom</sub> +1.0V, I <sub>OUT</sub> = 1mA	to 300mA	_	15	30	mV
Quiescent Current (Note 6)	I <sub>OUT</sub> = 0mA		_	35	50	uA
STANDBY	V <sub>EN</sub> = 0V (Disabled)		_	0.01	1.0	uA
Output Current	_		300	_	_	mA
Fold-back Short Current (Note 7)	V <sub>OUT</sub> short to ground		_	55	_	mA
PSRR (Note 8)	$V_{IN} = [V_{OUT} + 1V] \ VDC + 0.2Vp-pA$ $V_{OUT} \ge 1.8V$ , $I_{OUT} = 30mA$	C, f = 1kHz	_	75	_	dB
Output Noise Voltage (Notes 8 & 9)	BW = 10Hz to 100kHz, I <sub>OUT</sub> = 30mA		_	60	_	μVrms
		1.1V ≤ V <sub>OUT</sub> < 1.5V	_	0.50	0.62	V
		$1.5V \le V_{OUT} < 1.7V$	_	0.38	0.47	
	450-4	$1.7V \le V_{OUT} < 2.0V$	_	0.34	0.42	
	$I_{OUT} = 150 \text{mA}$	$2.0V \le V_{OUT} < 2.5V$	_	0.28	0.36	
Dropout Voltage (Note 5)		2.5V ≤ V <sub>OUT</sub> < 2.8V	_	0.22	0.30	
(Note 3)		2.8V ≤ V <sub>OUT</sub> ≤ 3.3V	_	0.21	0.27	
	I <sub>OUT</sub> = 300mA	V <sub>OUT</sub> = 1.8V	_	0.50	0.65	
		V <sub>OUT</sub> = 2.5V	_	0.37	0.48	
		V <sub>OUT</sub> = 3.3V	_	0.30	0.40	
Output Voltage Temperature Coefficient	I <sub>OUT</sub> = 30mA, T <sub>A</sub> = -40°C to +85°C		_	±30	_	ppm/°C
EN Input Low Voltage	_		0	_	0.5	V
EN Input High Voltage			1.3	_	5.25	V
EN Input Leakage	V <sub>EN</sub> = 0, V <sub>IN</sub> = 5.0V or V <sub>EN</sub> = 5.0V, V <sub>IN</sub> = 0V		-1.0	_	+1.0	μA
On Resistance of N-Channel for Auto-Discharge (Note 10)	V <sub>IN</sub> = 4.0V V <sub>EN</sub> = 0V (Disabled)		_	30	_	Ω

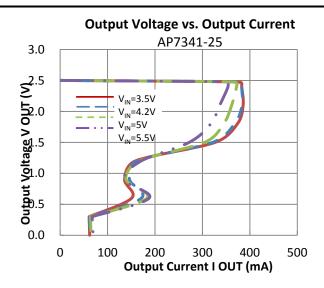
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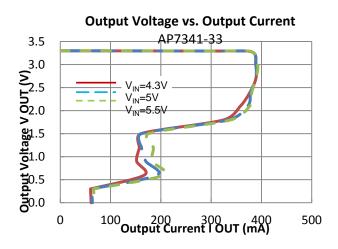
- 5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
- 6. Quiescent current is defined here is the difference in current between the input and the output. 7. Short circuit current is measured with VOUT pulled to GND.
- 8. This specification is guaranteed by design.
  9. To make sure lowest environment noise minimizes the influence on noise measurement.
- AP7341 has 2 options for output, Built-in discharge and non-discharge
   Potential multiple grades based on following output voltage accuracy.

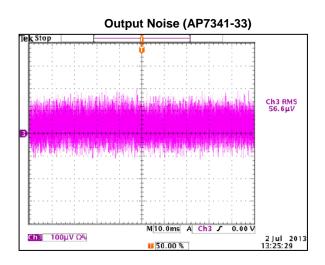


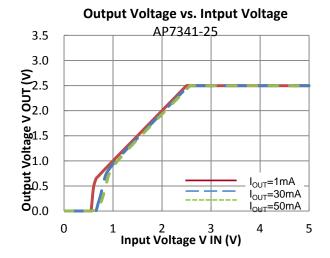
## **Typical Characteristics**

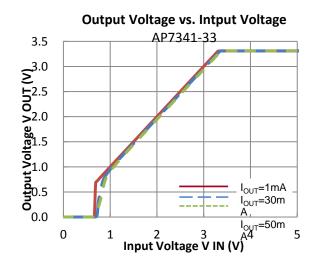




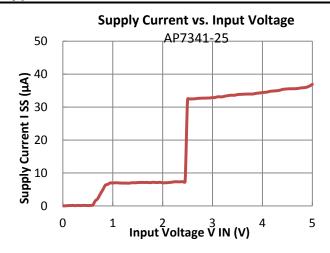


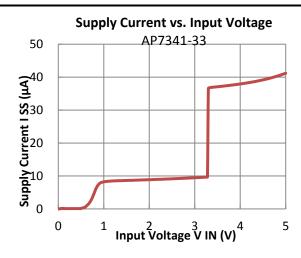


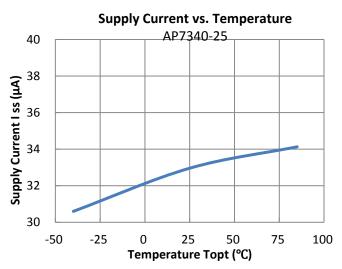


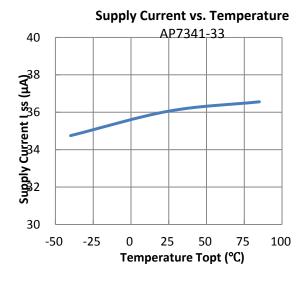


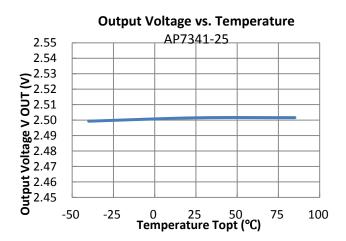


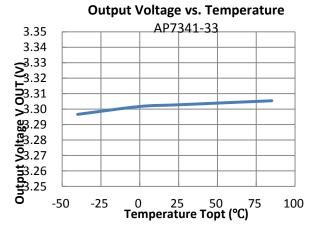




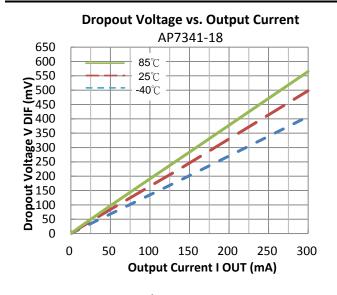


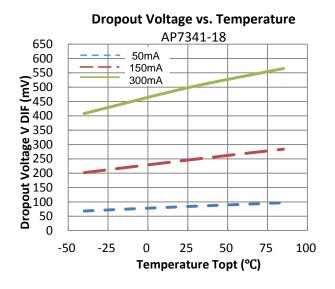


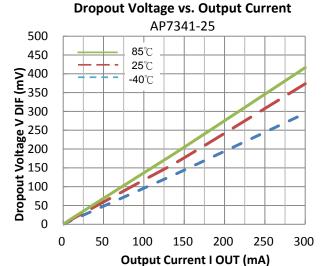


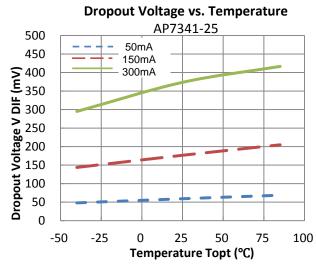


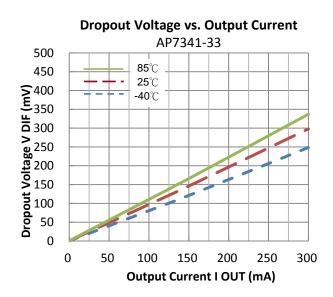


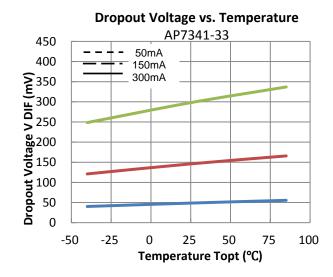




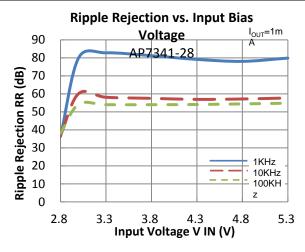


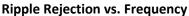


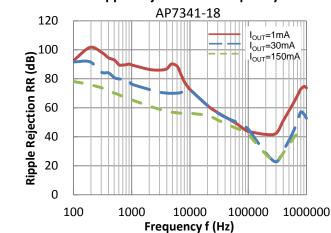




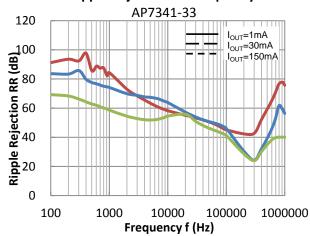


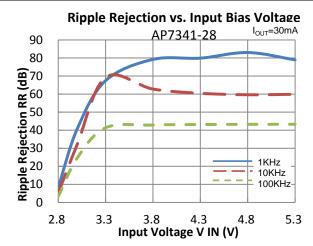




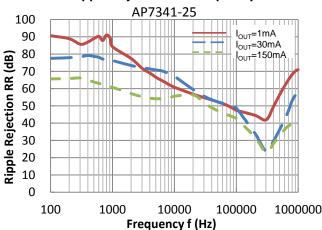


### Ripple Rejection vs. Frequency

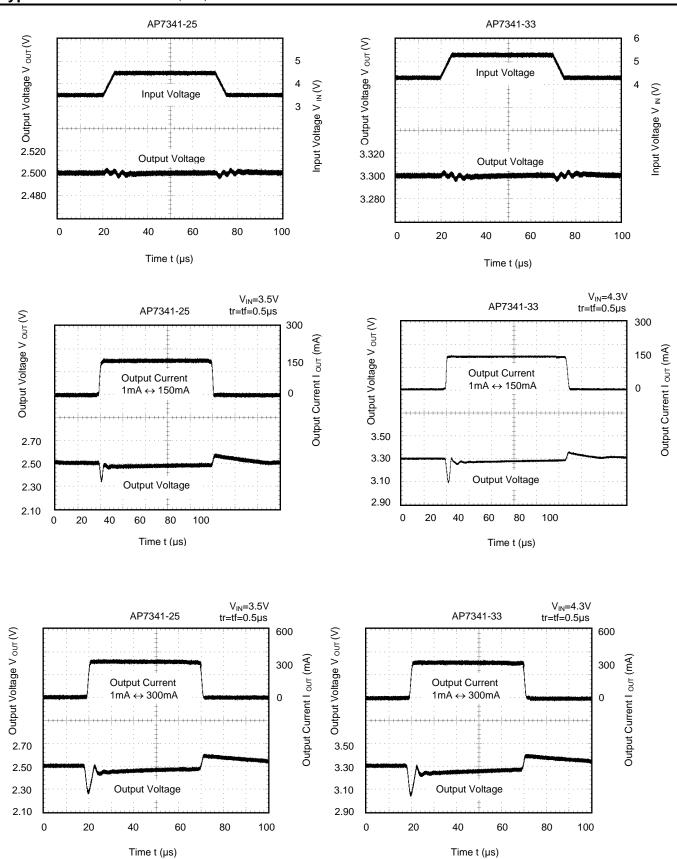




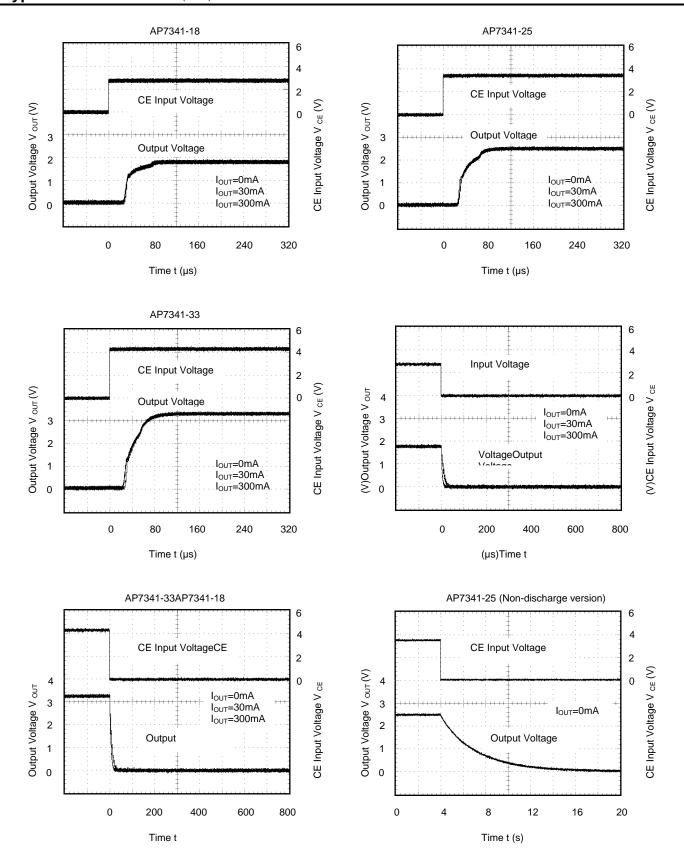
### Ripple Rejection vs. Frequency













### **Application Information**

#### **Output Capacitor**

An output capacitor (C<sub>OUT</sub>) is needed to improve transient response and maintain stability. The AP7341 is stable with very small ceramic output capacitors. The ESR (equivalent series resistance) and capacitance drives the selection. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors. It is recommended to place ceramic capacitors as close as possible to the load and the ground pin and care should be taken to reduce the impedance in the layout.

#### Input Capacitor

To prevent the input voltage from dropping during load steps it is recommended to utilize an input capacitor ( $C_{IN}$ ). A minimum 0.47 $\mu$ F ceramic capacitor is recommended between  $V_{IN}$  and GND pins to decouple input power supply glitch. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both  $V_{IN}$  and GND pins.

#### **Enable Control**

The AP7341 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to  $V_{IN}$  pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section.

#### **Short Circuit Protection**

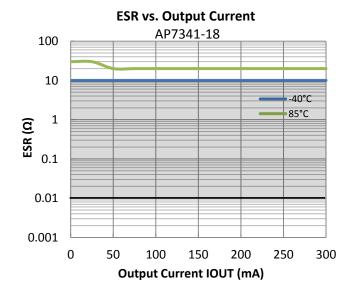
When  $V_{OUT}$  pin is short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 60mA. This feature protects the regulator from over-current and damage due to overheating.

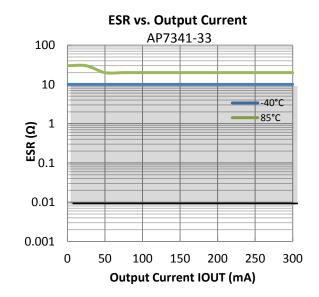
#### Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from  $V_{IN}$  to  $V_{OUT}$ , and load circuit.

## **ESR vs. Output Current**

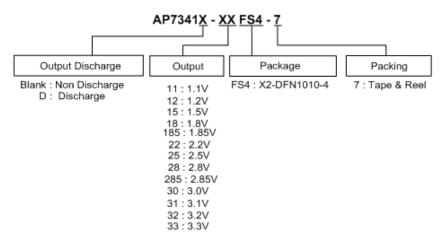
Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. The relations between I<sub>OUT</sub> (Output Current) and ESR of an output capacitor are shown below. The stable region is marked as the hatched area in the graph. Measurement conditions: Frequency Band: 10Hz to 2MHz, Temperature: -40°C to +85°C







## **Ordering Information** (Note 12)



Part Number	Package	age Backgring	7" Tape and Reel		
Part Number	Code	Packaging	Quantity	Part Number Suffix	
AP7341-XXFS4-7	FS4	X2-DFN1010-4	5000/Tape & Reel	-7	
AP7341D-XXFS4-7	FS4	X2-DFN1010-4	5000/Tape & Reel	-7	

Note: 12. For packaging details, go to our website at http://www.diodes.com/products/packages.html

### **Marking Information**

#### (1) X2-DFN1010-4

(Top View)



XX : Identification Code

Y : Year : 0~9

 $\overline{W}$ : Week : A $^{\sim}$ Z : 1 $^{\sim}$ 26 week;

a~z: 27~52 week; z represents

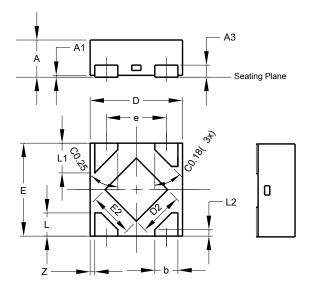
52 and 53 week  $\underline{X}$ : A $^{\sim}$ Z: Internal code

Part Number	Package	Identification Code
AP7341-11FS4-7	X2-DFN1010-4	TF
AP7341-12FS4-7	X2-DFN1010-4	T2
AP7341-15FS4-7	X2-DFN1010-4	T3
AP7341-18FS4-7	X2-DFN1010-4	T4
AP7341-185FS4-7	X2-DFN1010-4	T5
AP7341-22FS4-7	X2-DFN1010-4	TH
AP7341-25FS4-7	X2-DFN1010-4	T6
AP7341-28FS4-7	X2-DFN1010-4	T7
AP7341-285FS4-7	X2-DFN1010-4	T8
AP7341-30FS4-7	X2-DFN1010-4	Т9
AP7341-31FS4-7	X2-DFN1010-4	TC
AP7341-32FS4-7	X2-DFN1010-4	TD
AP7341-33FS4-7	X2-DFN1010-4	TE
AP7341D-11FS4-7	X2-DFN1010-4	UF
AP7341D-12FS4-7	X2-DFN1010-4	U2
AP7341D-15FS4-7	X2-DFN1010-4	U3
AP7341D-18FS4-7	X2-DFN1010-4	U4
AP7341D-185FS4-7	X2-DFN1010-4	U5
AP7341D-22FS4-7	X2-DFN1010-4	UH
AP7341D-25FS4-7	X2-DFN1010-4	U6
AP7341D-28FS4-7	X2-DFN1010-4	U7
AP7341D-285FS4-7	X2-DFN1010-4	U8
AP7341D-30FS4-7	X2-DFN1010-4	U9
AP7341D-31FS4-7	X2-DFN1010-4	UC
AP7341D-32FS4-7	X2-DFN1010-4	UD
AP7341D-33FS4-7	X2-DFN1010-4	UE



## Package Outline Dimensions (All dimensions in mm.)

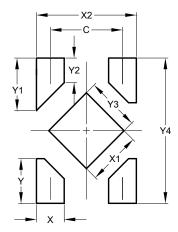
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



X2-DFN1010-4			
Dim	Min	Max	Тур
Α	-	0.40	0.39
A1	0.00	0.05	0.02
A3	-	-	0.13
b	0.20	0.30	0.25
D	0.95	1.05	1.00
D2	0.38	0.58	0.48
Е	0.95	1.05	1.00
E2	0.38	0.58	0.48
е	-	-	0.65
L	0.20	0.30	0.25
L1	0.27	0.37	0.32
L2	0.02	0.12	0.07
Z	-	-	0.050
All Dimensions in mm			

# **Suggested Pad Layout**

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

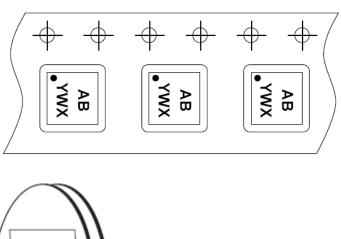


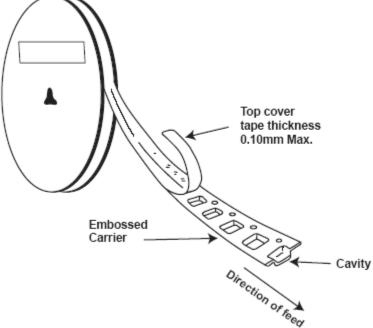
Dimensions	Value (in mm)			
С	0.650			
X	0.250			
X1	0.480			
X2	0.900			
Y	0.400			
Y1	0.470			
Y2	0.220			
Y3	0.480			
Y4	1.300			



## **Tape Orientation**

#### For X2-DFN1010-4





Note: 13. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf



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