

BGA3031

DOCSIS 3.0 plus upstream amplifier

Rev. 3 — 20 November 2014

Product data sheet

1. General description

The BGA3031 is an upstream amplifier meeting the Data Over Cable Service Interface Specifications (DOCSIS 3.0). It is designed for cable modem, CATV set top box and VoIP modem applications. The device operates from 5 MHz to 85 MHz. The BGA3031 provides 58 dB gain control range in 1 dB increments with high incremental accuracy. Its maximum gain setting delivers 34 dB voltage gain and a superior linear performance.

It supports high output power levels, exceeding the DOCSIS 3.0 power levels while minimizing distortion and output noise levels. The BGA3031 is capable of transmitting 1 to 8 64-QAM and 1 to 8 QPSK modulated carriers while meeting the DOCSIS 3.0 ACLR specification under DOCSIS 3.0 + 4 dB conditions.

The BGA3031 operates at 5 V supply. The gain is controlled via a 3-wire serial interface. The current consumption can be reduced in 4 steps via the serial interface. This enables the user to optimize between DC power efficiency and linearity. In addition the current is automatically reduced at lower gain settings while preserving the linearity performance. In disable mode the device draws typical 6 mA while it still can be programmed to new gain and current settings.

The BGA3031 is housed in 20 pins 5 mm × 5 mm leadless HVQFN package.

2. Features and benefits

- 58 dB gain control range in 1 dB steps using a 3-wire serial interface
- 5 MHz to 85 MHz frequency operating range
- ± 0.2 dB incremental gain step accuracy
- Maximum voltage gain 34 dB
- Excellent IMD3 of -70 dBc at 64 dBmV output power
- Excellent second harmonic level of -80 dBc at 64 dBmV output power
- Excellent third harmonic level of -67 dBc at 64 dBmV output power
- Excellent noise figure of 3.5 dB at maximum gain
- Capable of transmitting 1 to 8 64-QAM modulated carriers while meeting the DOCSIS 3.0 specification under DOCSIS 3.0 + 4 dB conditions (61 dBmV total output power)
- Capable of transmitting 1 to 8 QPSK modulated carriers while meeting the DOCSIS 3.0 specification under DOCSIS 3.0 + 4 dB conditions (65 dBmV total output power)
- 5 V single supply operation
- Excellent ESD protection at all pins
- Unconditionally stable



- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

3. Applications

- DOCSIS 3.0 and DOCSIS 3.0 + 4 dB cable modems
- VoIP modems
- Set-top boxes

4. Quick reference data

Table 1. Quick reference data

Typical values at $V_{CC} = 5\text{ V}$; current setting = 3; $T_{amb} = 25\text{ °C}$; $Z_i = 200\ \Omega$; $Z_o = 75\ \Omega$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--|---|-----|-----|-----|------|
| I _{CC} | supply current | transmit-enable mode; TX_EN = HIGH | - | 325 | - | mA |
| | | transmit-disable mode; TX_EN = LOW | - | 6.0 | - | mA |
| G _v | voltage gain | gain code = 111111 [1][2] | - | 34 | - | dB |
| NF | noise figure | transmit-enable mode; gain code = 111111 | - | 3.5 | - | dB |
| α _{2H} | second harmonic level | P _i = 30 dBmV; P _L = 64 dBmV into 75 Ω differential impedance | - | -80 | - | dBc |
| α _{3H} | third harmonic level | P _i = 30 dBmV; P _L = 64 dBmV into 75 Ω differential impedance | - | -67 | - | dBc |
| IMD3 | third-order intermodulation distortion | P _i = 27 dBmV per tone; P _L = 61 dBmV per tone into 75 Ω differential impedance | - | -70 | - | dBc |
| P _{L(1dB)} | output power at 1 dB gain compression | signal | - | 74 | - | dBmV |

[1] Voltage gain does not include loss due to input and output transformers.

[2] P_i = 30 dBmV.

Table 2. ACLR quick reference data

Typical values at $V_{CC} = 5\text{ V}$; current setting = 3; $T_{amb} = 25\text{ °C}$; $Z_i = 200\ \Omega$; $Z_o = 75\ \Omega$; channel bandwidth = 1280 kHz; integration bandwidth = 1280 kHz; $f = 5\text{ MHz to }85\text{ MHz}$, unless otherwise specified.

| Symbol | Parameter | Conditions | DOCSIS 3.0 spec. | Min | Typ | Max | Unit |
|----------------------------------|--------------------------------|--|------------------|-----|-----|-----|------|
| DOCSIS 3.0 + 4 dB; 64-QAM | | | | | | | |
| ACLR | adjacent channel leakage ratio | P _i = 29 dBmV; P _L = 61 dBmV | | | | | |
| | | 1 input channel | -50 | - | -68 | - | dBc |
| | | 2 input channels | -47 | - | -62 | - | dBc |
| | | 4 input channels | -44 | - | -58 | - | dBc |
| | | 8 input channels | - | - | -56 | - | dBc |
| DOCSIS 3.0 + 4 dB; QPSK | | | | | | | |
| ACLR | adjacent channel leakage ratio | P _i = 33 dBmV; P _L = 65 dBmV | | | | | |
| | | 1 input channel | -50 | - | -66 | - | dBc |
| | | 2 input channels | -47 | - | -58 | - | dBc |
| | | 4 input channels | -44 | - | -50 | - | dBc |
| | | 8 input channels | - | - | -42 | - | dBc |

5. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|----------|
| | Name | Description | Version |
| BGA3031 | HVQFN20 | plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 × 5 × 0.85 mm | SOT662-1 |

6. Functional diagram

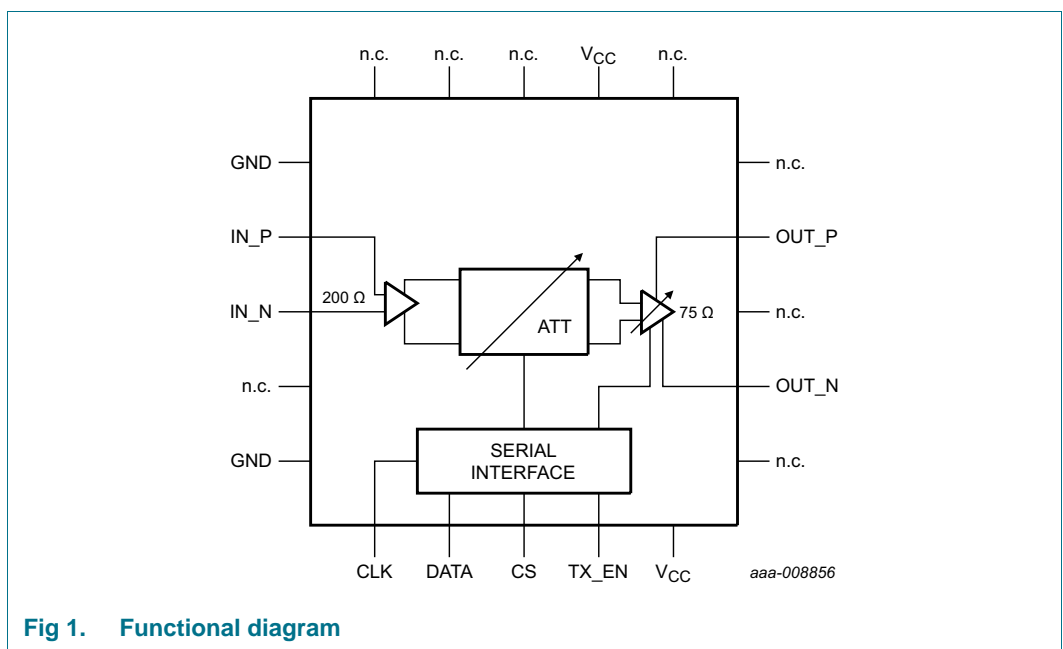


Fig 1. Functional diagram

7. Pinning information

7.1 Pinning

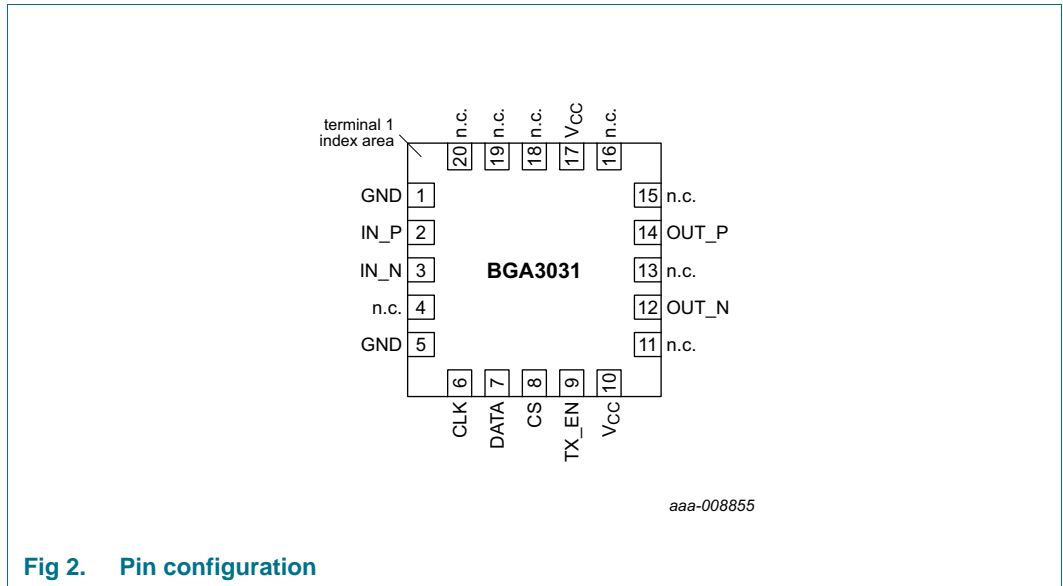


Fig 2. Pin configuration

7.2 Pin description

Table 4. Pin description

| Symbol | Pin | Description |
|-----------------|-----|--|
| GND | 1 | ground |
| IN_P | 2 | amplifier input + |
| IN_N | 3 | amplifier input – |
| n.c. | 4 | not connected |
| GND | 5 | ground |
| CLK | 6 | clock |
| DATA | 7 | data |
| CS | 8 | chip select |
| TX_EN | 9 | transmit enable |
| V _{CC} | 10 | supply voltage for serial interface |
| n.c. | 11 | not connected |
| OUT_N | 12 | amplifier output – |
| n.c. | 13 | not connected |
| OUT_P | 14 | amplifier output + |
| n.c. | 15 | not connected |
| n.c. | 16 | not connected |
| V _{CC} | 17 | supply voltage for Variable Gain Amplifier (VGA) |
| n.c. | 18 | not connected |

Table 4. Pin description ...continued

| Symbol | Pin | Description |
|--------|-----|---------------|
| n.c. | 19 | not connected |
| n.c. | 20 | not connected |
| Paddle | | ground |

8. Functional description

8.1 Logic programming

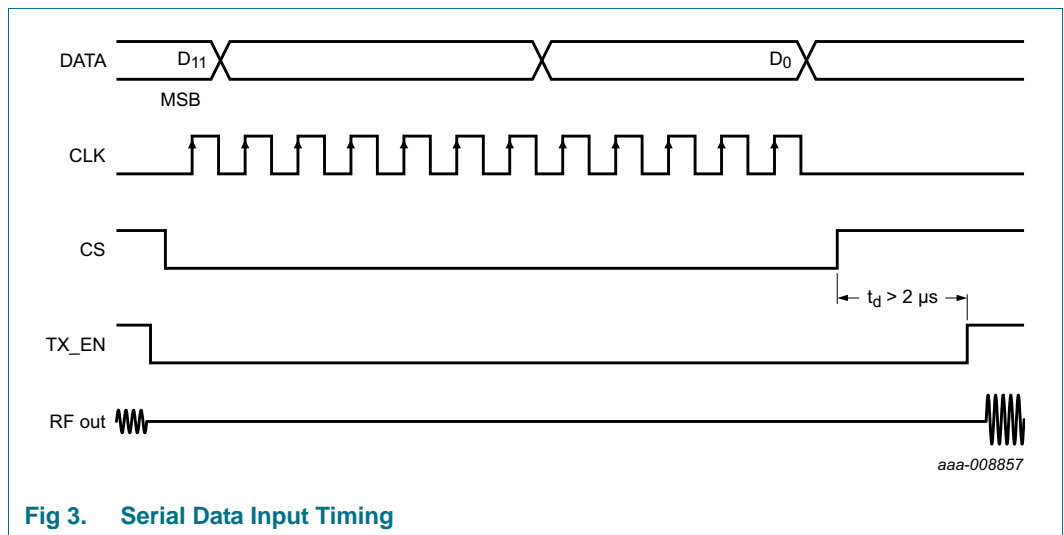
The programming word is set through a shift register via the data, clock and chip select lines. The data is entered in order with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The chip select line must be LOW for the duration of the data entry, then set HIGH to latch the shift register. The rising edge of the clock pulse shifts each data value into the register.

Table 5. Programming register

| Data bit | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------------|----|---|---|--------------------------------|------|---|------|------|------|------|------|
| Function | Register address | | | | Current setting ^[1] | | attenuation (gain) setting ^[2] | | | | | |
| Initialize | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Set gain | 0 | 0 | 0 | 0 | C[1] | C[0] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] |

[1] For current bit settings see [Table 7](#).

[2] For gain bit settings see [Table 6](#).



8.2 Register settings

8.2.1 Register address

Only addresses 0000 and 0001 are used. Using any other addresses will not affect the VGA.

8.2.2 Gain/attenuator setting

The gain shall be controlled via the 3-wire bus. Data bits D0 through D5 set the gain/attenuator level, with 111111 being the min attenuation setting, and 000101 being the max attenuation setting. A new gain/attenuator setting can be loaded while the VGA is on (transmit-enable), but shall not take effect until transmit-enable transitions from LOW to HIGH.

Table 6. Gain settings

| Gain setting G[5:0] | | Typical gain |
|----------------------------|------------------------|--------------|
| binary notation | decimal notation | (dB) |
| 000000 to 000101 | 0 to 5 | -24 |
| 000110 [1] | 6 [1] | -23 |
| 111110 [1] | 62 [1] | 33 |
| 111111 [1] | 63 [1] | 34 |

[1] With every increment of the gain setting between 000110 (6) and 111111 (63) the typical gain will increase accordingly.

8.2.3 Output stage current setting

The current (of the output stage) shall be controlled via the 3-wire bus. Data bits D6 and D7 set the current. Setting 11 will set the maximum current for maximum linearity. The current can be lowered for improved efficiency at lower output power levels, or lower linearity requirements. Setting 00 will set the minimum current. A new current setting can be loaded while the VGA is on (transmit-enable), but shall not take effect until transmit-enable transitions from LOW to HIGH.

Table 7. Supply current settings

At gain setting 63.

| Current setting C[1:0] | | Typical supply current |
|------------------------|------------------|------------------------|
| binary notation | decimal notation | (mA) |
| 00 | 0 | 215 |
| 01 | 1 | 260 |
| 10 | 2 | 290 |
| 11 | 3 | 325 |

The current is automatically reduced at lower gain settings while preserving the linearity performance.

Table 8. Supply current versus gain setting

| Gain setting G[5:0] | | Typical current (mA) | | | |
|---------------------|------------------|------------------------|------------------------|------------------------|------------------------|
| binary notation | decimal notation | Current setting C[1:0] | Current setting C[1:0] | Current setting C[1:0] | Current setting C[1:0] |
| | | 00 (decimal = 0) | 01 (decimal = 1) | 10 (decimal = 2) | 11 (decimal = 3) |
| 111111 | 63 | 215 | 260 | 290 | 325 |
| 110111 | 55 | 215 | 260 | 290 | 325 |
| 110110 | 54 | 165 | 190 | 200 | 215 |
| 110001 | 49 | 165 | 190 | 200 | 215 |
| 110000 | 48 | 135 | 150 | 160 | 160 |
| 101000 | 40 | 135 | 150 | 160 | 160 |
| 100111 | 39 | 120 | 125 | 125 | 125 |
| 000101 | 5 | 120 | 125 | 125 | 125 |

8.3 Tx enable / Tx disable

The amplifier can be disabled or enabled by making TX_EN (pin 9) LOW or HIGH. A LOW to HIGH Tx enable transition will activate new programmed settings. If no new settings are programmed the last programmed setting will be re-activated.

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Absolute Maximum Ratings are given as Limiting Values of stress conditions during operation, that must not be exceeded under the worst probable conditions.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|---------------------------------|--|----------|------|------|
| V _{CC} | supply voltage | | - | 6.0 | V |
| V _I | input voltage | on pin IN_P | -0.5 | +6.0 | V |
| | | on pin IN_N | -0.5 | +6.0 | V |
| | | on pin CLK | [1] -0.5 | +6.0 | V |
| | | on pin DATA | [1] -0.5 | +6.0 | V |
| | | on pin CS | [1] -0.5 | +6.0 | V |
| | | on pin TX_EN | [1] -0.5 | +6.0 | V |
| | | on pin OUT_N | -0.5 | +6.0 | V |
| | | on pin OUT_P | -0.5 | +6.0 | V |
| P _{i(max)} | maximum input power | | - | 40 | dBmV |
| T _{amb} | ambient temperature | | -40 | +85 | °C |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| T _j | junction temperature | | - | 150 | °C |
| V _{ESD} | electrostatic discharge voltage | Human Body Model (HBM); According JEDEC standard 22-A114E | - | 4000 | V |
| | | Charged Device Model (CDM); According JEDEC standard 22-C101B | - | 2000 | V |

[1] All digital pins may not exceed V_{CC} as the internal ESD circuit can be damaged. To prevent this it is recommended that control pins are limited to a maximum of 5 mA.

10. Thermal characteristics

Table 10. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|-----------------|---|---------------------------------|-----|------|
| $R_{th(j-bop)}$ | thermal resistance from junction to bottom of package | in free air [1] | 14 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air [2] | 35 | K/W |

[1] Simulated using final element method model resembling the device mounted on the application board. See [Section 13](#).

[2] Device mounted on application board.

11. Static characteristics

Table 11. Characteristics

Typical values at $V_{CC} = 5\text{ V}$; current setting = 3; $T_{amb} = 25\text{ °C}$; $Z_i = 200\ \Omega$; $Z_o = 75\ \Omega$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|------------------------------------|-----|-------|----------------|------|
| I_{CC} | supply current | transmit-enable mode; TX_EN = HIGH | - | 325 | - | mA |
| | | transmit-disable mode; TX_EN = LOW | - | 6.0 | - | mA |
| V_{IH} | HIGH-level input voltage | [1] | 2.0 | - | $V_{CC} + 0.6$ | V |
| V_{IL} | LOW-level input voltage | [1] | 0 | - | 0.8 | V |
| P | power dissipation | | - | 1.625 | | W |

[1] Voltage on the control pins.

12. Dynamic characteristics

Table 12. Characteristics

Typical values at $V_{CC} = 5\text{ V}$; current setting = 3; $Z_i = 200\ \Omega$; $Z_o = 75\ \Omega$; $T_{amb} = 25\ ^\circ\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|--|--|-----|-----------|-----|---------------|
| G_v | voltage gain | gain code = 111111 [1][2] | - | 34 | - | dB |
| | | gain code = 000000 [1][2] | - | -24 | - | dB |
| G_{flat} | gain flatness | $f = 5\text{ MHz to }42\text{ MHz}$ [2] | - | ± 0.4 | - | dB |
| | | $f = 5\text{ MHz to }85\text{ MHz}$ [2] | - | ± 0.6 | - | dB |
| G_{step} | gain step | [2] | - | 1.0 | - | dB |
| $E_{G(dif)}$ | differential gain error | [2] | - | ± 0.2 | - | dB |
| $R_{i(dif)}$ | differential input resistance | | - | 200 | - | Ω |
| $R_{o(dif)}$ | differential output resistance | | - | 75 | - | Ω |
| f_{range} | frequency range | | 5 | - | 85 | MHz |
| P_n | noise power | transmit-disable mode; TX_EN = LOW; any bandwidth = 160 kHz from $f = 5\text{ MHz to }85\text{ MHz}$ | - | -69 | - | dBmV |
| α_{isol} | isolation | transmit-disable mode; TX_EN = LOW; $f = 85\text{ MHz}$ | - | -90 | - | dB |
| NF | noise figure | transmit mode; gain code = 111111 | - | 3.5 | - | dB |
| | | transmit mode; gain code = 101110 | - | 6.5 | - | dB |
| $t_{sw(G)}$ | gain switch time | transmit-disable/transmit-enable transient duration | - | 1.8 | - | μs |
| V_{os} | overshoot voltage | transmit-disable/transmit-enable transient step size | | | | |
| | | 55 dBmV output power | - | 80 | - | mV(p-p) |
| | | 49 dBmV output power | - | 50 | - | mV(p-p) |
| | | 43 dBmV output power | - | 25 | - | mV(p-p) |
| | | 37 dBmV output power | - | 5 | - | mV(p-p) |
| $\leq 31\text{ dBmV output power}$ | - | 5 | - | mV(p-p) | | |
| α_{2H} | second harmonic level | $P_i = 30\text{ dBmV}$; $P_L = 64\text{ dBmV}$ into 75 Ω differential impedance | - | -80 | - | dBc |
| α_{3H} | third harmonic level | $P_i = 30\text{ dBmV}$; $P_L = 64\text{ dBmV}$ into 75 Ω differential impedance | - | -67 | - | dBc |
| IMD3 | third-order intermodulation distortion | $P_i = 27\text{ dBmV}$ per tone; $P_L = 61\text{ dBmV}$ per tone into 75 Ω differential impedance | - | -70 | - | dBc |
| $P_{L(1dB)}$ | output power at 1 dB gain compression | CW signal | - | 74 | - | dBmV |

[1] Voltage gain does not include loss due to input and output transformers.

[2] $P_i = 30\text{ dBmV}$.

Table 13. ACLR characteristics

Typical values at $V_{CC} = 5\text{ V}$; current setting = 3; $T_{amb} = 25\text{ °C}$; $Z_i = 200\ \Omega$; $Z_o = 75\ \Omega$; channel bandwidth = 1280 kHz; integration bandwidth = 1280 kHz; $f = 5\text{ MHz to }85\text{ MHz}$, unless otherwise specified.

| Symbol | Parameter | Conditions | DOCSIS 3.0 spec. | Min | Typ | Max | Unit |
|----------------------------------|--------------------------------|---|------------------|-----|-----|-----|------|
| DOCSIS 3.0; 64-QAM | | | | | | | |
| ACLR | adjacent channel leakage ratio | $P_i = 29\text{ dBmV}$; $P_L = 57\text{ dBmV}$ | | | | | |
| | | 1 input channel | -50 | - | -68 | - | dBc |
| | | 2 input channels | -47 | - | -62 | - | dBc |
| | | 4 input channels | -44 | - | -58 | - | dBc |
| | | 8 input channels | - | - | -56 | - | dBc |
| DOCSIS 3.0; QPSK | | | | | | | |
| ACLR | adjacent channel leakage ratio | $P_i = 33\text{ dBmV}$; $P_L = 61\text{ dBmV}$ | | | | | |
| | | 1 input channel | -50 | - | -66 | - | dBc |
| | | 2 input channels | -47 | - | -58 | - | dBc |
| | | 4 input channels | -44 | - | -54 | - | dBc |
| | | 8 input channels | - | - | -52 | - | dBc |
| DOCSIS 3.0 + 3 dB; 64-QAM | | | | | | | |
| ACLR | adjacent channel leakage ratio | $P_i = 29\text{ dBmV}$; $P_L = 60\text{ dBmV}$ | | | | | |
| | | 1 input channel | -50 | - | -68 | - | dBc |
| | | 2 input channels | -47 | - | -62 | - | dBc |
| | | 4 input channels | -44 | - | -58 | - | dBc |
| | | 8 input channels | - | - | -56 | - | dBc |
| DOCSIS 3.0 + 3 dB; QPSK | | | | | | | |
| ACLR | adjacent channel leakage ratio | $P_i = 33\text{ dBmV}$; $P_L = 64\text{ dBmV}$ | | | | | |
| | | 1 input channel | -50 | - | -66 | - | dBc |
| | | 2 input channels | -47 | - | -58 | - | dBc |
| | | 4 input channels | -44 | - | -54 | - | dBc |
| | | 8 input channels | - | - | -48 | - | dBc |
| DOCSIS 3.0 + 4 dB; 64-QAM | | | | | | | |
| ACLR | adjacent channel leakage ratio | $P_i = 29\text{ dBmV}$; $P_L = 61\text{ dBmV}$ | | | | | |
| | | 1 input channel | -50 | - | -68 | - | dBc |
| | | 2 input channels | -47 | - | -62 | - | dBc |
| | | 4 input channels | -44 | - | -58 | - | dBc |
| | | 8 input channels | - | - | -56 | - | dBc |
| DOCSIS 3.0 + 4 dB; QPSK | | | | | | | |
| ACLR | adjacent channel leakage ratio | $P_i = 33\text{ dBmV}$; $P_L = 65\text{ dBmV}$ | | | | | |
| | | 1 input channel | -50 | - | -66 | - | dBc |
| | | 2 input channels | -47 | - | -58 | - | dBc |
| | | 4 input channels | -44 | - | -50 | - | dBc |
| | | 8 input channels | - | - | -42 | - | dBc |

13. Application information

13.1 External components

Matching the balanced output of the chip to a single-ended 75 Ω load is accomplished using a 1 : 1 ratio transformer. For measurements in a 50 Ω system R7 and R8 are added for impedance transformation from 75 Ω to 50 Ω. R7 and R8 are not required in the final application.

The transformer also cancels even mode distortion products and common mode signals, such as the voltage transients that occur while enabling and disabling the amplifiers. External capacitors are needed for the functionality of the circuit, the pins are internal nodes in the output amplifier.

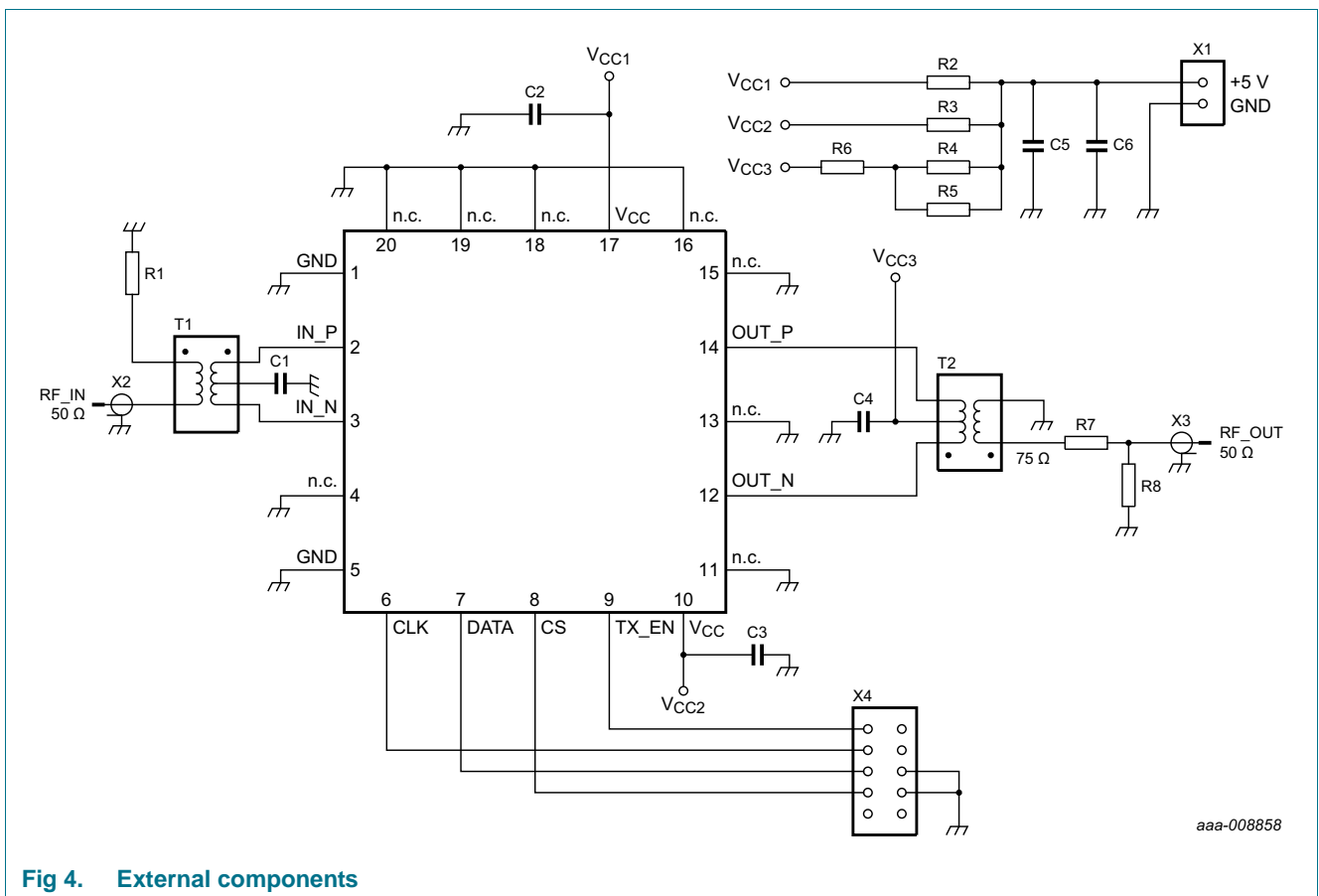


Fig 4. External components

Table 14. List of components

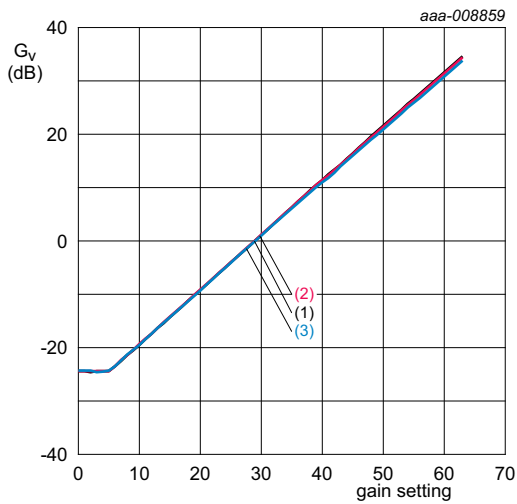
For application diagram, see [Figure 4](#).

| Component | Description | Value | Size | Supplier: Part No. |
|----------------|-------------|--------|----------|--------------------|
| C1, C2, C3, C4 | capacitor | 10 nF | SMD 0603 | |
| C5 | capacitor | 100 nF | SMD 0603 | |
| C6 | capacitor | 10 μF | SMD 1206 | |
| R1, R6 | resistor | 0 Ω | SMD 0603 | |
| R2, R3 | resistor | 0 Ω | SMD 0805 | |
| R4, R5 | resistor | 4.7 Ω | SMD 0603 | |

Table 14. List of components ...continued
 For application diagram, see [Figure 4](#).

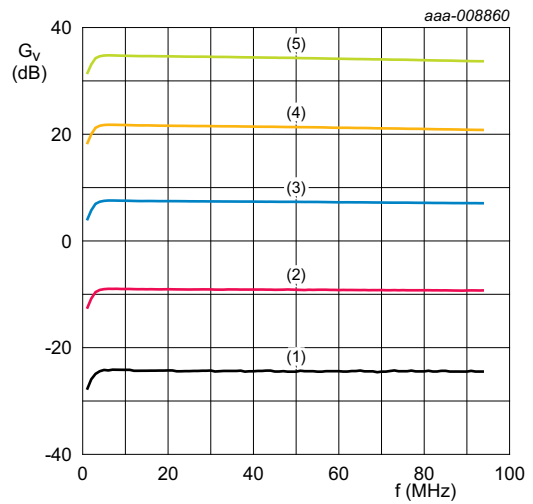
| Component | Description | Value | Size | Supplier: Part No. |
|-----------|---------------|--------|----------|-----------------------------|
| R7 | resistor | 43.3 Ω | SMD 0603 | |
| R8 | resistor | 86.6 Ω | SMD 0603 | |
| T1 | input balun | - | - | TOKO: #617DB-1714 |
| T2 | output balun | - | - | M/A-COM: MABA-009572-CF18A0 |
| X1 | 2-pin header | - | - | |
| X2, X3 | SMA connector | - | - | |
| X4 | 10-pin header | - | - | FCI: Minitek |

13.2 Graphs



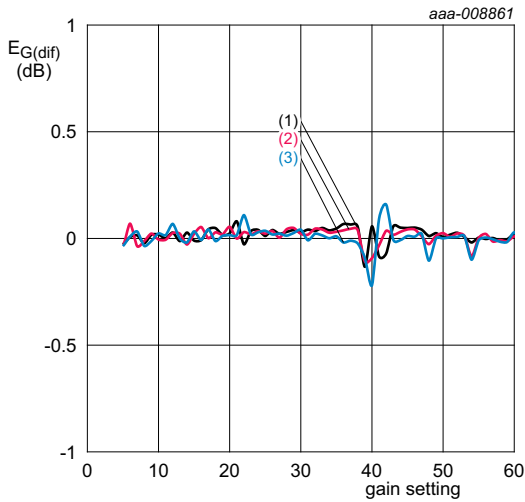
aaa-008859
 $V_{CC} = 5\text{ V}$; current setting = 3; $T_{amb} = 25\text{ °C}$;
 $P_i = 30\text{ dBmV}$.
 (1) $f = 5\text{ MHz}$
 (2) $f = 42\text{ MHz}$
 (3) $f = 85\text{ MHz}$

Fig 5. Voltage gain as a function of gain setting; typical values



aaa-008860
 $V_{CC} = 5\text{ V}$; current setting = 3; $T_{amb} = 25\text{ °C}$;
 $P_i = 30\text{ dBmV}$.
 (1) gain setting = 5
 (2) gain setting = 20
 (3) gain setting = 36
 (4) gain setting = 50
 (5) gain setting = 63

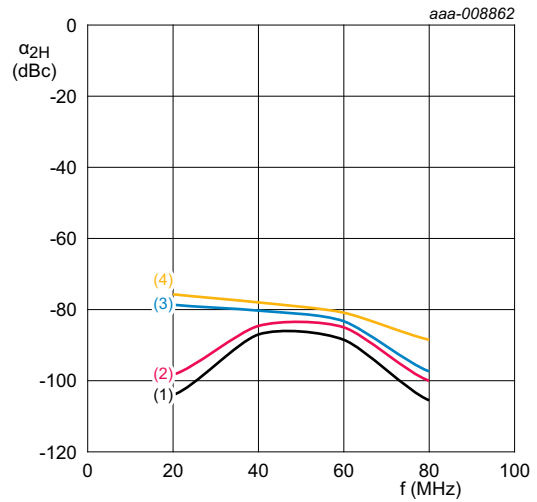
Fig 6. Voltage gain as a function of frequency; typical values



$V_{CC} = 5\text{ V}$; current setting = 3; $T_{amb} = 25\text{ }^{\circ}\text{C}$;
 $P_i = 30\text{ dBmV}$.

- (1) $f = 5\text{ MHz}$
- (2) $f = 42\text{ MHz}$
- (3) $f = 85\text{ MHz}$

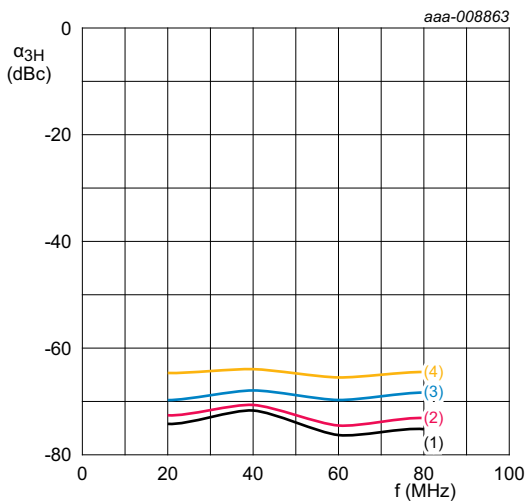
Fig 7. Differential gain error as a function of gain setting; typical values



$V_{CC} = 5\text{ V}$; $P_i = 30\text{ dBmV}$; $P_L = 64\text{ dBmV}$;
 current setting = 3; gain setting = 63.

- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = -10\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = +25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = +85\text{ }^{\circ}\text{C}$

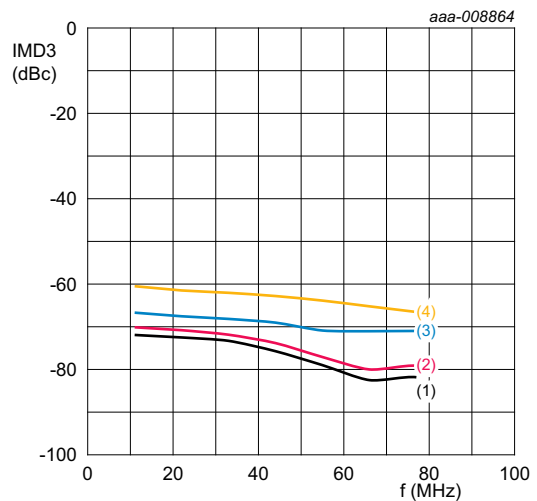
Fig 8. Second harmonic level as a function of frequency; typical values



$V_{CC} = 5\text{ V}$; $P_i = 30\text{ dBmV}$; $P_L = 64\text{ dBmV}$;
 current setting = 3; gain setting = 63.

- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = -10\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = +25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = +85\text{ }^{\circ}\text{C}$

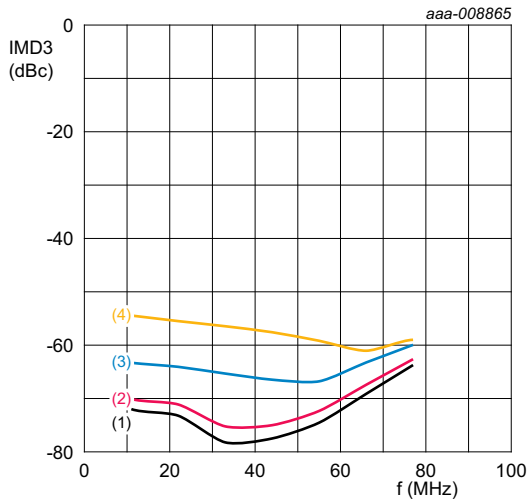
Fig 9. Third harmonic level as a function of frequency; typical values



$V_{CC} = 5\text{ V}$; $P_i = 27\text{ dBmV per tone}$; $P_L = 61\text{ dBmV per tone}$;
 current setting = 3; gain setting = 63.

- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = -10\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = +25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = +85\text{ }^{\circ}\text{C}$

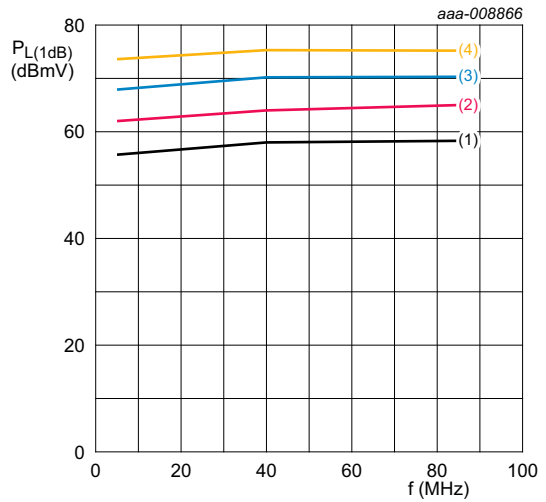
Fig 10. Third order intermodulation distortion as a function of frequency; typical values



$V_{CC} = 5\text{ V}$; $P_i = 30\text{ dBmV}$ per tone; $P_L = 64\text{ dBmV}$ per tone; current setting = 3; gain setting = 63.

- (1) $T_{amb} = -40\text{ }^\circ\text{C}$
- (2) $T_{amb} = -10\text{ }^\circ\text{C}$
- (3) $T_{amb} = +25\text{ }^\circ\text{C}$
- (4) $T_{amb} = +85\text{ }^\circ\text{C}$

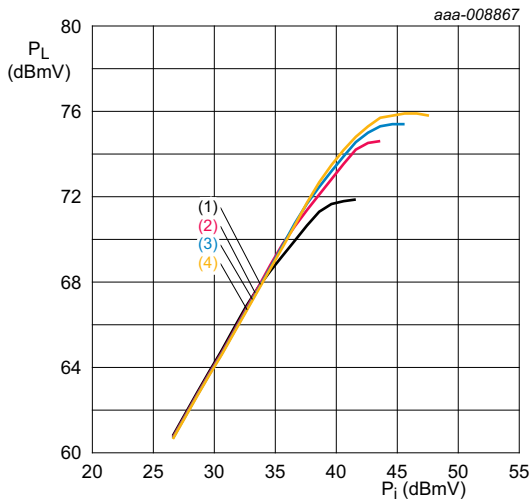
Fig 11. Third order intermodulation distortion as a function of frequency; typical values



$V_{CC} = 5\text{ V}$; current setting = 3; $T_{amb} = 25\text{ }^\circ\text{C}$; $P_i = 30\text{ dBmV}$.

- (1) gain setting = 39
- (2) gain setting = 48
- (3) gain setting = 54
- (4) gain setting = 63

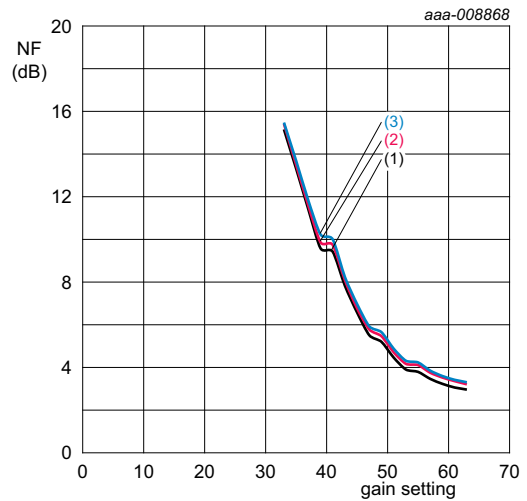
Fig 12. Output power at 1 dB gain compression as a function of frequency; typical values



$T_{amb} = 25\text{ }^\circ\text{C}$; $V_{CC} = 5\text{ V}$; $f = 85\text{ MHz}$; gain setting = 63.

- (1) current setting = 0
- (2) current setting = 1
- (3) current setting = 2
- (4) current setting = 3

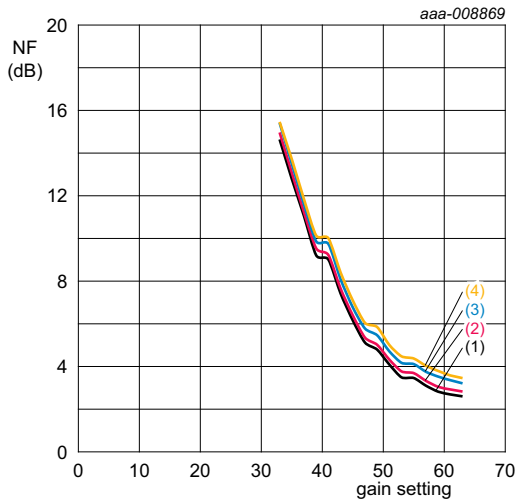
Fig 13. Output power as a function of input power; typical values



$T_{amb} = 25\text{ }^\circ\text{C}$; $V_{CC} = 5\text{ V}$; current setting = 3.

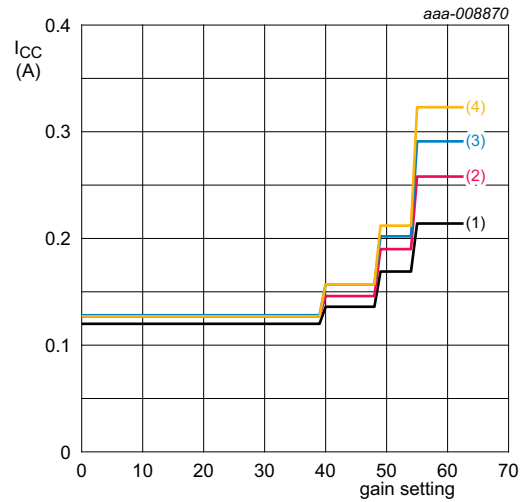
- (1) $f = 5\text{ MHz}$
- (2) $f = 42\text{ MHz}$
- (3) $f = 85\text{ MHz}$

Fig 14. Noise figure as a function of gain setting; typical values



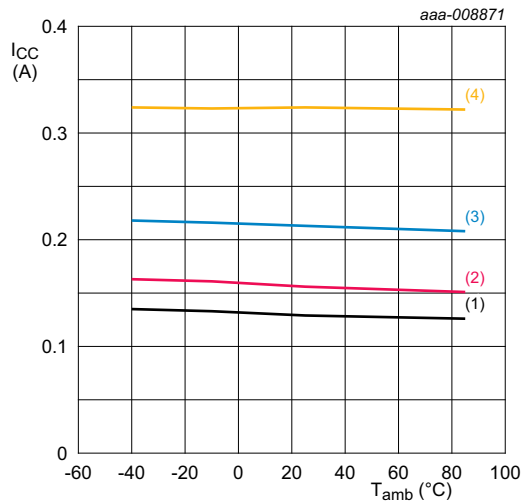
$f = 45 \text{ MHz}$; $V_{CC} = 5 \text{ V}$; current setting = 3.
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = -10 \text{ }^\circ\text{C}$
 (3) $T_{amb} = +25 \text{ }^\circ\text{C}$
 (4) $T_{amb} = +85 \text{ }^\circ\text{C}$

Fig 15. Noise figure as a function of gain setting; typical values



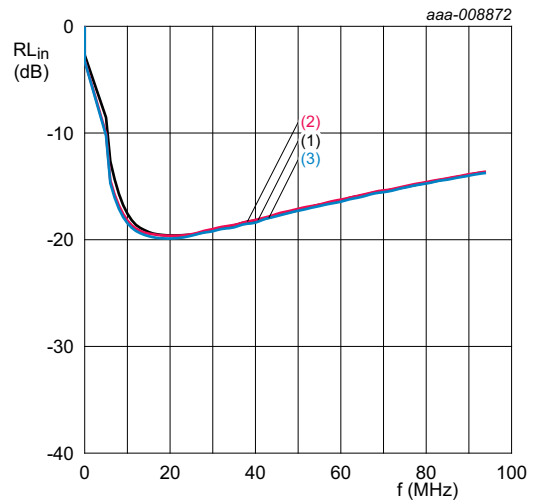
$T_{amb} = 25 \text{ }^\circ\text{C}$; $V_{CC} = 5 \text{ V}$.
 (1) current setting = 0
 (2) current setting = 1
 (3) current setting = 2
 (4) current setting = 3

Fig 16. Supply current as a function of gain setting; typical values



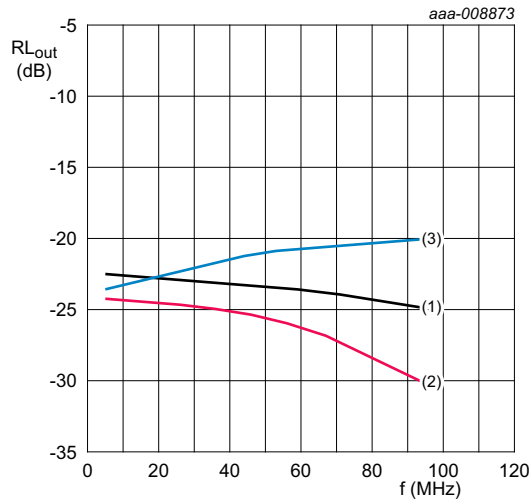
$V_{CC} = 5 \text{ V}$; current setting = 3.
 (1) gain setting = 20
 (2) gain setting = 44
 (3) gain setting = 52
 (4) gain setting = 60

Fig 17. Supply current as a function of ambient temperature; typical values



$T_{amb} = 25 \text{ }^\circ\text{C}$; $V_{CC} = 5 \text{ V}$; current setting = 3.
 (1) gain setting = 5
 (2) gain setting = 36
 (3) gain setting = 63

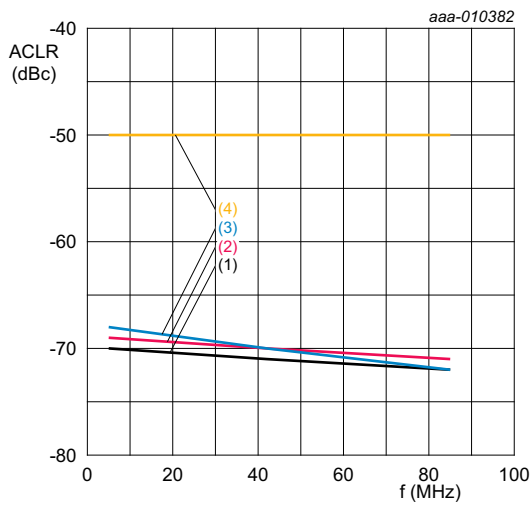
Fig 18. Input return loss as a function of frequency; typical values



T_{amb} = 25 °C; V_{CC} = 5 V; current setting = 3.

- (1) gain setting = 5
- (2) gain setting = 63
- (3) amplifier disabled (TX_EN LOW)

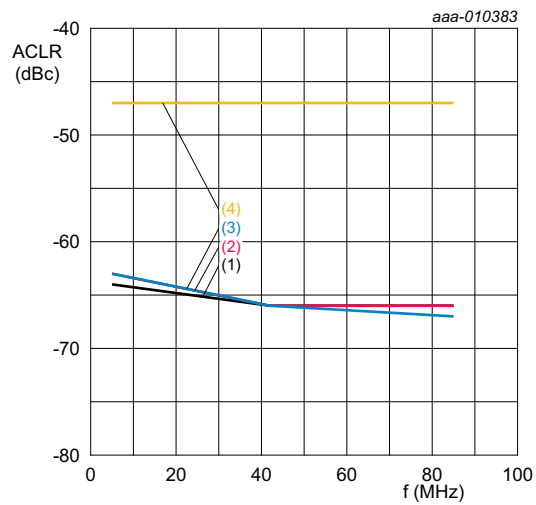
Fig 19. Output return loss as a function of frequency; typical values



One carrier 64-QAM; T_{amb} = 25 °C; V_{CC} = 5 V; max. current; P_i = 29 dBmV.

- (1) P_L = 57 dBmV
- (2) P_L = 60 dBmV
- (3) P_L = 61 dBmV
- (4) DOCSIS 3.0 specification

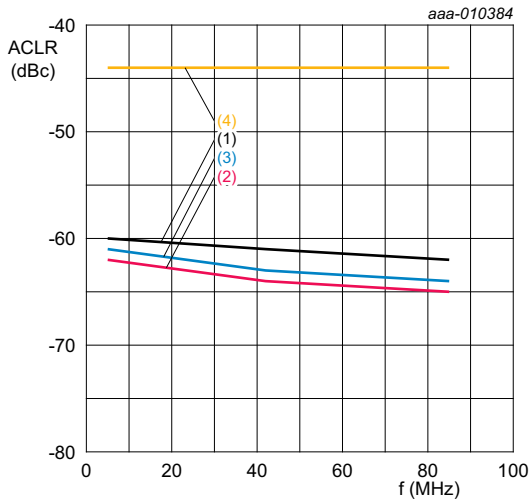
Fig 20. Adjacent channel leakage ratio as a function of frequency; typical values



Two carrier 64-QAM; T_{amb} = 25 °C; V_{CC} = 5 V; max. current; P_i = 29 dBmV.

- (1) P_L = 57 dBmV
- (2) P_L = 60 dBmV
- (3) P_L = 61 dBmV
- (4) DOCSIS 3.0 specification

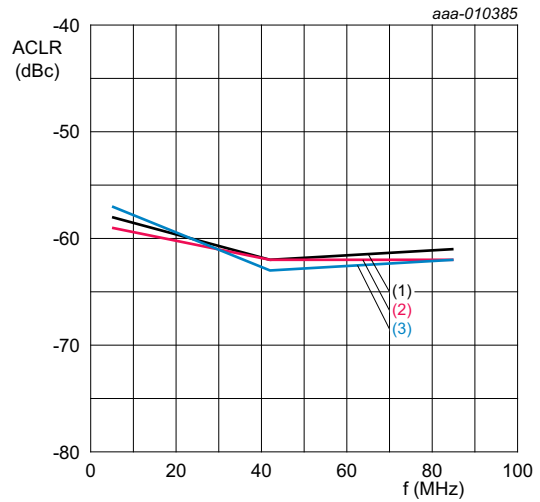
Fig 21. Adjacent channel leakage ratio as a function of frequency; typical values



Four carrier 64-QAM; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$; max. current; $P_i = 29\text{ dBmV}$.

- (1) $P_L = 57\text{ dBmV}$
- (2) $P_L = 60\text{ dBmV}$
- (3) $P_L = 61\text{ dBmV}$
- (4) DOCSIS 3.0 specification

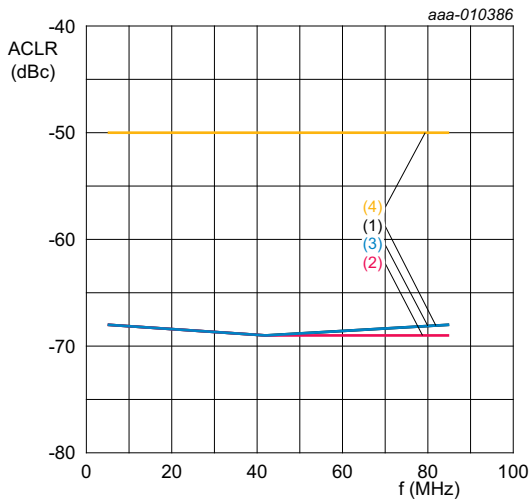
Fig 22. Adjacent channel leakage ratio as a function of frequency; typical values



Eight carrier 64-QAM; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$; max. current; $P_i = 29\text{ dBmV}$.

- (1) $P_L = 57\text{ dBmV}$
- (2) $P_L = 60\text{ dBmV}$
- (3) $P_L = 61\text{ dBmV}$

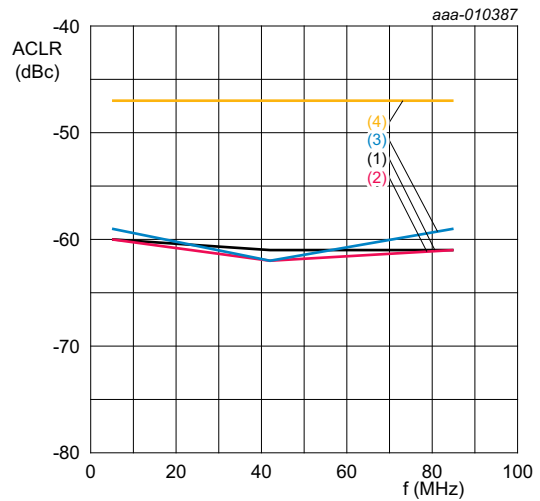
Fig 23. Adjacent channel leakage ratio as a function of frequency; typical values



One carrier QPSK; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$; max. current; $P_i = 33\text{ dBmV}$.

- (1) $P_L = 61\text{ dBmV}$
- (2) $P_L = 64\text{ dBmV}$
- (3) $P_L = 65\text{ dBmV}$
- (4) DOCSIS 3.0 specification

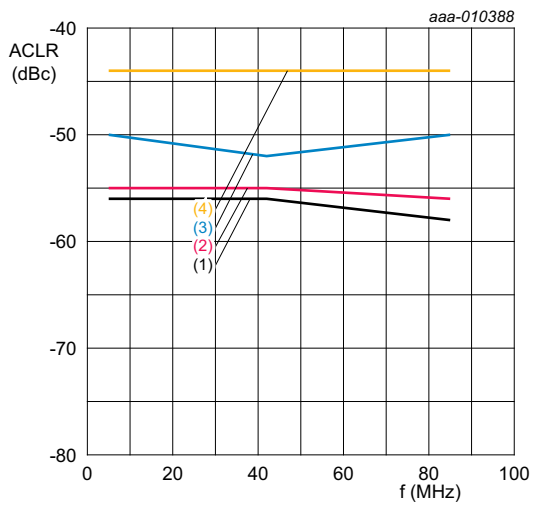
Fig 24. Adjacent channel leakage ratio as a function of frequency; typical values



Two carrier QPSK; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$; max. current; $P_i = 33\text{ dBmV}$.

- (1) $P_L = 61\text{ dBmV}$
- (2) $P_L = 64\text{ dBmV}$
- (3) $P_L = 65\text{ dBmV}$
- (4) DOCSIS 3.0 specification

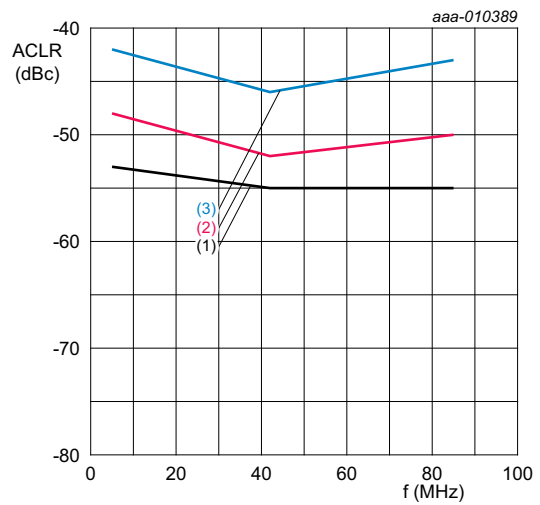
Fig 25. Adjacent channel leakage ratio as a function of frequency; typical values



Four carrier QPSK; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$;
max. current; $P_i = 33\text{ dBmV}$.

- (1) $P_L = 61\text{ dBmV}$
- (2) $P_L = 64\text{ dBmV}$
- (3) $P_L = 65\text{ dBmV}$
- (4) DOCSIS 3.0 specification

Fig 26. Adjacent channel leakage ratio as a function of frequency; typical values



Eight carrier QPSK; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$;
max. current; $P_i = 33\text{ dBmV}$.

- (1) $P_L = 61\text{ dBmV}$
- (2) $P_L = 64\text{ dBmV}$
- (3) $P_L = 65\text{ dBmV}$

Fig 27. Adjacent channel leakage ratio as a function of frequency; typical values

14. Package outline

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads;
20 terminals; body 5 x 5 x 0.85 mm

SOT662-1

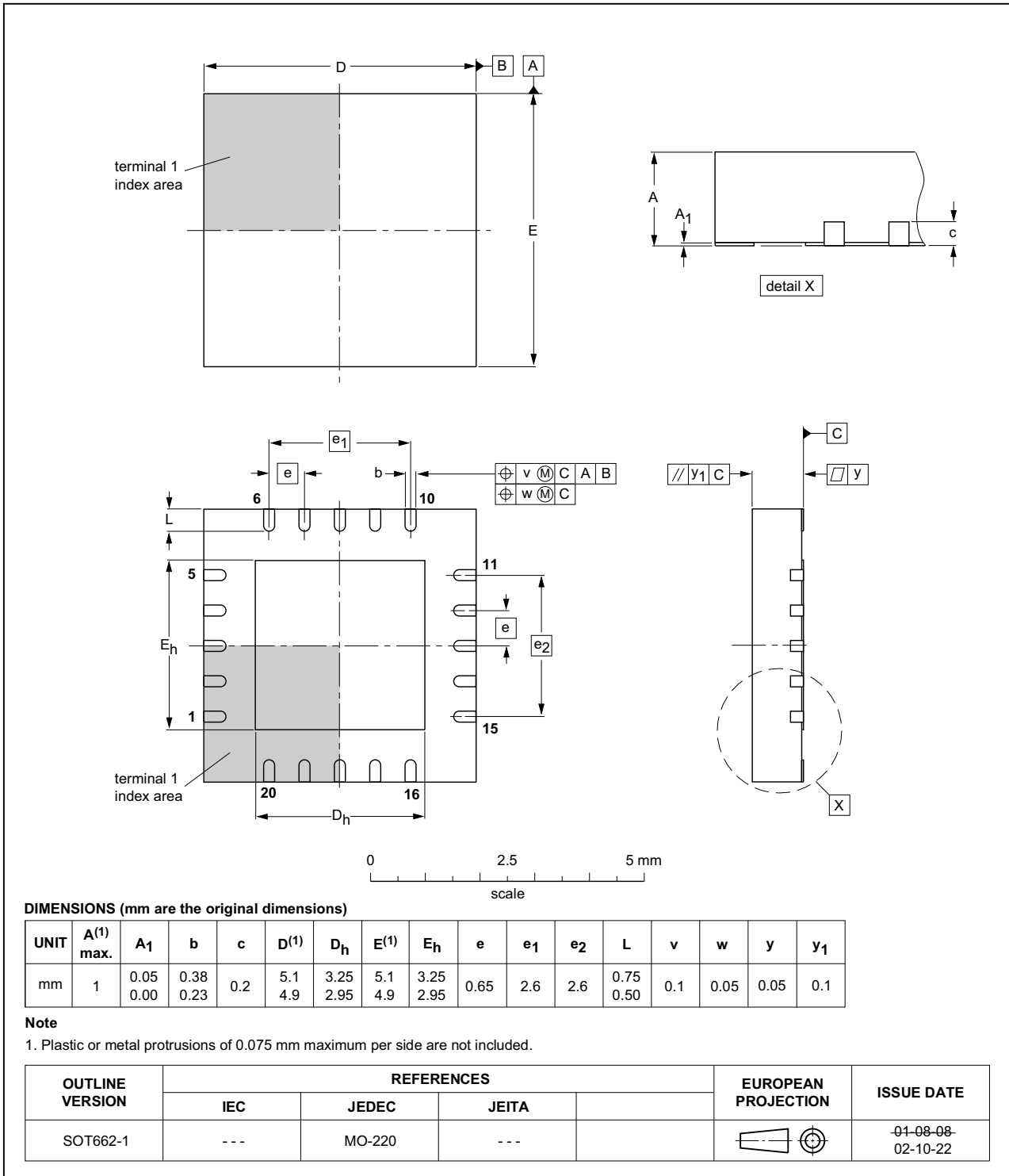


Fig 28. Package outline SOT662-1 (HVQFN20)

15. Handling information

15.1 Moisture sensitivity

Table 15. Moisture sensitivity level

| Test methodology | Class |
|------------------|-------|
| JESD-22-A113 | 1 |

16. Abbreviations

Table 16. Abbreviations

| Acronym | Description |
|---------|--|
| CATV | Community Antenna TeleVision |
| CW | Continuous Wave |
| ESD | ElectroStatic Discharge |
| HVQFN | Heatsink Very thin Quad Flat pack No leads |
| QAM | Quadrature Amplitude Modulation |
| QPSK | Quadrature Phase-Shift Keying |
| SMA | SubMiniature version A |
| SMD | Surface-Mounted Device |
| Tx | Transmission |
| VoIP | Voice over Internet Protocol |

17. Revision history

Table 17. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|--|--------------------|---------------|-------------|
| BGA3031 v.3 | 20141120 | Product data sheet | - | BGA3031 v.2 |
| Modifications | <ul style="list-style-type: none"> • T_{case} replaced by T_{amb} in whole document • Table 9 on page 7: added extra line: T_{amb}, ambient temperature, -40 °C min., $+85\text{ °C max.}$ • Figure 8 on page 13: figure updated • Figure 9 on page 13: figure updated • Figure 10 on page 13: figure updated • Figure 11 on page 14: figure updated • Figure 15 on page 15: figure updated • Figure 17 on page 15: figure updated | | | |
| BGA3031 v.2 | 20140226 | Product data sheet | - | BGA3031 v.1 |
| BGA3031 v.1 | 20130815 | Product data sheet | - | - |

18. Legal information

18.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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