

## Serial-in / Parallel-out Driver Series

# Serial / Parallel 5-input Driver


**BA829**

No.09051EAT02

**●Description**

Serial-in-parallel-out driver is a constant-current output driver with a built-in shift register and a latch circuit to turn on a maximum of 8 LED by a 5-line interface linked to a microcontroller. Output current value of constant-current can be set up to a maximum of 300mA.

**●Features**

- 1) This product can drive a maximum of 300mA.
- 2) When the strobe terminal is controlled by the drive timing pulse, current during a period without driving can be reduced.
- 3) When the data output terminal is used as the next input data, cascade connection becomes possible.
- 4) Digital ground and power ground are separated.
- 5) Latch is built in between the shift register and the driver output.
- 6) Stand-by function is incorporated. (10 $\mu$ A Typ. upon standby)

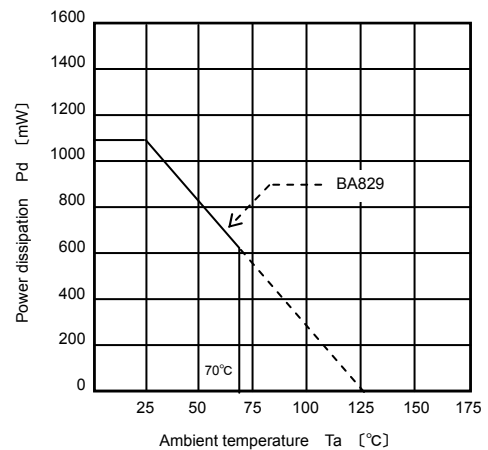
**●Applications**

For AV equipment such as, component stereo sets, videos and TV sets, PCs, and control microcontroller mounted equipment.

**●Absolute maximum ratings**

| Parameter             | Symbol            | Limit                   | Unit |
|-----------------------|-------------------|-------------------------|------|
| Power supply voltage  | V <sub>DD</sub>   | -0.3 to +7.0            | V    |
| Power dissipation     | P <sub>d</sub>    | 1100*                   | mW   |
| Input voltage         | I <sub>SINK</sub> | -0.3 to V <sub>CC</sub> | V    |
| Output voltage        | V <sub>O</sub>    | 15                      | V    |
| Operating temperature | T <sub>opr</sub>  | -25 to +70              | °C   |
| Storage temperature   | T <sub>stg</sub>  | -55 to +125             | °C   |

\*1 Reduced by 11 mW/°C over 25°C.

**●Thermal derating curve**


● Recommended operating conditions (Topr=-25°C to +70°C)

| Parameter                       | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---------------------------------|--------|------|------|------|------|-----------|
| Power supply                    | VCC    | 4.5  | 5.0  | 5.5  | V    | -         |
| Clock frequency                 | TCLK   | -    | -    | 500  | kHz  | -         |
| Power setup time                | tPset  | 500  | -    | -    | ns   | Fig.4     |
| Clock pulse width               | tWC    | 1    | -    | -    | ns   | Fig.4     |
| Data setup time                 | tDset  | 300  | -    | -    | ns   | Fig.4     |
| Data hold time                  | tDhold | 400  | -    | -    | ns   | Fig.4     |
| Latch pulse timing 1            | tLT1   | 600  | -    | -    | ns   | Fig.4     |
| Latch pulse timing 2            | tLT2   | 250  | -    | -    | ns   | Fig.4     |
| Latch pulse width               | tWL    | 800  | -    | -    | ns   | Fig.4     |
| Strobe pulse timing 1           | tST1   | 300  | -    | -    | ns   | Fig.4     |
| Strobe pulse width              | tws    | 3    | -    | -    | μs   | Fig.4     |
| Voltage between L-GND and P-GND | VG     | -    | -    | 0.2  | V    | -         |

\* Electric potential is a difference of L-GND and P-GND. Short-circuit near the power source whenever possible.  
However, between L-GND Pin and P-GND Pin, product should be used in a range not exceeding 0.2V.

● Electrical characteristics (Unless otherwise specified, Ta=25°C, Vcc=5.0V)

| Parameter                       | Symbol | Min. | Typ.  | Max. | Unit | Condition                      | Test Circuit |
|---------------------------------|--------|------|-------|------|------|--------------------------------|--------------|
| Supply current 1                | Icc1   | —    | 10    | 20   | μA   | PSW“L”                         | Fig.1        |
| Supply current 2                | Icc2   | —    | 110   | 158  | mA   | PSW“H”, STB“H”                 | Fig.1        |
| Supply current 3                | Icc3   | —    | 14    | 20   | mA   | PSW“H”, STB“L”                 | Fig.1        |
| Output ON voltage               | VOON   | —    | 0.4   | 0.6  | V    | IccN=300 mA                    | Fig.1        |
| Output leakage current          | IOOFF  | —    | 10    | 50   | μA   | V0=13.5V                       | Fig.1        |
| Data transference time          | fCLK   | 500  | —     | —    | kHz  | —                              | Fig.1        |
| Input high-level voltage        | VIH    | 2.6  | —     | —    | V    | —                              | Fig.2        |
| Input low-level voltage         | VIL    | —    | —     | 0.8  | V    | —                              | Fig.2        |
| Input high-level current        | IiH1   | —    | 0.1   | 10   | μA   | V1=3.4V,CLK,LATCH<br>,DATA,STB | Fig.1        |
| Input low-level current         | IiL1   | —    | -0.01 | -0.1 | mA   | V1=0.4V,CLK,LATCH<br>,DATA,STB | Fig.1        |
| Output high-level voltage       | VDDH   | 2.8  | 3.0   | —    | V    | IDOH=-400μA                    | Fig.1        |
| Output low-level voltage        | VDDL   | —    | 0.3   | 0.4  | V    | IDOL=∠1.6mA                    | Fig.1        |
| Data output transmission delay  | tDLH   | —    | 0.6   | 1.0  | μs   | RLD=10kΩ                       | Fig.4        |
| Data output transmission delay  | tDHL   | —    | 0.6   | 2.0  | μs   | RLD=10kΩ                       | Fig.4        |
| Print output transmission delay | tOLH   | —    | —     | 10   | μs   | RL=560kΩ560,<br>V0=13.5V       | Fig.4        |
| Print output transmission delay | tOHL   | —    | —     | 10   | μs   | RL=560kΩ560,<br>V0=13.5V       | Fig.4        |
| Input high-level current        | IiH2   | —    | 0.04  | 0.1  | mA   | V1=3.4V,PSW                    | Fig.1        |
| Input low-level current         | IiL2   | —    | 0.1   | 10   | μA   | V1=0.4V,PSW                    | Fig.1        |

●Block diagram

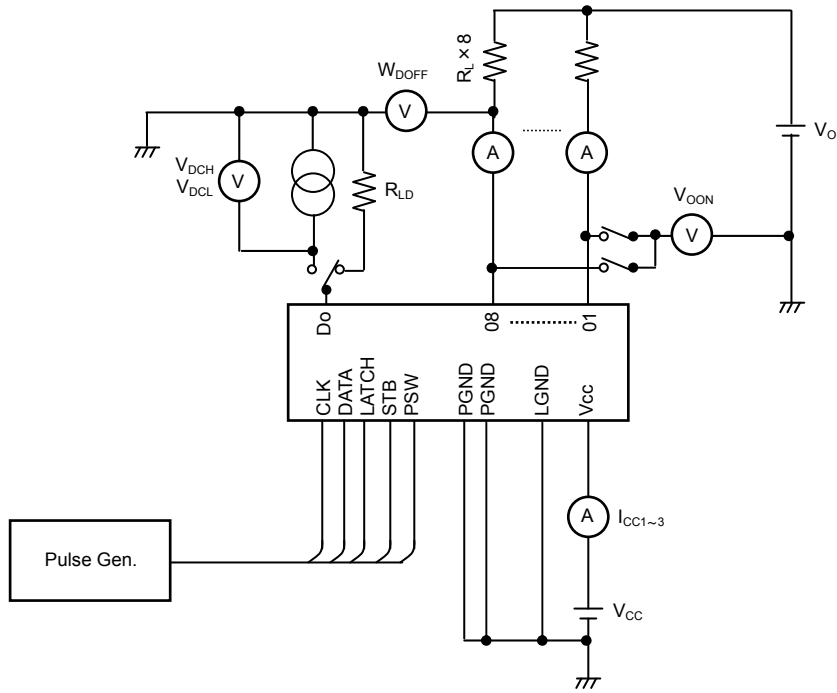


Fig.1

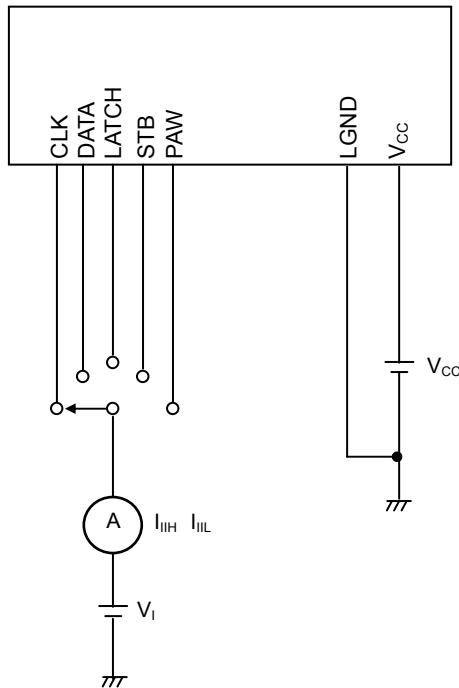


Fig.2

### ●Block diagram

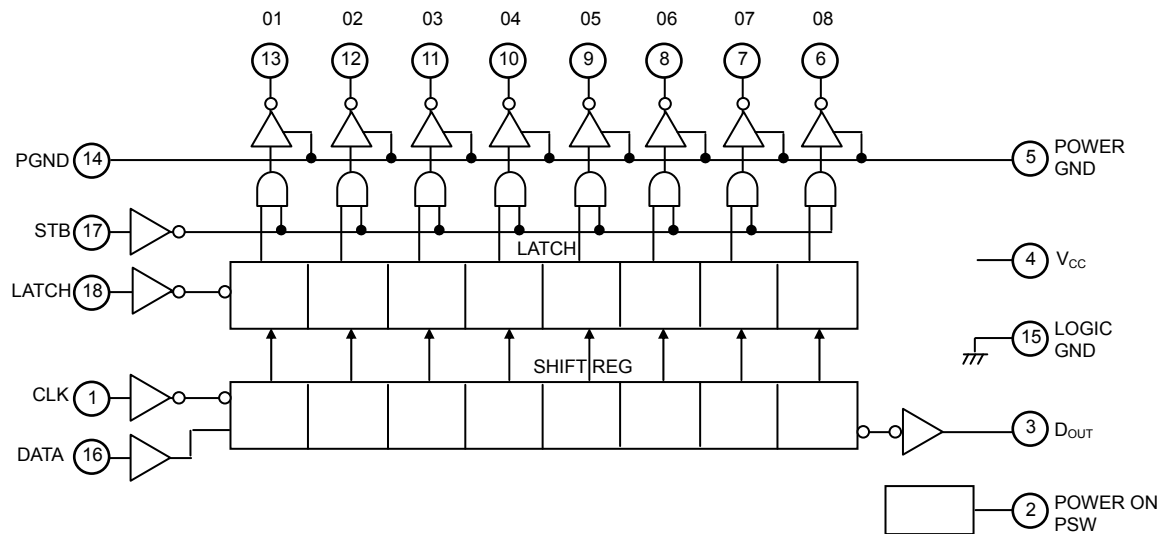


Fig.3

### ●Pin descriptions

| PIN No. | Terminal | I/O | Function                 |
|---------|----------|-----|--------------------------|
| 1       | CLK      | I   | Clock input              |
| 2       | PSW      | I   | Power switch             |
| 3       | DOUT     | O   | Cascade output           |
| 4       | VCC      | -   | Power supply             |
| 5       | PGND     | -   | GND                      |
| 6       | O8       | O   | Parallel data output     |
| 7       | O7       | O   |                          |
| 8       | O6       | O   |                          |
| 9       | O5       | O   |                          |
| 10      | O4       | O   |                          |
| 11      | O3       | O   |                          |
| 12      | O2       | O   |                          |
| 13      | O1       | O   |                          |
| 14      | PGND     | -   | GND                      |
| 15      | LGND     | -   | GND                      |
| 16      | DATA     | I   | Serial data input        |
| 17      | STB      | I   | Strobe input, "L" active |
| 18      | LATCH    | I   | Latch input              |

### ●Description of operation

BA829 is configured internally as shown in the logic circuit diagram. Terminals of clock (CLK), data (DATA), latch (LATCH), strobe (STB), and power switch (PSW) are available as input.

Data input is synchronized with the clock, read serially during the rise time and latched at the rise time edge of the shifted shift register. Latched data appears on the output terminal of O1-O8 by the strobe input. Pulse width is the same as that of the strobe input. Data output terminal DOUT, is a terminal used for cascade connection of the IC, where the output of the final stage of the shift register has appeared, and is connected to the next data input terminal DATA. In this case, when the clock and the strobe are used in conjunction, output terminal can be increased by 8 bits at a time.

To affect the standby mode, set the power switch to "L".

●Timing chart

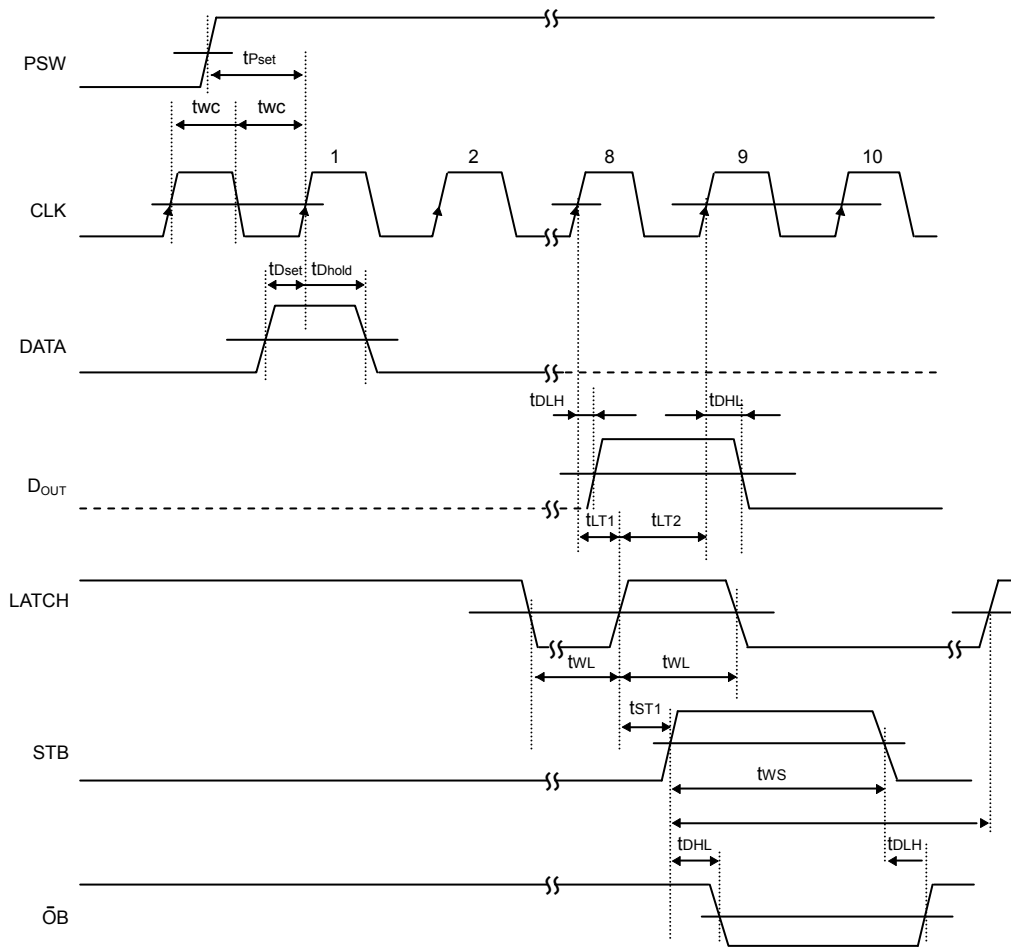
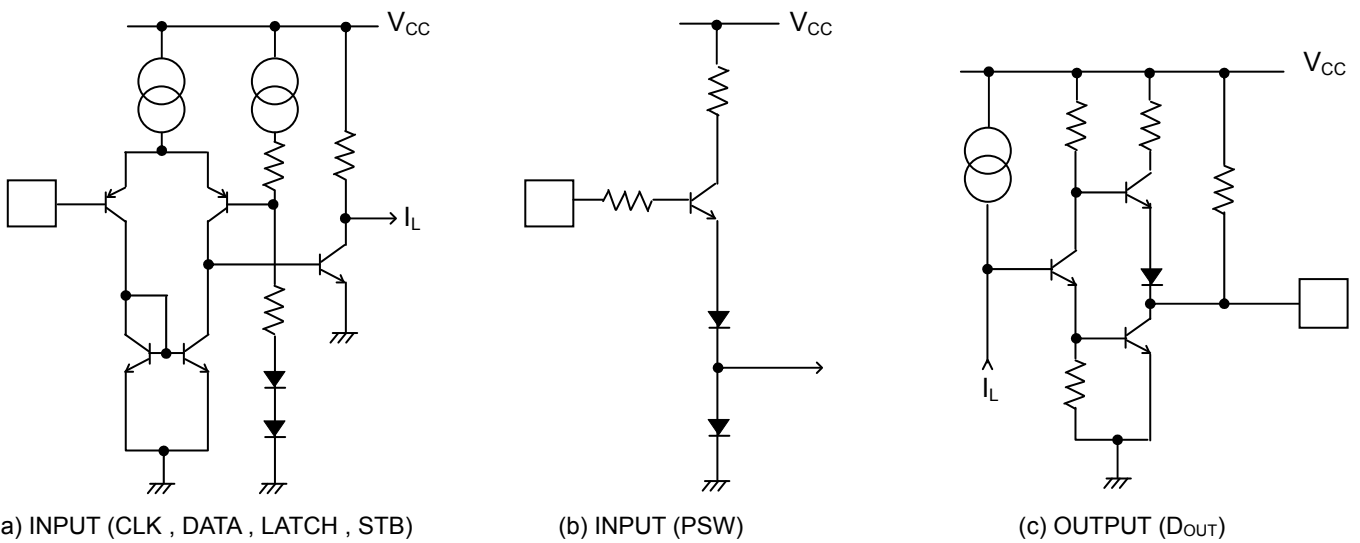


Fig.4

●Interfaces



## ● Operation Notes

### 1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

### 2. Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

### 3. Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.

### 4. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

### 5. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

### 6. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

### 7. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

### 8. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

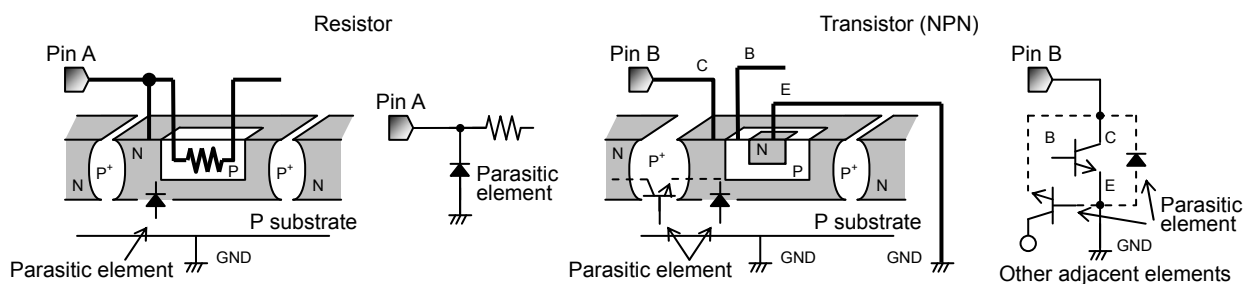


Fig.5 Example of IC structure

### 9. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Ordering part number

|   |   |
|---|---|
| B | D |
|---|---|

Part No.

|   |   |   |
|---|---|---|
| 8 | 2 | 9 |
|---|---|---|

Part No.

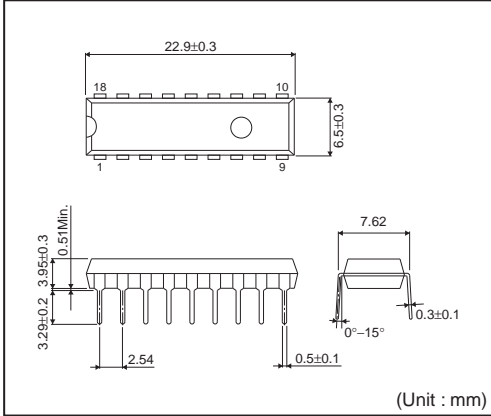
|  |
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Package  
None:DIP18

|  |  |
|--|--|
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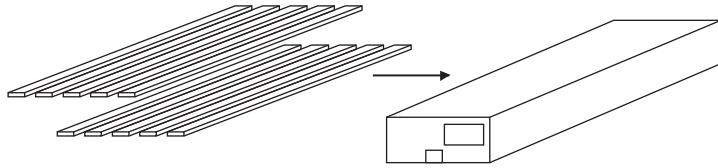
Packaging and forming specification  
None: Tube

DIP18



<Tape and Reel information>

|                   |  |
|-------------------|--|
| Container         | Tube   |
| Quantity          | 1000pcs  |
| Direction of feed | Direction of products is fixed in a container tube |



\*Order quantity needs to be multiple of the minimum quantity.

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