REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 17-08-22	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR-DIGITAL, 8-CHANNEL, I^2C, 12-BIT SAR ADC WITH TEMPERATURE SENSOR, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/17610**
	REV	**PAGE** 1 **OF** 11

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AMSC N/A

5962-V076-17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 8-Channel, I^2C, 12-Bit SAR ADC with Temperature Sensor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/17610	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7291 –EP	8-Channel, I^2C, 12-Bit SAR ADC with Temperature Sensor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-220-WGGD-11	Lead Frame Chip Scale Package (LFCSP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to GND1, GND	-0.3 V to +5 V
V_{DRIVE} to GND1, GND	-0.3 V to +5 V
Analog Input Voltage to GND1	−0.3 V to +3 V
Digital Input Voltage to GND1	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND1	−0.3 V to V_{DRIVE} + 0.3 V
V_{REF} to GND1	−0.3 V to +3 V
GND to GND1	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies 2/	±10 m A
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
Pb-free Tem perature, Soldering:	
Reflow	260(+0)°C
ESD	2 kV

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA}	θ_{JC}	Unit
Case X 3/	52	6.5	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51	–	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Transient currents of up to 100 mA do not cause latch-up.
3/ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 9 thermal vias. See JEDEC JESD51.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Test conditions 2/	Limits 3/			Unit
		Min	Typ	Max	
DYNAMIC PERFORMANCE (f_{IN} = 1 kHz sine wave)					
Signal-to-Noise Ratio (SNR)		70	71		dB
Signal-to-Noise + Distortion Ratio (SINAD)		70	71		dB
Total Harmonic Distortion (THD)			-84	-78	dB
Spurious-Free Dynamic Range (SFDR)			-85	-80	dB
Intermodulation Distortion (IMD)	f_A = 5.4 kHz, f_B = 4.6 kHz				
Second-Order Terms			-88		dB
Third-Order Terms			-88		dB
Channel-to-Channel Isolation	f_{IN} = 10 kHz		-100		dB
Full Power Bandwidth 4/					
	At 3 dB		30		MHz
	At 0.1 dB		10		MHz
DC ACCURACY					
Resolution		12			Bits
Integral Nonlinearity (INL)			±0.5	±1	LSB
Differential Nonlinearity (DNL)	Guaranteed no missing codes to 12 bit		±0.5	±0.99	LSB
Offset Error			±2	±4.5	LSB
Offset Error Matching			±2.5	±4.5	LSB
Offset Temperature Drift			4		ppm/°C
Gain Error			±1	±4	LSB
Gain Error Matching			±1	±2.5	LSB
Gain Temperature Drift			0.5		ppm/°C
ANALOG INPUT					
Input Voltage Ranges		0		V_{REF}	V
DC Leakage Current			±0.01	±1	µA
Input Capacitance 4/	When in track		34		pF
	When in hold		8		pF
REFERENCE INPUT/OUTPUT					
Reference Output Voltage 5/	±0.3% maximum at 25°C	2.4925	2.5	2.5075	V
Long-Term Stability	For 1000 hours		150		ppm
Output Voltage Hysteresis			50		ppm
Reference Input Voltage Range 6/		1		2.5	
DC Leakage Current	External reference applied to Pin V_{REF}		±0.01	±1	µA
VREF Output Impedance			1		
Reference Temperature Coefficient			12	35	ppm/°C
V_{REF} Noise 4/	Bandwidth = 10 MHz		60		µV/ms
LOGIC INPUTS (SDA, SCL)					
Input High Voltage V_{INH}		07 × V_{DRIVE}			V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} < 1.8 V_{DRIVE} ≥ 1.8	V_{DRIVE} − 0.3 V_{DRIVE} − 0.2			V
Output Low Voltage, V_{OL}	I_{SINK} = 3 mA I_{SINK} = 6 mA			0.4 0.6	V
Floating State Leakage Current			±0.01	±1	µA
Floating State Output Capacitance 4/			8		pF
INTERNAL TEMPERATURE SENSOR					
Operating Range		-55		+125	°C
Accuracy	T_A = −55°C to +85°C T_A = 85°C to 125°C		±1 ±1	±2 ±3	°C
Resolution	LSB size		0.25		°C
CONVERSION RATE					
Conversion Time			3.2		s
Autocycle Update Rate 7/			50		s
Throughput Rate	f_{SCL} = 400 kHz			22.22	kSPS
POWER REQUIREMENTS (Digital inputs = 0 V or V_{DRIVE})					
V_{DD}		2.8	3	3.6	V
V_{DRIVE}		1.65	3	3.6	V
I_{TOTAL} 8/ 9/					
Normal Mode (Operational)			2.9	3.5	mA
Norm al Mode (Static)			2,9	3.4	mA
Full Power-Down Mode	T_A = −55°C to +25°C		0.3	1.6	A
	T_A = >25°C to 85°C		1.6	4.5	A
	T_A = >85°C to 125°C		4,9	13	A
Power Dissipation 9/					
Normal Mode (Operational)	V_{DD} = 3 V, V_{DRIVE} = 3 V		8.7	10.5	mW
			10.4	12.6	mW
Norm al Mode (Static)			10.4	12.2	mW
Full Power-Down Mode	T_A = −55°C to +25°C		1.1	5.8	µW
	T_A = >25°C to 85°C		5.8	16.2	µW
	T_A = >85°C to 125°C		17.6	46.8	µW

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 2.8 V to 3.6 V; V_{DRIVE} = 1.65 V to 3.6 V; f_{SCL} = 400 kH z, fast SCLK mode; V_{REF} = 2.5 V internal/external; T_A = −55°C to +125°C, unless otherwise noted

3/ All specifications expressed in decibels are referred to full-scale range (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

4/ Sample tested during initial product release to ensure compliance.

5/ Refers to Pin V_{REF} specified for 25°C.

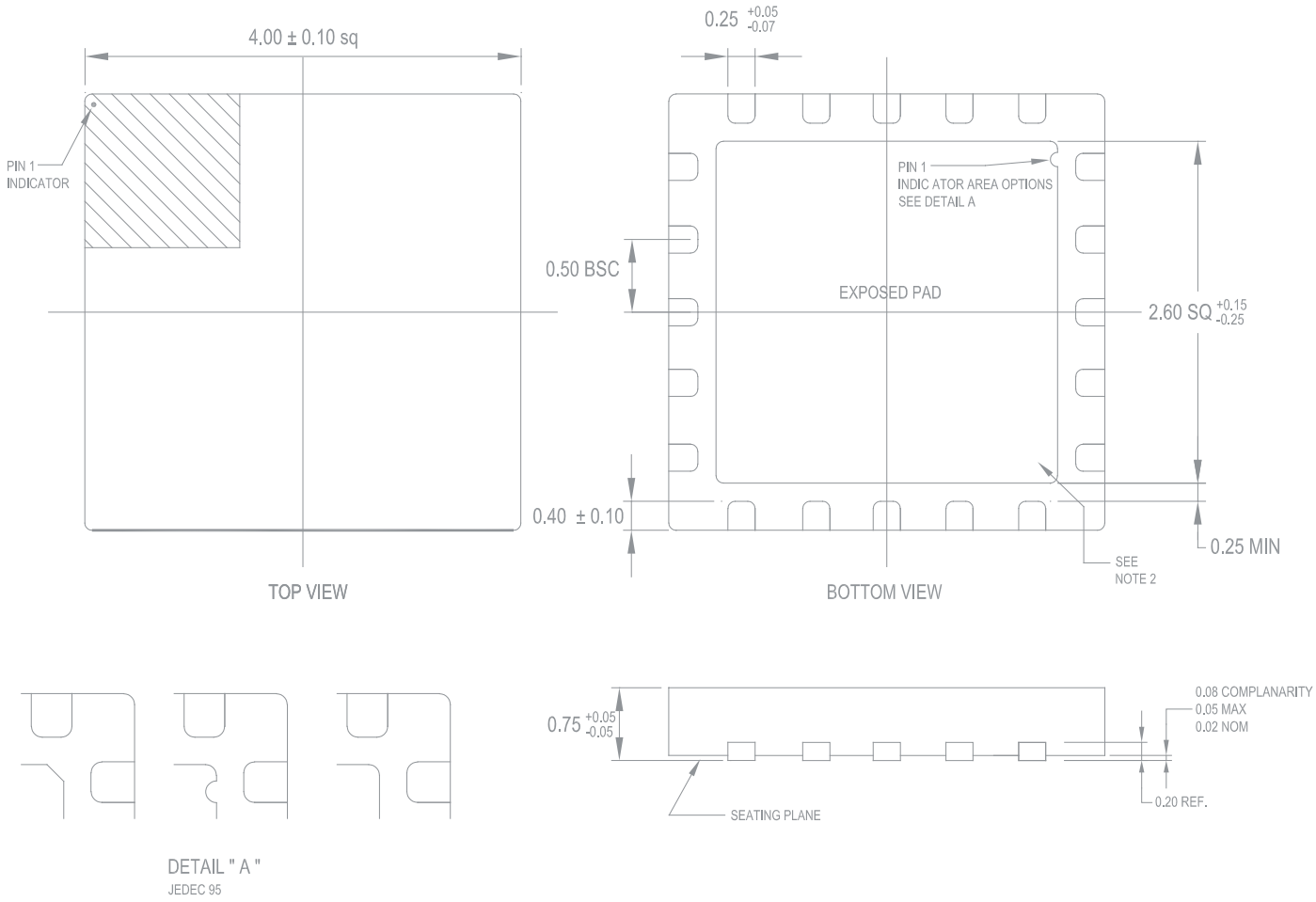
6/ A correction factor can be required on the temperature sensor results when using an external VREF (see manufacturer AD7291 data sheet).

7/ Sampled during initial product release to ensure compliance; not subject to production testing.

8/ I_{TOTAL} is the total current flowing in V_{DD} and V_{DRIVE}.

9/ I_{TOTA}L and power dissipation are specified with V_{DD} = V_{DRIVE} = 3.6 V, unless otherwise noted.

Case X



NOTES:

1. All linear dimensions are in millimeters.
2. For proper connection of the Exposed PAD, Refer to the Terminal Configuration and Terminal functions section of this data sheet.
3. Falls within JEDEC MO-220-VGGD-11.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{IN3}	20	V_{IN2}
2	V_{IN4}	19	V_{IN1}
3	V_{IN5}	18	V_{IN0}
4	V_{IN6}	17	$\overline{PD}/\overline{RST}$
5	V_{IN7}	16	V_{DRIVE}
6	GND1	15	SCL
7	V_{REF}	14	SDA
8	D_{CAP}	13	AS1
9	GND	12	ALERT
10	V_{DD}	11	AS0

NOTES:

1. The EXPOSED Metal paddle on the bottom of the LFCSP package should be soldered to the PCB Ground for proper Heat Dissipation and performance

FIGURE 2. Terminal connections.

Terminal number	Terminal symbol	DESCRIPTION
1, 2, 3, 4, 5, 18, 19, 20	V_{IN3}, V_{IN4}, V_{IN5}, V_{IN6}, V_{IN7}, V_{IN0}, V_{IN1}, V_{IN2}	Analog Inputs. The AD7291-EP has eight single-ended analog inputs that are multiplexed into the on-chip track and-hold amplifier. Each input channel can accept analog inputs from 0 V to 2.5 V. Any unused input channels must be connected to GND1 to avoid noise pickup.
6	GND1	Ground. Ground reference point for the internal reference circuitry on the AD7291-EP. All analog input signals and the external reference signals must be referred to this GND1 voltage. The GND1 pin must be connected to the ground plane of a system . All ground pins must ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. The VREF pin must be decoupled to this ground pin via a 10 F decoupling capacitor.
7	V_{REF}	Internal Reference/External Reference Supply. The nominal internal reference voltage of 2.5 V appears at this pin. Provided the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system . Decoupling capacitors must be connected to this pin to decouple the reference buffer. For best performance, it is recommended to use a 10 F decoupling capacitor on this pin to GND1. The internal reference can be disabled and an external reference supplied to this pin if required. The input voltage range for the external reference is 2.0 V to 2.5 V.
8	D_{CAP}	Decoupling Capacitor Pin. Decoupling capacitors (1 F recommended) are connected to this pin to decouple the internal low dropout regulator (LDO).
9	GND	Ground. Ground reference point for all analog and digital circuitry on the AD7291-EP. The GND pin must be connected to the ground plane of the system . All ground pins must ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. Both DCAP and VDD pins must be decoupled to this GND pin.
10	V_{DD}	Supply Voltage, 2.8 V to 3.6 V. This supply must be decoupled to GND with 10 F and 100 nF decoupling capacitors.
11, 13	AS0, AS1	Logic Inputs. Together, the logic state of these two inputs selects a unique I2C address for the AD7291-EP. See the manufacturer AD7291 data sheet for details. The device address depends on the voltage applied to these pins.
12	ALERT	Digital Output. This pin acts as an out-of-range indicator and, if enabled, becomes active when the conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ register values. See the manufacturer AD7291 data sheet for further details.
14	SDA	Digital Input/Output. Serial bus bidirectional data. This open-drain output requires a pull-up resistor. The output coding is straight binary for the voltage channels and twos complement for the temperature sensor result.

FIGURE 3. Terminal function.

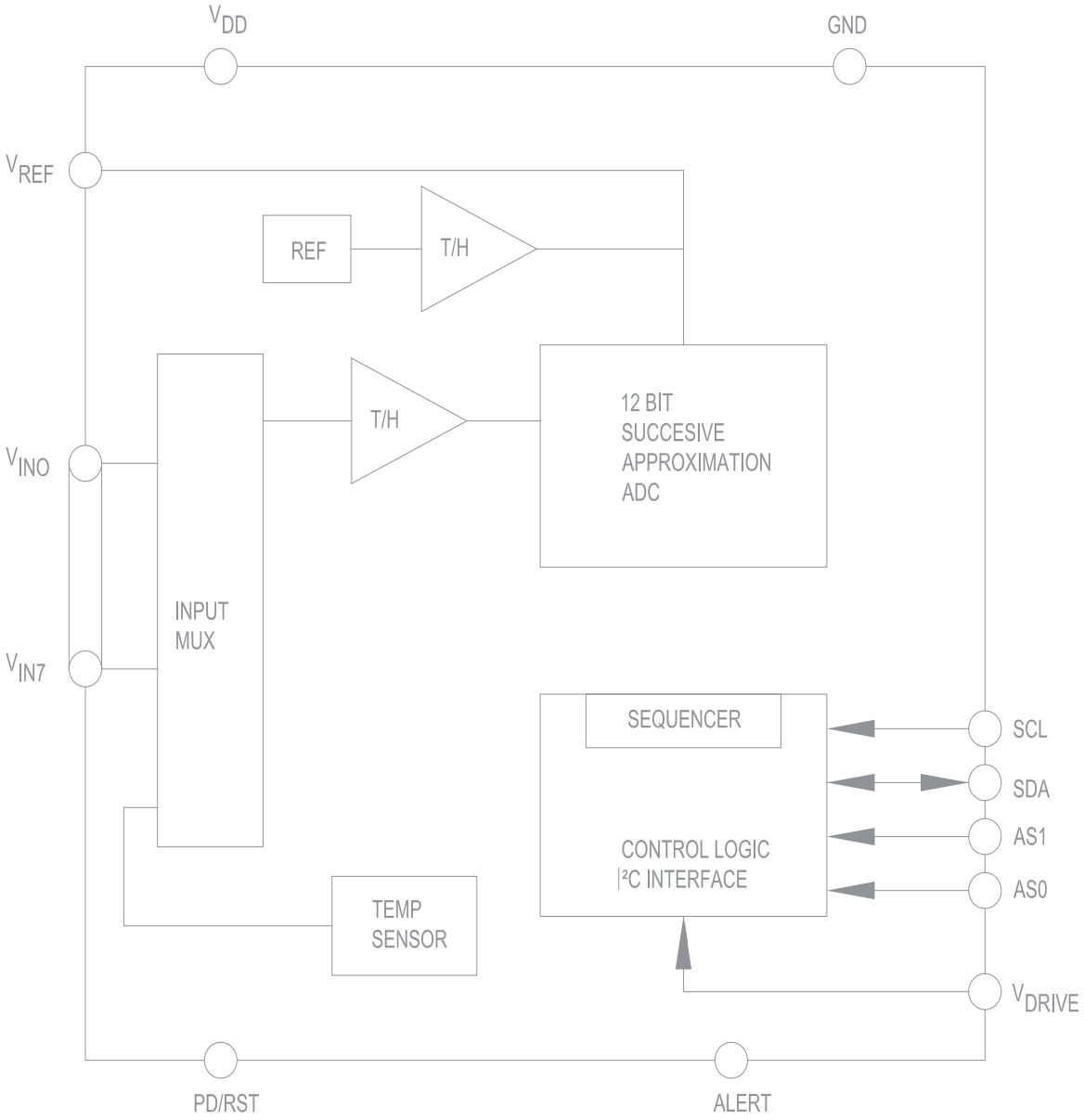


FIGURE 4. Functional block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Order Quantity	Vendor part number
V62/17610-01XE	24355	Tray units = 490	AD7291TCPZ-EP
		Reel units = 1500	AD7291TCPZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106