Features

- **EE Programmable 65,536 x 1-, 131,072 x 1-, and 262,144 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **In-System Programmable via 2-wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with Atmel AT6000, AT40K FPGAs, Altera FLEX® Devices, Lucent ORCA® FPGAs, Xilinx XC3000, XC4000, XC5200, SPARTAN® FPGAs, Motorola MPA1000 FPGAs**
- **Cascadable Read Back to Support Additional Configurations or Future Higher-density Arrays (128K and 256K only)**
- **Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available in the Space-efficient Plastic DIP or SOIC Packages; PLCC Package is Pin-compatible Across Product Family**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Available in 3.3V ± 10% LV and 5V ± 5% C Versions**
- **Low-power Standby Mode**

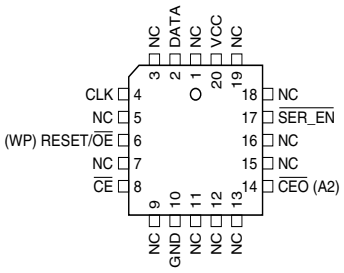
Description

The AT17C65/128/256 and AT17LV65/128/256 (low-density AT17 Series) FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The low-density AT17 Series is packaged in the 8-pin PDIP, 8-lead SOIC, and the popular 20-lead PLCC and SOIC. The AT17 Series family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17 Series organization supplies enough memory to configure one or multiple smaller FPGAs. Using a feature of the AT17 Series, the user can select the polarity of the reset function by programming a special EEPROM byte. These devices also support a write-protection mechanism within its programming mode.

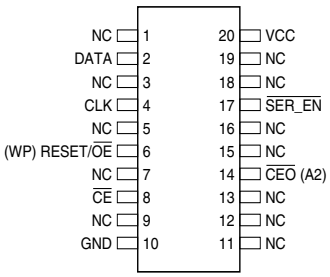
The AT17 Series Configurators can be programmed with industry-standard programmers, or Atmel's ATDH2200E Programming Kit.

Pin Configurations

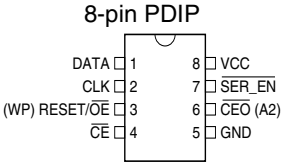
20-lead PLCC



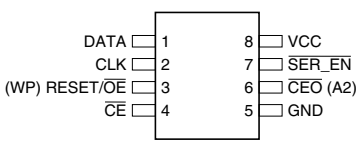
20-lead SOIC



8-pin PDIP



8-lead SOIC



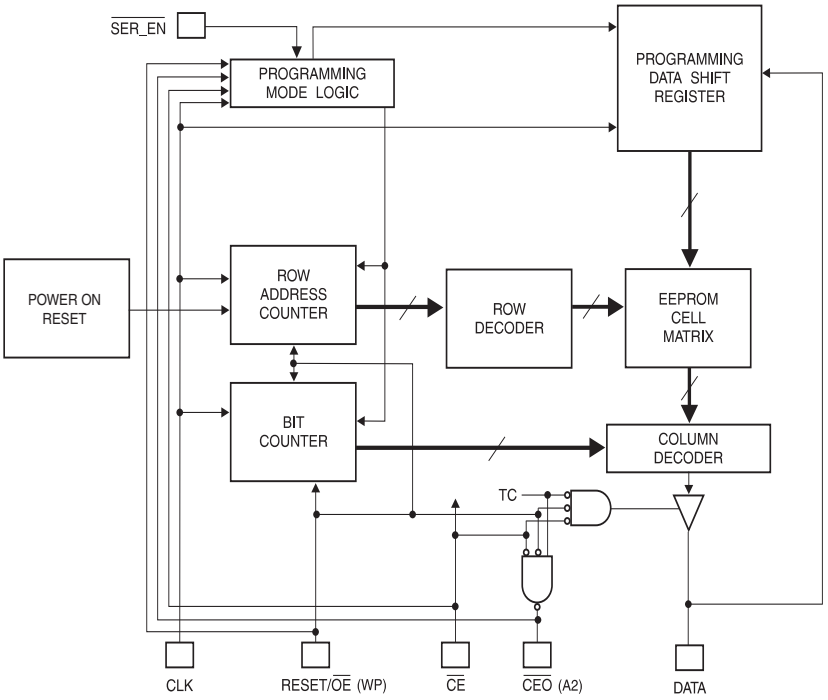
FPGA Configuration EEPROM Memory

64K, 128K and 256K

AT17C65
AT17LV65
AT17C128
AT17LV128
AT17C256
AT17LV256

Rev. 1636B–05/00

Block Diagram



FPGA Master Serial Mode Summary

The I/O and logic functions of the FPGA and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The AT17 Serial Configuration EEPROM has been designed for compatibility with the Master Serial Mode.

This document discusses the AT6000 FPGA interface. For more details or AT40K FPGA applications, please reference “AT6000 Series Configuration” or “AT40K Series Configuration” application notes.

Controlling the Low-density AT17 Series Serial EEPROMs During Configuration

Most connections between the FPGA device and the AT17 Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17 Series Configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17 Series Configurator.
- The $\overline{CEO}$ output of any AT17C/LV128/256 drives the $\overline{CE}$ input of the next AT17C/LV128/256 in a cascade chain of EEPROMs. An AT17C/LV65 can only be used at the end of a cascade chain or as a standalone device.
- $\overline{SER\_EN}$ must be connected to VCC (except during ISP).

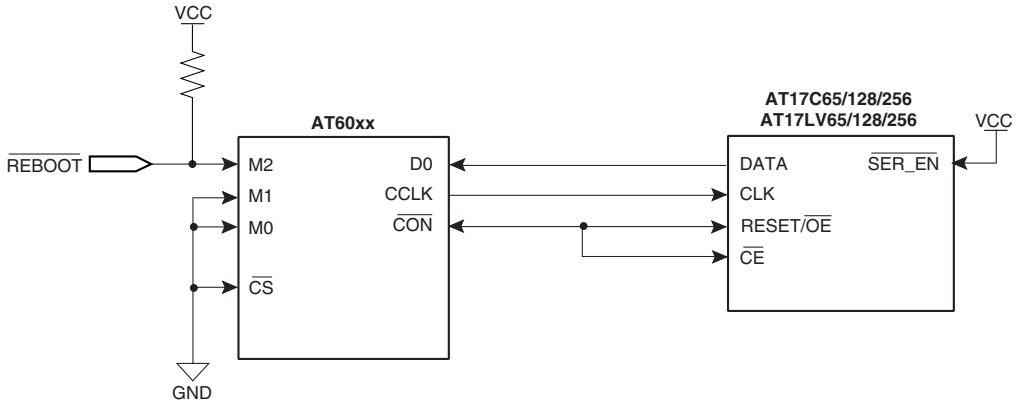
There are two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$.

Condition 1

The simplest connection is to have the FPGA $\overline{CON}$ pin drive both $\overline{CE}$ and RESET/$\overline{OE}$[1] in parallel (Figure 1). Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configuration cycle. If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the AT17 Series Configurator does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Note: 1. For this condition, the reset polarity of the EEPROM must be set active High.

Figure 1. Condition 1 Connection



Notes: 1. 4.7 kΩ resistors used unless otherwise specified.
2. Reset polarity of EEPROM must be set active High.

Condition 2

The FPGA $\overline{\text{CON}}$ pin drives only the $\overline{\text{CE}}$ input of the AT17 Series Configurator, while the RESET/$\overline{\text{OE}}$ input is driven by an input to the FPGA $\overline{\text{RESET}}$ input pin. This connection works under all normal circumstances, even when the user aborts a configuration before $\overline{\text{CON}}$ has gone High. A Low level on the RESET/$\overline{\text{OE}}$[1] input – during FPGA reset – clears the Configurator's internal address pointer, so that the reconfiguration starts at the beginning.

Note: 1. For this condition, the reset polarity of the EEPROM must be set active Low.

The AT17 Series Configurator does not require an inverter for either condition since the RESET polarity is programmable.

Cascading Serial Configuration EEPROMs (AT17C/LV128 and AT17C/LV256 only)[1]

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory.

After the last bit from the first Configurator is read, the next clock signal to the Configurator asserts its $\overline{\text{CEO}}$ output low and disables its DATA line driver. The second Configurator recognizes the Low level on its $\overline{\text{CE}}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded Configurators are reset if the RESET/$\overline{\text{OE}}$ on each Configurator is driven to its active (default High) level.

If the address counters are not to be reset upon completion, then the RESET/$\overline{\text{OE}}$ input can be tied to its inactive (default Low) level.

Note: 1. A single AT17C/LV65 may be used at the end of a cascade chain.

AT17 Series Reset Polarity

The AT17 Series Configurator allows the user to program the reset polarity as either RESET/$\overline{\text{OE}}$ or $\overline{\text{RESET}}$/OE. This feature is supported by industry-standard programmer algorithms. For more details on programming the EEPROM's reset polarity, please reference the "Programming Specification for Atmel's FPGA Configuration EEPROMs" application note.

Programming Mode

The programming mode is entered by bringing $\overline{\text{SER\_EN}}$ Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at VCC supply only. Programming super voltages are generated inside the chip. See the "Programming Specification for Atmel's FPGA Configuration EEPROMs" application note for further information. The AT17C parts are read/write at 5V nominal. The AT17LV parts are read/write at 3.3V nominal.

Standby Mode

The AT17C/LV65/128/256 enters a low-power standby mode whenever $\overline{\text{CE}}$ is asserted High. In this mode, the Configurator consumes less than 75 µA of current at 5.0V. The output remains in a high impedance state regardless of the state of the $\overline{\text{OE}}$ input.

Pin Configurations

20 PLCC/ SOIC Pin	8 DIP/ SOIC Pin	Name	I/O	Description
2	1	DATA	I/O	Three-state DATA output for configuration. Open-collector bi-directional pin for programming.
4	2	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
6	3	RESET/$\overline{OE}$	I	RESET/Output Enable input (when $\overline{SER\_EN}$ is High). A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This document describes the pin as RESET/$\overline{OE}$.
		WP	I	Write protect (WP) input (when $\overline{CE}$ is Low). When WP is Low, the entire memory can be written. When WP is enabled (High), the lowest block of the memory cannot be written. This feature is only active in the 2-wire serial Programming Mode (i.e., when $\overline{SER\_EN}$ is Low; see “Programming Specification” application note for more details).
8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will not enable/disable the device in the 2-wire Serial Programming Mode (i.e., when $\overline{SER\_EN}$ is Low).
10	5	GND		Ground pin. A 0.2 µF decoupling capacitor between VCC and GND is recommended.
14	6	$\overline{CEO}$	O	Chip Enable Output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter, $\overline{CEO}$ will stay High until the entire EEPROM is read again.
		A2	I	Device selection input, A2. This is used to enable (or select) the device during programming (i.e. when $\overline{SER\_EN}$ is Low; see the “Programming Specification” application note for more details.
17	7	$\overline{SER\_EN}$	I	Serial enable must be held High during FPGA loading operations. Bringing $\overline{SER\_EN}$ Low enables the 2-wire Serial Programming Mode.
20	8	VCC		+3.3V/+5V Power Supply Pin.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		AT17CXXX Min/Max	AT17LVXXX Min/Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75/5.25	3.0/3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5/5.5	3.0/3.6	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5/5.5	3.0/3.6	V

DC Characteristics

V_{CC} = 5V ± 5% Commercial/5V ± 10% Ind./Mil.

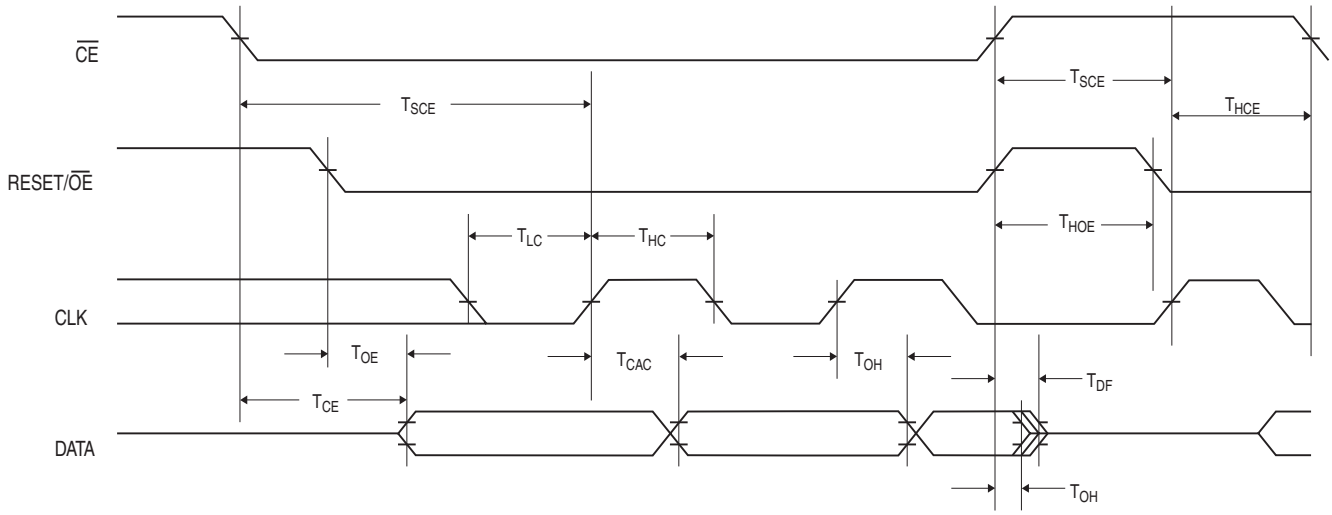
Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.6		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.5		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode			10	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		75	µA
		Industrial/Military		150	µA

DC Characteristics

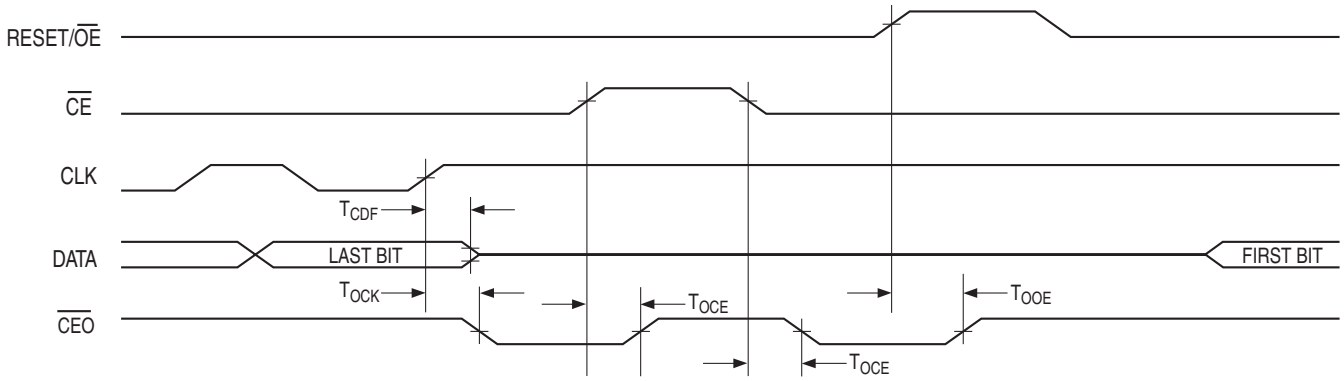
V_{CC} = 3.3V ± 10%

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -2.5 mA)	Commercial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Industrial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Military	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +2.5 mA)			0.4	V
I_{CCA}	Supply current, active mode			5	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		50	µA
		Industrial/Military		100	µA

AC Characteristics



AC Characteristics When Cascading



AC Characteristics for AT17C65/128

V_{CC} = 5V ± 5% Commercial/V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		30		35	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		50		50	ns
T_{CAC}[2]	CLK to Data Delay		50		55	ns
T_{OH}	Data Hold from $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	30		35		ns
T_{HC}	CLK High Time	30		35		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	45		50		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (guarantees counter is reset)	25		25		ns
F_{MAX}	MAX Input Clock Frequency	12.5		12.5		MHz

AC Characteristics for AT17C128 When Cascading

V_{CC} = 5V± 5% Commercial/V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50		50	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		55		60	ns
T_{OCE}[2]	$\overline{CE}$ to $\overline{CEO}$ Delay		55		60	ns
T_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		40		45	ns
F_{MAX}	MAX Input Clock Frequency	8		8		MHz

Notes:
1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

AC Characteristics for AT17C256

V_{CC} = 5V ±5% Commercial/V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		30		35	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		45		45	ns
T_{CAC}[2]	CLK to Data Delay		50		55	ns
T_{OH}	Data Hold from $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	20		20		ns
T_{HC}	CLK High Time	20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		40		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (guarantees counter is reset)	20		20		ns
F_{MAX}	MAX Input Clock Frequency	12.5		12.5		MHz

AC Characteristics for AT17C256 When Cascading

V_{CC} = 5V±5% Commercial/V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50		50	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		35		40	ns
T_{OCE}[2]	$\overline{CE}$ to $\overline{CEO}$ Delay		35		35	ns
T_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		30		35	ns
F_{MAX}	MAX Input Clock Frequency	10		10		MHz

Notes:
1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

AC Characteristics for AT17LV65/128/256

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		50		55	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		60		60	ns
T_{CAC}[2]	CLK to Data Delay		75		80	ns
T_{OH}	Data Hold from $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		55		55	ns
T_{LC}	CLK Low Time	25		25		ns
T_{HC}	CLK High Time	25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		60		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (guarantees counter is reset)	25		25		ns
F_{MAX}	MAX Input Clock Frequency	10		10		MHz

AC Characteristics for AT17LV128/256 When Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		60		60	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		55		60	ns
T_{OCE}[2]	$\overline{CE}$ to $\overline{CEO}$ Delay		55		60	ns
T_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		40		45	ns
F_{MAX}	MAX Input Clock Frequency	8		8		MHz

Notes:
1. Preliminary specifications for military operating range only.
2. AC test lead = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

Ordering Information – 5V Devices

Memory Size	Ordering Code	Package	Operation Range
64K	AT17C65-10PC AT17C65-10NC AT17C65-10JC AT17C65-10SC	8P3 8S1 20J 20S	Commercial (0°C to 70°C)
	AT17C65-10PI AT17C65-10NI AT17C65-10JI AT17C65-10SI	8P3 8S1 20J 20S	Industrial (-40°C to 85°C)
128K	AT17C128-10PC AT17C128-10NC AT17C128-10JC AT17C128-10SC	8P3 8S1 20J 20S	Commercial (0°C to 70°C)
	AT17C128-10PI AT17C128-10NI AT17C128-10JI AT17C128-10SI	8P3 8S1 20J 20S	Industrial (-40°C to 85°C)
256K	AT17C256-10PC AT17C256-10NC AT17C256-10JC AT17C256-10SC	8P3 8S1 20J 20S	Commercial (0°C to 70°C)
	AT17C256-10PI AT17C256-10NI AT17C256-10JI AT17C256-10SI	8P3 8S1 20J 20S	Industrial (-40°C to 85°C)

Package Type	
8P3	8-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20S	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

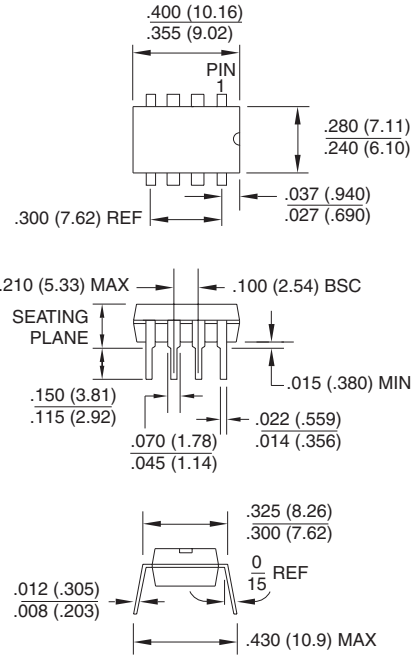
Ordering Information – 3.3V Devices

Memory Size	Ordering Code	Package	Operation Range
64K	AT17LV65-10PC	8P3	Commercial (0°C to 70°C)
	AT17LV65-10NC	8S1	
	AT17LV65-10JC	20J	
	AT17LV65-10SC	20S	
	AT17LV65-10PI	8P3	Industrial (-40°C to 85°C)
	AT17LV65-10NI	8S1	
	AT17LV65-10JI	20J	
	AT17LV65-10SI	20S	
128K	AT17LV128-10PC	8P3	Commercial (0°C to 70°C)
	AT17LV128-10NC	8S1	
	AT17LV128-10JC	20J	
	AT17LV128-10SC	20S	
	AT17LV128-10PI	8P3	Industrial (-40°C to 85°C)
	AT17LV128-10NI	8S1	
	AT17LV128-10JI	20J	
	AT17LV128-10SI	20S	
256K	AT17LV256-10PC	8P3	Commercial (0°C to 70°C)
	AT17LV256-10NC	8S1	
	AT17LV256-10JC	20J	
	AT17LV256-10SC	20S	
	AT17LV256-10PI	8P3	Industrial (-40°C to 85°C)
	AT17LV256-10NI	8S1	
	AT17LV256-10JI	20J	
	AT17LV256-10SI	20S	

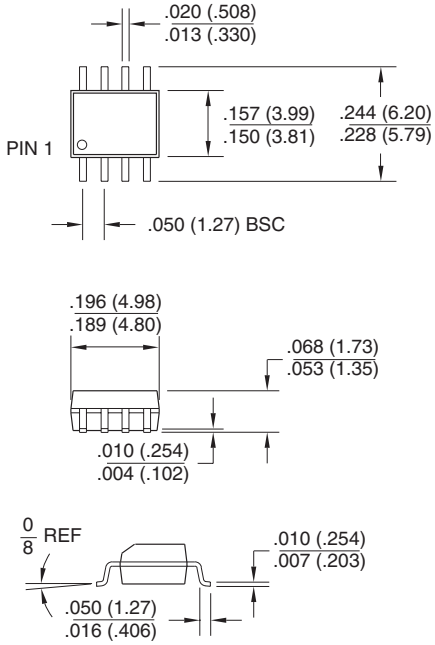
Package Type	
8P3	8-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20S	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Packaging Information

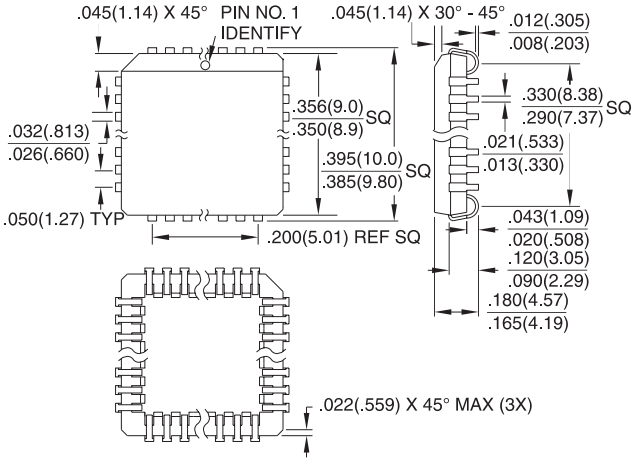
8P3, 8-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BA



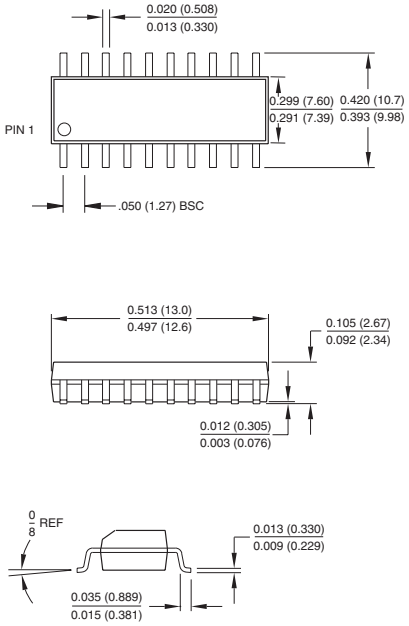
8S1, 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Dimensions in Inches and (Millimeters)



20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



20S, 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



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