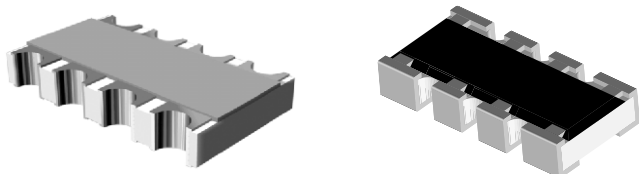


## Professional Thin Film Chip Resistor Array



ACAC 0612 (concave terminations) and ACAS 0612 (convex terminations) thin film chip resistor arrays combine the proven reliability of professional thin film chip resistor products with the advantages of chip resistor arrays. A small package enables the design of high density circuits in combination with reduction of assembly costs. Four equal resistor values or two pairs are available.

### FEATURES

- Advanced thin film technology
- Two pairs or four equal resistor values
- TCR down to  $\pm 25$  ppm/K
- Tolerance down to  $\pm 0.5$  %
- Pure Sn termination on Ni barrier layer
- Compliant to RoHS directive 2002/95/EC



**RoHS**  
COMPLIANT

### APPLICATIONS

- Voltage divider
- Feedback circuits
- Signal conditioning

TECHNICAL SPECIFICATIONS	
DESCRIPTION	ACAC 0612, ACAS 0612
EIA size	0612
Metric size	RR 1632M
Configuration, isolated	4 x 0603
Design:	
All equal	AE
Two pairs	TP
Resistance values	47 $\Omega$ to 221 k $\Omega$ <sup>(1)</sup>
Absolute tolerance <sup>(2)</sup>	$\pm 1$ %; $\pm 0.5$ %
Absolute temperature coefficient <sup>(2)</sup>	$\pm 50$ ppm/K; $\pm 25$ ppm/K
Max. resistance ratio $R_{min}/R_{max}$ .	1:10
Rated dissipation: $P_{70}$ <sup>(3)</sup>	
Element	0.1 W
Package, 4 x 0603	0.3 W
Operating voltage	75 V
Permissible film temperature	125 °C
Insulation voltage ( $U_{ins}$ ) against ambient and between isolated resistors, continuous	75 V

#### Notes

<sup>(1)</sup> Resistance values to be selected from E24 and E96

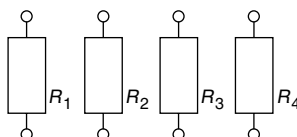
<sup>(2)</sup> For TCR tracking, tolerance matching and tighter absolute tolerance please refer to data sheet ACAC 0612, ACAS 0612 - Precision available on our web site at [www.vishay.com/doc?28751](http://www.vishay.com/doc?28751)

<sup>(3)</sup> Please refer to APPLICATION INFORMATION, see below

## APPLICATION INFORMATION

The power dissipation on the resistor generates a temperature rise against the local ambient, depending on the heat flow support of the printed-circuit board (thermal resistance). The rated dissipation applies only if the permitted film temperature is not exceeded. These resistors do not feature a limited lifetime when operated within the permissible limits.

## SKETCHES



ACAC 0612, ACAS 0612

DESIGN	
TYPE	ACAC 0612, ACAS 0612
AE	$R_1 = R_2 = R_3 = R_4$
TP	$R_1 = R_4 < R_2 = R_3$

PART NUMBER AND PRODUCT DESCRIPTION <sup>(1)</sup>																	
PART NUMBER: ACASA110012200P500																	
A	C	A	S	A	1	1	0	0	1	2	2	0	0	P	5	0	0
MODEL		TERMINAL		SIZE	RESISTANCE VALUE <sup>(2)</sup>		ACCURACY GRADE <sup>(3)</sup>		RESISTANCE VALUE <sup>(2)</sup>		PACKAGING <sup>(4)</sup>			SPECIAL			
ACA		C = Concave S = Convex square		A = 0612	3 digit resistance value <i>R</i> <sub>1</sub> , <i>R</i> <sub>4</sub> 1 digit multiplier  MULTIPLIER 9 = *10 <sup>-1</sup> 0 = *10 <sup>0</sup> 1 = *10 <sup>1</sup> 2 = *10 <sup>2</sup> 3 = *10 <sup>3</sup>		TCR and tolerance 1 2 3		3 digit resistance value <i>R</i> <sub>2</sub> , <i>R</i> <sub>3</sub> 1 digit multiplier  MULTIPLIER 9 = *10 <sup>-1</sup> 0 = *10 <sup>0</sup> 1 = *10 <sup>1</sup> 2 = *10 <sup>2</sup> 3 = *10 <sup>3</sup>		P1 P5			00 = Standard			
PRODUCT DESCRIPTION: ACAS 0612 110R 1 220R P5																	
ACA		S		0612		110R		1		220R		P5					
MODEL		TERMINATION		SIZE		RESISTANCE VALUE <i>R</i> <sub>1</sub> , <i>R</i> <sub>4</sub> <sup>(2)</sup>		ACCURACY GRADE <sup>(3)</sup>		RESISTANCE VALUE <i>R</i> <sub>2</sub> , <i>R</i> <sub>3</sub> <sup>(2)</sup>		PACKAGING <sup>(4)</sup>					
ACA = Chip Array		C = Concave S = Convex square		0612		110R = 110 Ω 1K1 = 1.1 kΩ 22K1 = 22.1 kΩ		TCR and tolerance 1 2 3		220R = 220 Ω 1K1 = 1.1 kΩ 22K1 = 22.1 kΩ		P1 P5					

### Notes

<sup>(1)</sup> Products can be ordered using either the PART NUMBER or the PRODUCT DESCRIPTION

<sup>(2)</sup>  $R_1 = R_4 \leq R_2 = R_3$

<sup>(3)</sup> Please refer to table TEMPERATURE COEFFICIENT AND RESISTANCE RANGE, see next page

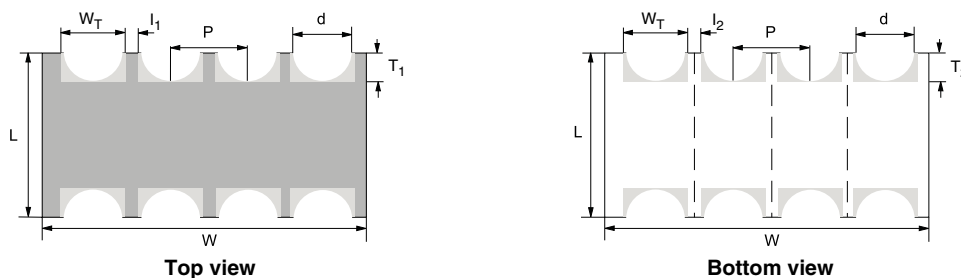
<sup>(4)</sup> Please refer to table PACKAGING, see next page

**TEMPERATURE COEFFICIENT AND RESISTANCE RANGE**

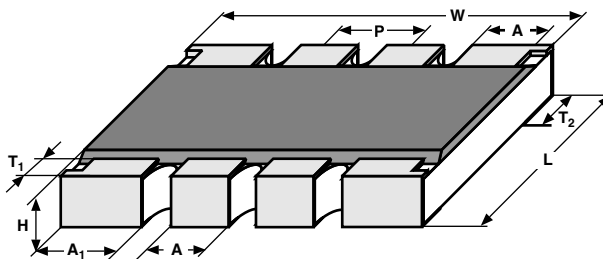
DESCRIPTION			RESISTANCE VALUE
ACCURACY GRADE	ABSOLUTE TCR	ABSOLUTE TOLERANCE	ACAC 0612, ACAS 0612
1	$\pm 25$ ppm/K	$\pm 0.5$ %	47 $\Omega$ to 221 k $\Omega$
2	$\pm 50$ ppm/K	$\pm 0.5$ %	47 $\Omega$ to 221 k $\Omega$
3	$\pm 50$ ppm/K	$\pm 1$ %	47 $\Omega$ to 221 k $\Omega$

**PACKAGING**

MODEL	TAPE WIDTH	DIAMETER	PIECES	PITCH	PACKAGING CODE
					PAPER TAPE
ACAC 0612	8 mm	180 mm/7"	1000	4 mm	P1
ACAS 0612	8 mm	180 mm/7"	5000	4 mm	P5

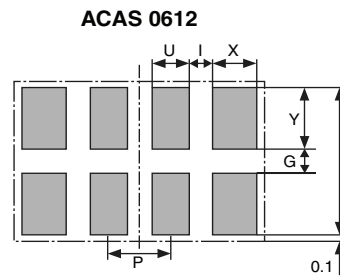
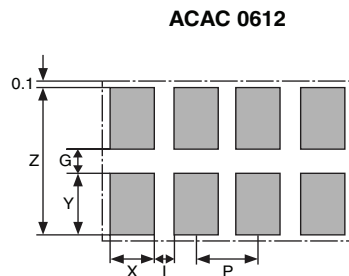
**DIMENSIONS ACAC 0612****DIMENSIONS** - Chip resistor array, mass and relevant physical dimensions


TYPE	L (mm)	W (mm)	H (mm)	P (mm)	W <sub>T</sub> (mm)	T <sub>1</sub> (mm)	T <sub>2</sub> (mm)	d (mm)	l <sub>1</sub> (mm)	l <sub>2</sub> (mm)	MASS (mg)
ACAC 0612	1.6 $\pm$ 0.15	3.2 $\pm$ 0.15	0.55 $\pm$ 0.1	0.8 $\pm$ 0.1	0.5 $\pm$ 0.15	0.3 $\pm$ 0.15	0.4 $\pm$ 0.15	0.3 $\pm$ 0.1	min. 0.15	min. 0.25	9.6

**DIMENSIONS ACAS 0612****DIMENSIONS** - Chip resistor array, mass and relevant physical dimensions

TYPE	L (mm)	W (mm)	H (mm)	P (mm)	A <sub>1</sub> (mm)	A (mm)	T <sub>1</sub> (mm)	T <sub>2</sub> (mm)	MASS (mg)
ACAS 0612	1.5 $\pm$ 0.15	3.2 $\pm$ 0.15	0.45 $\pm$ 0.1	0.8 $\pm$ 0.1	0.6 $\pm$ 0.1	0.4 $\pm$ 0.1	0.3 $\pm$ 0.15	0.4 $\pm$ 0.15	6.6

### PATTERN STYLES FOR CHIP RESISTOR ARRAYS



Dimensions in mm  
 limits for solder resist

### RECOMMENDED SOLDER PAD DIMENSIONS FOR CHIP RESISTOR ARRAYS

TYPE	G (mm)	Y (mm)	X (mm)	U (mm)	Z (mm)	I (mm)	P (mm)
ACAC 0612	0.7	0.7	0.5	-	2.1	0.3	0.8
ACAS 0612	0.7	0.7	0.64	0.5	2.1	0.3	0.8

### DESCRIPTION

The production of the components is strictly controlled and follows an extensive set of instructions established for reproducibility. A homogeneous film of metal alloy is deposited on a high grade (96 %  $\text{Al}_2\text{O}_3$ ) ceramic substrate using a mask to separate the adjacent resistors and conditioned to achieve the desired temperature coefficient. Specially designed inner contacts are realized on both sides. A special laser is used to achieve the target value by smoothly cutting a meander groove in the resistive layer without damaging the ceramics.

The resistor elements are covered by a protective coating designed for electrical, mechanical and climatic protection. The terminations receive a final pure tin on nickel plating.

The result of the determined production is verified by an extensive testing procedure and optical inspection performed on 100 % of the individual chip resistors. Only accepted products are laid directly into the paper tape in accordance with **IEC 60286-3** <sup>(3)</sup>.

### ASSEMBLY

The resistors are suitable for processing on automatic SMD assembly systems. They are suitable for automatic soldering using reflow or vapour phase as shown in **IEC 61760-1** <sup>(3)</sup>. For ACAC resistor arrays automatic soldering using wave can also be used. The encapsulation is resistant to all cleaning solvents commonly used in the electronics industry, including alcohols, esters and aqueous solutions.

The suitability of conformal coatings, if applied, shall be qualified by appropriate means to ensure the long-term stability of the whole system. The resistors are RoHS compliant; the pure tin plating provides compatibility with lead (Pb)-free and lead-containing soldering processes. The permitted storage time is 20 years, whereas the solderability is specified for 2 years after production or requalification. The immunity of the plating against tin whisker growth has been proven under extensive testing.

All products comply with the **GADSL** <sup>(1)</sup> and the **CEPIC-EECA-EICTA** <sup>(2)</sup> list of legal restrictions on hazardous substances. This includes full compliance with the following directives:

- 2000/53/EC End of Vehicle life Directive (ELV) and Annex II (ELV II)
- 2002/95/EC Restriction of the use of Hazardous Substances directive (RoHS)
- 2002/96/EC Waste Electrical and Electronic Equipment Directive (WEEE)

### TESTS

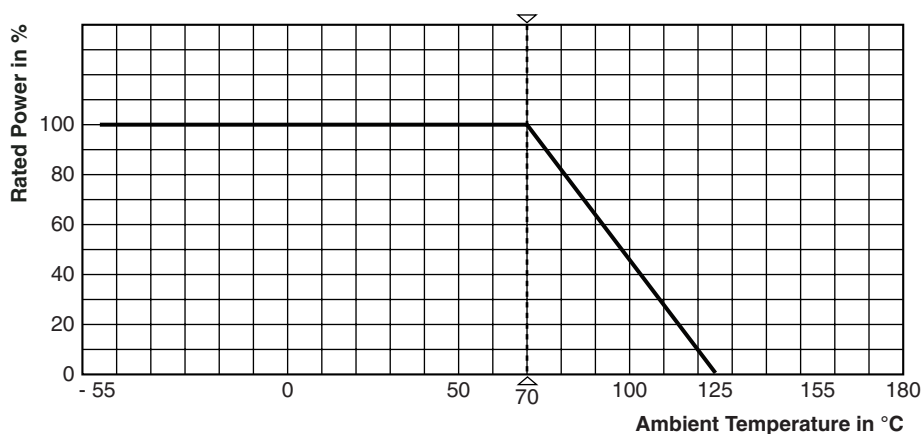
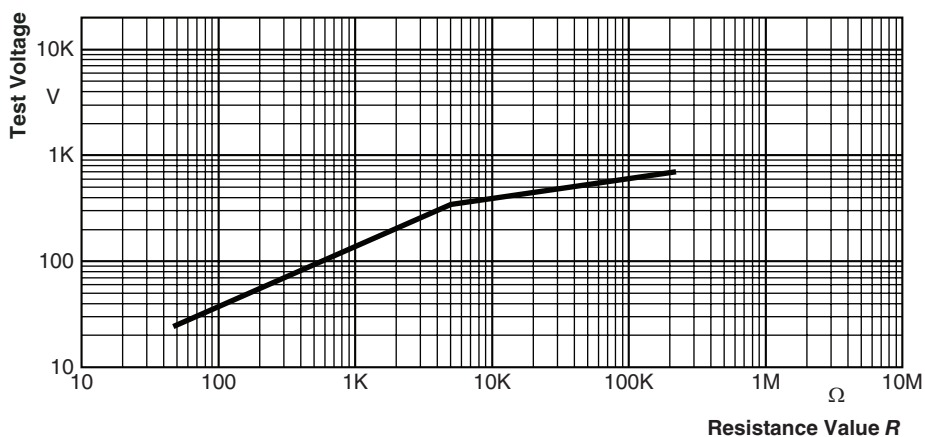
Where applicable, the resistors are tested in accordance with **EN 140401-801** which refers to **EN 60115-1** and **EN 140400**.

### Notes

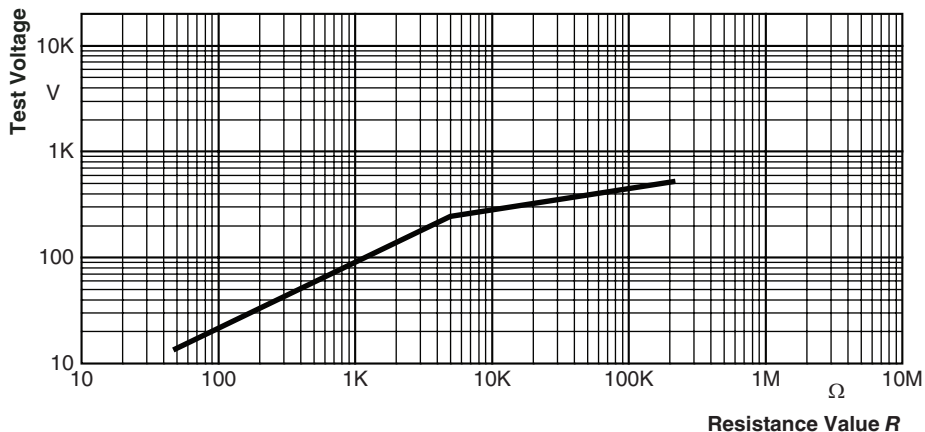
<sup>(1)</sup> Global Automotive Declarable Substance List, see [www.gadsl.org](http://www.gadsl.org)

<sup>(2)</sup> CEPIC (European Chemical Industry Council), EECA (European Electronic Component Manufacturers Association), EICTA (European trade organisation representing the information and communications technology and consumer electronics), see [www.eicta.org](http://www.eicta.org) → policy → environmental policy group → chemicals → jig → Joint Industry Guide (JIG-101 Ed 2.0)

<sup>(3)</sup> The quoted IEC standards are also released as EN standards with the same number and identical contents

**FUNCTIONAL PERFORMANCE****Derating**

Pulse load rating for arrays (ACAC 0612 or ACAS 0612) with equal values, design type AE, in accordance with EN 60115-1 clause 4.27; 1.2 μs/50 μs; 5 pulses at 12 s interval; for permissible resistance change  $(0.5 \% \times R + 0.05 \Omega)$

**1.2/50 Pulse**

Pulse load rating for arrays (ACAC 0612 or ACAS 0612) with equal values, design type AE in accordance with EN 60115-1 clause 4.27; 10 μs/700 μs; 10 pulses at 1 min intervals; for permissible resistance change  $(0.5 \% \times R + 0.05 \Omega)$

**10/700 Pulse**

### TESTS AND REQUIREMENTS

Essentially all tests are carried out in accordance with the following specifications:

**EN 60115-1**, generic specification

**EN 140400**, sectional specification

**EN 140401-801**, detail specification

The testing also covers most of the requirements specified by EIA/IS-703 and JIS-C-5202.

The tests are carried out in accordance with **IEC 60068 (1)** and under standard atmospheric conditions according to **IEC 60068-1 (1)**, 5.3. Climatic category LCT/UCT/56 (rated

temperature range: Lower Category Temperature, Upper Category Temperature; damp heat, long term, 56 days) is valid (LCT = - 55 °C/UCT = 125 °C).

Unless otherwise specified the following values apply:

Temperature: 15 °C to 35 °C

Relative humidity: 45 % to 75 %

Air pressure: 86 kPa to 106 kPa (860 mbar to 1060 mbar)

The requirements stated in the "Test Procedures and Requirements" table are based on the required tests and permitted limits of EN 140401-801 where applicable.

TEST PROCEDURES AND REQUIREMENTS				
EN 60115-1 CLAUSE	IEC 60068-2 (1) TEST METHOD	TEST	PROCEDURE	REQUIREMENTS (2) PERMISSIBLE CHANGE ( $\Delta R$ )
			Stability for product types:  <b>ACAC 0612</b> <b>ACAS 0612</b>	47 $\Omega$ to 221 k $\Omega$ 47 $\Omega$ to 221 k $\Omega$
4.5	-	Resistance	-	$\pm 1 \% R$ ; $\pm 0.5 \% R$ ; $\pm 0.25 \% R$
4.8.4.2	-	Temperature coefficient	At (20/- 55/20) °C and (20/125/20) °C	$\pm 50$ ppm/K; $\pm 25$ ppm/K
4.25.1	-	Endurance	$U = \sqrt{P_{70}} \times R$ or $U = U_{max.}$ ; 1.5 h on; 0.5 h off; 70 °C; 1000 h	$\pm (0.25 \% R + 0.05 \Omega)$
4.25.3	-	Endurance at upper category temperature	125 °C; 1000 h	$\pm (0.25 \% R + 0.05 \Omega)$
4.24	78 (Cab)	Damp heat, steady state	(40 $\pm$ 2) °C; 56 days; (93 $\pm$ 3) % RH	$\pm (0.5 \% R + 0.05 \Omega)$
4.13	-	Short time overload (3)	$U = 2.5 \times \sqrt{P_{70}} \times R$ or $U = 2 \times U_{max.}$ ; 5 s	$\pm (0.1 \% R + 0.01 \Omega)$ no visible damage
4.19	14 (Na)	Rapid change of temperature	30 min at - 55 °C and 30 min at 125 °C; 5 cycles	$\pm (0.1 \% R + 0.01 \Omega)$ no visible damage
4.18.2	58 (Td)	Resistance to soldering heat	Reflow method 2 (IR/forced gas convention); (260 $\pm$ 5) °C; (10 $\pm$ 1) s	$\pm (0.25 \% R + 0.01 \Omega)$ no visible damage

TEST PROCEDURES AND REQUIREMENTS				
EN 60115-1 CLAUSE	IEC 60068-2 <sup>(1)</sup> TEST METHOD	TEST	PROCEDURE	REQUIREMENTS <sup>(2)</sup> PERMISSIBLE CHANGE ( $\Delta R$ )
			Stability for product types:  <b>ACAC 0612</b> <b>ACAS 0612</b>	47 $\Omega$ to 221 k $\Omega$ 47 $\Omega$ to 221 k $\Omega$
4.17.2	58 (Td)	Solderability	Solder bath method; SnPb; non-activated flux accelerated ageing 4 h/155 °C (215 $\pm$ 3) °C; (3 $\pm$ 0.3) s  Solder bath method; SnAgCu; non-activated flux accelerated ageing 4 h/155 °C (235 $\pm$ 3) °C; (2 $\pm$ 0.2) s	Good tinning ( $\geq$ 95 % covered); no visible damage
4.32	21 (Ue <sub>3</sub> )	Shear (adhesion)	45 N	No visible damage
4.33	21 (Ue <sub>1</sub> )	Substrate bending	Depth 2 mm, 3 times	$\pm$ (0.1 % $R$ + 0.01 $\Omega$ ) no visible damage; no open circuit in bent position
4.7	-	Voltage proof	$U_{RMS} = U_{ins}$ (60 $\pm$ 5) s; against ambient, between adjacent resistors	No flashover or breakdown

**Notes**

<sup>(1)</sup> The quoted IEC standards are also released as EN standards with the same number and identical contents

<sup>(2)</sup> Figures are given for arrays with equal values, design type AE

<sup>(3)</sup> For a single element



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