



# AAT7551

## 20V P-Channel Power MOSFET

### General Description

The AAT7551 is a dual low threshold P-channel MOSFET designed for the battery, cell phone, and PDA markets. Using AnalogicTech's ultra-high-density MOSFET process and space-saving, small outline, J-lead package, performance superior to that normally found in a TSOP-6 footprint has been squeezed into the footprint of an SC70JW-8 package.

### Applications

- Battery Packs
- Battery-Powered Portable Equipment
- Cellular and Cordless Telephones

### Absolute Maximum Ratings

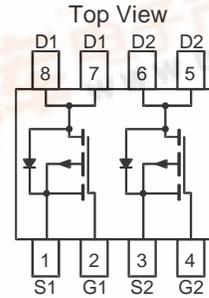
T<sub>A</sub> = 25°C, unless otherwise noted.

Symbol	Description	Value	Units
V <sub>DS</sub>	Drain-Source Voltage	-20	V
V <sub>GS</sub>	Gate-Source Voltage	±12	
I <sub>D</sub>	Continuous Drain Current @ T <sub>J</sub> = 150°C <sup>1</sup>	T <sub>A</sub> = 25°C	A
		T <sub>A</sub> = 70°C	
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	±8	
I <sub>S</sub>	Continuous Source Current (Source-Drain Diode) <sup>1</sup>	-0.6	
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C

### Features

- Drain-Source Voltage (max): -20V
- Continuous Drain Current<sup>1</sup> (max): -2.7A @ 25°C
- Low On-Resistance:
  - 100mΩ @ V<sub>GS</sub> = -4.5V
  - 175mΩ @ V<sub>GS</sub> = -2.5V

### Dual SC70JW-8 Package



### Thermal Characteristics<sup>1</sup>

Symbol	Description	Typ	Max	Units
R <sub>θJA</sub>	Junction-to-Ambient Steady State	132	165	°C/W
R <sub>θJA2</sub>	Junction-to-Ambient t<5 Seconds	83	104	
R <sub>θJF</sub>	Junction-to-Foot	60	72	
P <sub>D</sub>	Maximum Power Dissipation	T <sub>A</sub> = 25°C	1.2	W
		T <sub>A</sub> = 70°C	0.75	

1. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. R<sub>θJF</sub> + R<sub>θFA</sub> = R<sub>θJA</sub> where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. R<sub>θJF</sub> is guaranteed by design; however, R<sub>θCA</sub> is determined by the PCB design. Actual maximum continuous current is limited by the application's design.  
 2. Pulse test: Pulse Width = 300µs.



### Electrical Characteristics

$T_J = 25^\circ\text{C}$ , unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
<b>DC Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
$R_{DS(ON)}$	Drain-Source On-Resistance <sup>1</sup>	$V_{GS} = -4.5V, I_D = -2.7A$		80	100	m $\Omega$
		$V_{GS} = -2.5V, I_D = -2.0A$		140	175	
$I_{D(ON)}$	On-State Drain Current <sup>1</sup>	$V_{GS} = -4.5V, V_{DS} = -5V$ (pulsed)	-8			A
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu A$	-0.6			V
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS} = \pm 12V, V_{DS} = 0V$			$\pm 100$	nA
$I_{DSS}$	Drain Source Leakage Current	$V_{GS} = 0V, V_{DS} = -20V$			-1	$\mu A$
		$V_{GS} = 0V, V_{DS} = -16V, T_J = 70^\circ\text{C}$ <sup>2</sup>			-5	
$g_{fs}$	Forward Transconductance <sup>1</sup>	$V_{DS} = -5V, I_D = -2.7A$		4		S
<b>Dynamic Characteristics<sup>2</sup></b>						
$Q_G$	Total Gate Charge	$V_{DS} = -10V, R_D = 3.7\Omega, V_{GS} = -4.5V$		5.9		nC
$Q_{GS}$	Gate-Source Charge	$V_{DS} = -10V, R_D = 3.7\Omega, V_{GS} = -4.5V$		1		
$Q_{GD}$	Gate-Drain Charge	$V_{DS} = -10V, R_D = 3.7\Omega, V_{GS} = -4.5V$		2		
$t_{D(ON)}$	Turn-On Delay	$V_{DS} = -10V, R_D = 3.7\Omega, V_{GS} = -4.5V, R_G = 6\Omega$		22		ns
$t_R$	Turn-On Rise Time	$V_{DS} = -10V, R_D = 3.7\Omega, V_{GS} = -4.5V, R_G = 6\Omega$		10		
$t_{D(OFF)}$	Turn-Off Delay	$V_{DS} = -10V, R_D = 3.7\Omega, V_{GS} = -4.5V, R_G = 6\Omega$		20		
$t_F$	Turn-Off Fall Time	$V_{DS} = -10V, R_D = 3.7\Omega, V_{GS} = -4.5V, R_G = 6\Omega$		40		
<b>Source-Drain Diode Characteristics</b>						
$V_{SD}$	Source-Drain Forward Voltage <sup>1</sup>	$V_{GS} = 0, I_S = -2.7A$			-1.3	V
$I_S$	Continuous Diode Current <sup>3</sup>				-0.6	A

1. Pulse test: Pulse Width = 300 $\mu s$ .

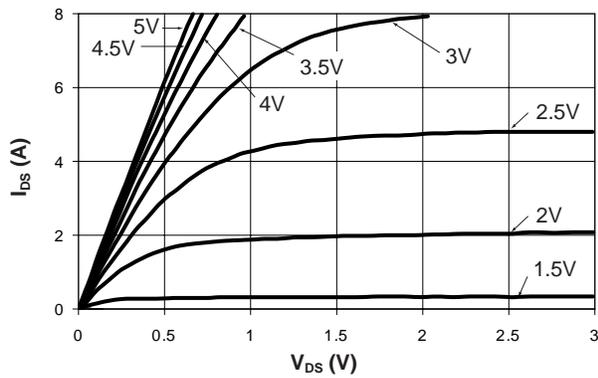
2. Guaranteed by design. Not subject to production testing.

3. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications.  $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$  where the foot thermal reference is defined as the normal solder mounting surface of the device's leads.  $R_{\theta JF}$  is guaranteed by design; however,  $R_{\theta CA}$  is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

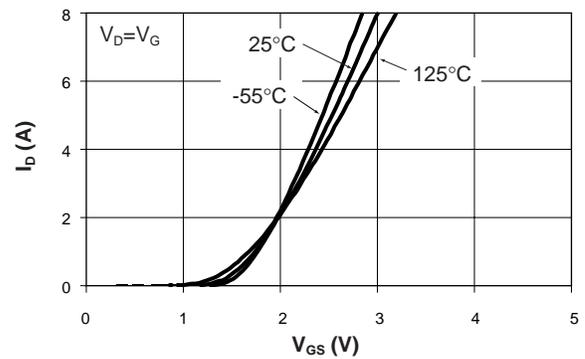
### Typical Characteristics

$T_J = 25^\circ\text{C}$ , unless otherwise noted.

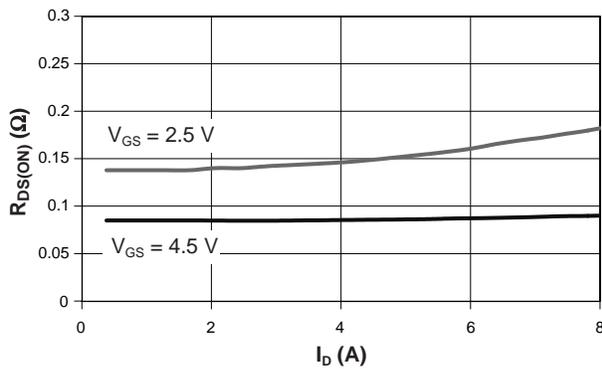
#### Output Characteristics



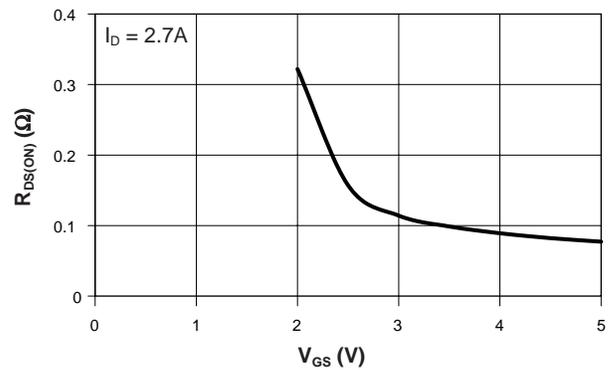
#### Transfer Characteristics



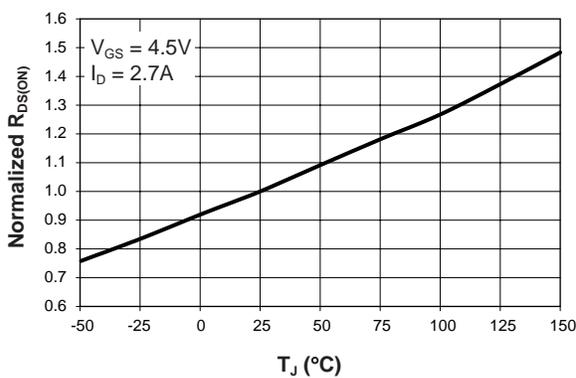
#### On-Resistance vs. Drain Current



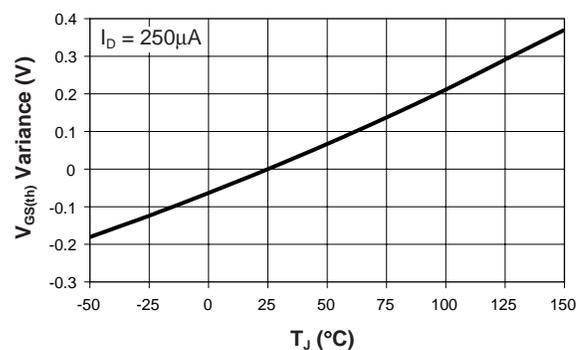
#### On-Resistance vs. Gate-to-Source Voltage



#### On-Resistance vs. Junction Temperature



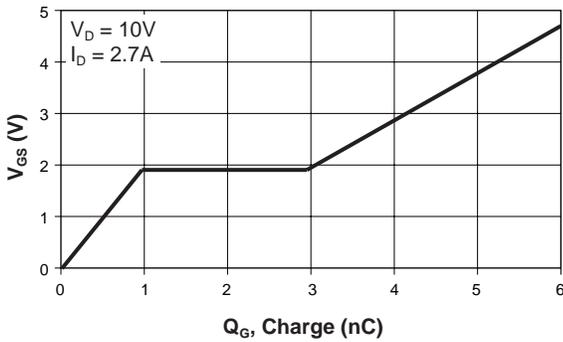
#### Threshold Voltage



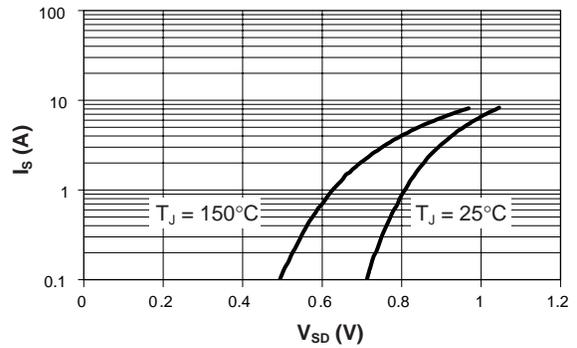
### Typical Characteristics

$T_J = 25^\circ\text{C}$ , unless otherwise noted.

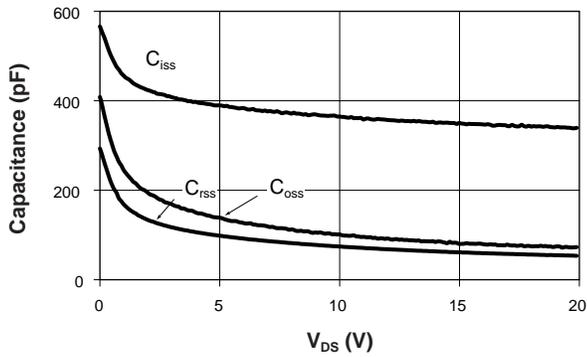
**Gate Charge**



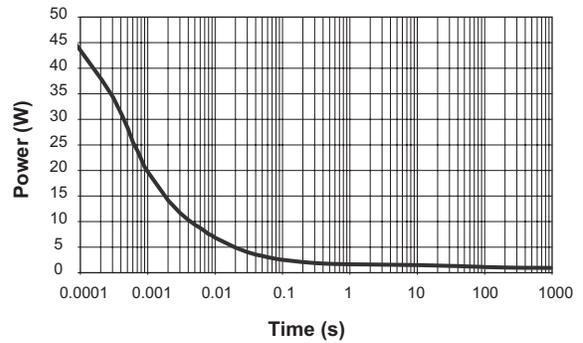
**Source-Drain Diode Forward Voltage**



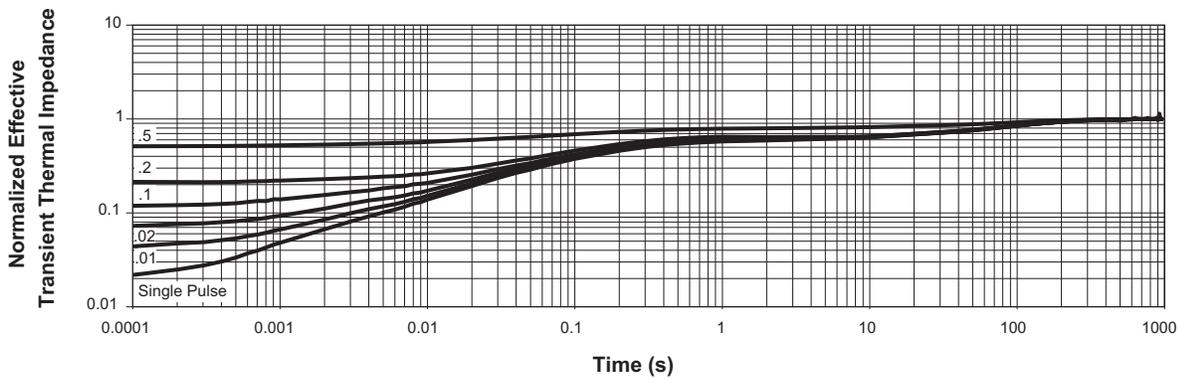
**Capacitance**



**Single Pulse Power, Junction to Ambient**



**Transient Thermal Response, Junction to Ambient**

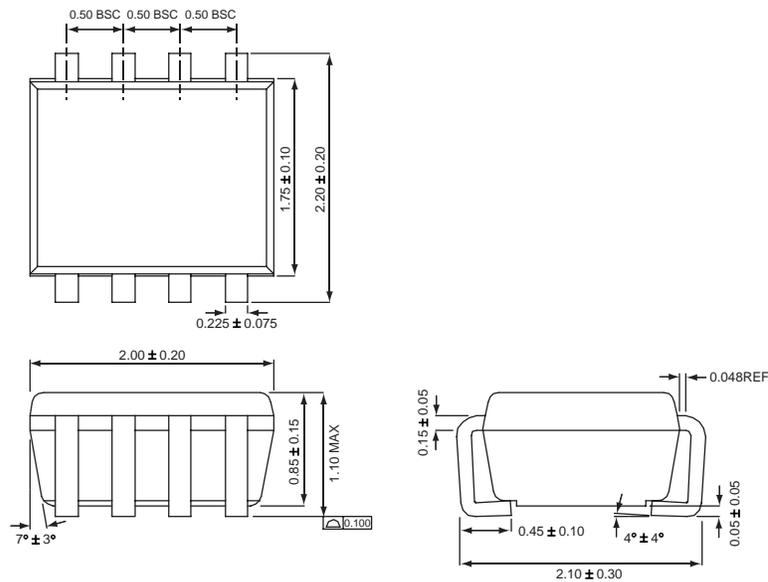


### Ordering Information

Package	Marking <sup>1</sup>	Part Number (Tape and Reel) <sup>2</sup>
SC70JW-8	KDXY	<b>AAT7551IJS-T1</b>

### Package Information

#### SC70JW-8



All dimensions in millimeters.

1. XYY = assembly and date code.  
 2. Sample stock is generally held on part numbers listed in **BOLD**.

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