1/3.2-Inch 13Mp CMOS Digital Image Sensor Die

AR1335 Die Datasheet, Rev. 3

For the latest data sheet, please visit: www.aptina.com

Features

- 13Mp CMOS sensor with advanced 1.1µm pixel BSI technology
- Data interfaces: two- and four-lane serial mobile industry processor interface (MIPI)
- Compression available for MIPI interface: DPCM 10-8-10 and 10-6-10 available for reduced interface clock speeds and lanes.
- 6.8 kbits (870 bytes) one-time programmable memory (OTPM) for storing shading correction coefficients of three light sources and module information
- Programmable controls: gain, horizontal and vertical blanking, auto black level offset correction, frame size/rate, exposure, left–right and top–bottom image reversal, window size, and panning
- Two on-die phase-locked loop (PLL) oscillators for super low noise performance
- Bayer pattern down-size scaler
- Superior low-light performance
- Low dark current
- Simple two-wire fast-mode+ serial interface
- Auto black level calibration
- On-chip lens shading correction
- Support for external mechanical shutter
- Support for external LED or xenon flash
- Extended Flash duration that is up to start of frame readout

General Physical Specifications

- Die thickness: 200µm ±12µm
  (Consult factory for other thickness)
- Backside wafer surface of bare silicon
- Bond pad metallization composition: 6000Å Al over Cu
- Typical topside passivation:
  1250Å Nitride over 2100Å Oxide
- Passivation openings (MIN): 88µm x 77µm

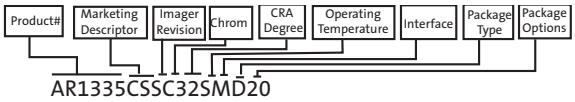
Order Information

AR1335CSSC32SMD20

Die Database

- Die outline, see Figure 2 on page 9
- Singulated die size
  – 6300 ± 25µm x 5700 ± 25µm
- Bond Pad Identification Tables, see pages 5–10

Options	Designator
• Form	
– Die	D
• Testing	
– Standard (level 1) probe	C1



Note: Consult die distributor or factory before ordering to verify long-term availability of these die products.

Key Performance Parameters

- Optical format: 1/3.2-inch (4:3)
- Active imager size: 4.6mm x 3.4mm: 5.7mm diagonal
- Active pixels: 4208H x 3120V
- Pixel size: 1.1µm x 1.1µm back side illumination (BSI)
- Color filter array: RGB Bayer pattern
- CRA: 32 degrees
- Shutter type
  – Electronic rolling shutter (ERS)
- Maximum data rate/master clock
  – MIPI: 1.2 Gbps/lane (4 lanes)
- Frame rate
  – 13Mp full resolution at 30 fps
- ADC resolution: 10-bit, on-die
- Responsivity: 0.83 V/lux-seconds
- Dynamic range: 68.8 dB
- SNR MAX: 35.6 dB

©Semiconductor Components Industries, LLC, 2014

‡This document contains information on a new product. Specifications and information herein are subject to change without notice.

Key Performance Parameters (continued)

- Supply voltage
  - Digital I/O: 1.7 - 1.9V (1.8V nominal)
  - Digital Core: 1.14-1.3V (1.2V nominal)
  - Analog: 2.6–2.9V (2.7V nominal)
  - Digital PHY: 1.14-1.3 (1.2V nominal)
- Power consumption:
  - Full resolution (MIPI): 270 mW at 60°C (Typ)
  - Hardware standby/shutdown: 50µA max. at 60°C (by XSHUTDOWN pin). No state retention.
- Operating temperature: –30°C to +70°C (at junction)

General Description

The ON Semiconductor AR1335 is a 1/3.2-inch CMOS active-pixel digital image sensor with a pixel array of 4208H x 3120V (4224H x 3136V including border pixels). It incorporates sophisticated on-chip camera functions such as windowing, mirroring, column and row skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface.

The AR1335 digital image sensor features ON Semiconductor's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The AR1335 sensor can generate full resolution image at up to 30 frames per second (fps). An on-chip analog-to-digital converter (ADC) generates a 10-bit value for each pixel.

Die Testing Procedures

ON Semiconductor imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in ON Semiconductor's standard package. Because the package environment is not within ON Semiconductor's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

ON Semiconductor retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. ON Semiconductor reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to ON Semiconductor's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

These specifications are provided for reference only. For target functional and parametric specifications, refer to the AR1335 Datasheet.

©Semiconductor Components Industries, LLC, 2014 .

Bonding Instructions

The AR1335 imager die has 58 bond pads. Refer to Table 1 and Table 2 on pages 5–8 for a complete list of bond pads and coordinates.

The AR1335 imager die does not require the user to determine bond option features.

The die also has several pads defined as ATEST or TEST. These pads are used for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die. Use of switching regulator may severely degrade the performance and is thus not recommended.

Figure 1 on page 4 shows the AR1335 typical die connections. For low-noise operation, the AR1335 die requires separate supplies for analog and digital power. Power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

ON Semiconductor recommends having all supplies of a certain voltage tied together. The ground of the 2.7V supplies and the 1.8V supplies is considered analog ground (AGND) and must be tied together closely. The ground of the 1.2V supply is considered digital ground (DGND) and all DGND must be tied together. Doing so will minimize risk of damage to the sensor in an ESD event. The cleanness of the 2.7V supply VAA_PIX and its associated analog ground AGND_PIX is essential to the pixel performance. It is recommended that star-connections are used to separate the traces for VAA_PIX and AGND_PIX. It is recommended that AGND_PIX is connected to the lowest potential point of AGND.

The 1.8V supply is used for both I/O purpose (VDD_IO) and analog purpose (VDDIO_ANA). For better performance, it is recommended that star-connections are used to separate the traces for VDD_IO and VDDIO_ANA.

The 1.2V supply/ground is used for both digital purpose (DVDD/DGND) and for analog purpose (DVDD_ANA/DGND_ANA). For better performance, it is recommended that star-connections are used to separate the traces for DVDD/DGND and DVDD_ANA/DGND_ANA).

To ensure the performance of the PLL, it is recommended that star-connections are used to separate the trace for VDD_PLL.

To ensure the performance of the MIPI, good power connection is recommended for DVDD_PHY. DVDD_PHY is internally connected to DVDD inside the chip. DVDD_PHY and DVDD can thus be tied together at module or board level.

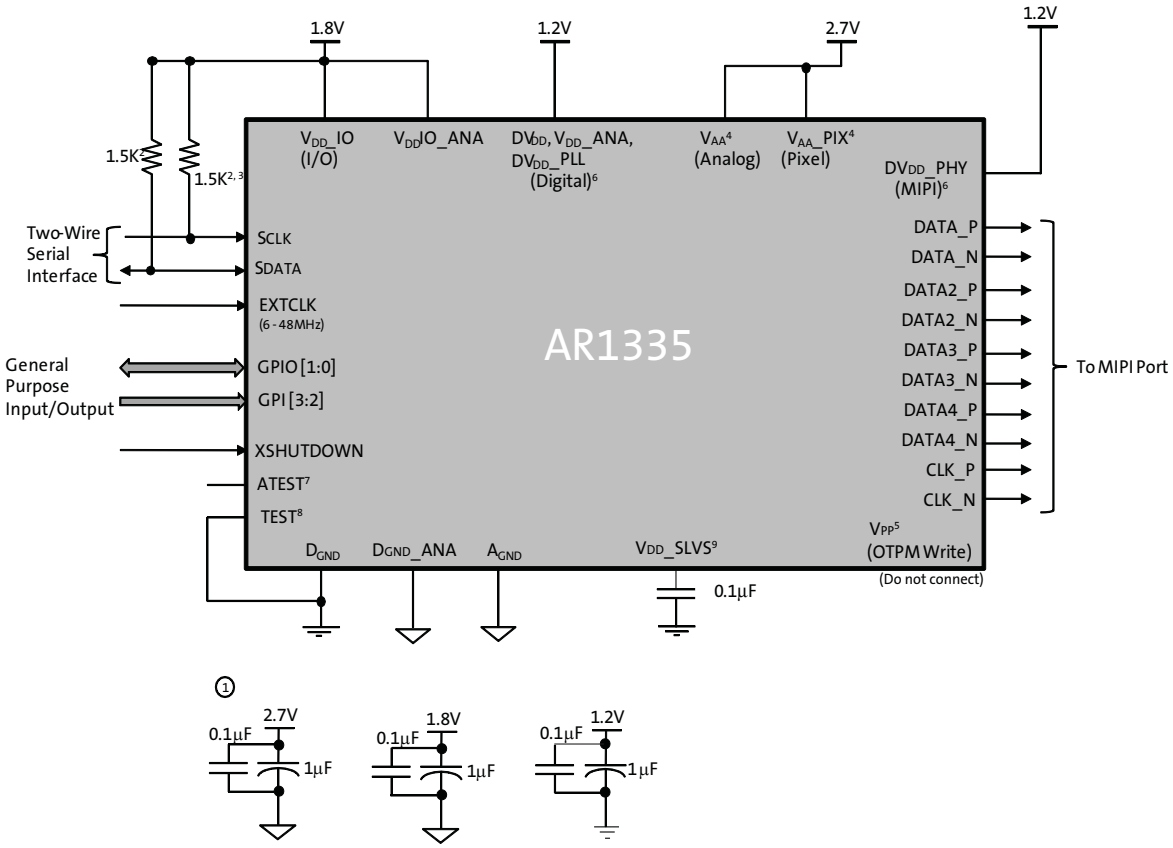
Storage Requirements

ON Semiconductor die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the die to a similar environment for storage. ON Semiconductor recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

©Semiconductor Components Industries, LLC, 2014 .

Typical Connections

Figure 1: Typical Connections



For connectivity above:

Notes:
1. All power supplies should be adequately decoupled; recommended cap values are:
   - 2.7V: 1.0µF and 0.1µF
   - 1.2V: 1.0uF and 0.1µF
   - 1.8V: 1.0uF and 0.1µF
2. Resistor value 1.5kΩ is recommended, but may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. VAA and VAA_PIX must be tied together.
5. Internal charge pump is used for OTPM programming.
6. Digital and MIPI supply can be tied together.
7. ATEST must be left floating.
8. TEST pin must be tied to DGND.
9. VDD_SLVS must be connected to DGND with a bypass cap (0.1uF).

©Semiconductor Components Industries, LLC, 2014 .

Bond Pad Identification Tables

Table 1: Bond Pad Location and Identification from Center of Pad1

Pad Number	Pad Name	"X"[1] µm	"Y"[1] µm
1	DVDD	0.0	0.0
2	DGND	0.0	-203.8
3	TEST	0.0	-357.0
4	DVDD	0.0	-580.2
5	DGND	0.0	-742.0
6	GPI3	0.0	-885.8
7	GPI2	0.0	-1025.8
8	DVDD	0.0	-1249.0
9	SDATA	0.0	-1365.2
10	SCLK	0.0	-1479.8
11	DGND	0.0	-1992.4
12	DVDD	0.0	-2277.8
13	VPP	0.0	-2470.6
14	VDD_IO	0.0	-2597.0
15	GPIO1	0.0	-2796.2
16	GPIO0	0.0	-2908.2
17	XSHUTDOWN	0.0	-3044.8
18	AGND	0.0	-3319.4
19	VAA_PIX	0.0	-3495.6
20	ATEST1	0.0	-3756.0
21	VAA	0.0	-3892.4
22	AGND	0.0	-4068.6
23	VAA	0.0	-4194.8
24	AGND	0.0	-4371.0
25	VDDIO_ANA	0.0	-4548.4
26	DVDD_ANA	0.0	-4754.0
27	DGND_ANA	0.0	-4957.0
28	DGND_ANA	-5956.0	-5059.2
29	DVDD_ANA	-5956.0	-4856.2
30	VDD_IO	-5956.0	-4650.6
31	AGND	-5956.0	-4473.2
32	VAA	-5956.0	-4297.0
33	AGND	-5956.0	-4185.8
34	ATEST2	-5956.0	-4010.2
35	VAA_PIX	-5956.0	-3800.6
36	AGND	-5956.0	-3624.4
37	DVDD_PHY2	-5956.0	-3314.0
38	DATA4_N	-5956.0	-3174.0
39	DATA4_P	-5956.0	-3014.0
40	DATA3_N	-5956.0	-2854.0
41	DATA3_P	-5956.0	-2694.0
42	DGND	-5956.0	-2534.0
43	VDD_SLVS	-5956.0	-2374.0
44	CLK_N	-5956.0	-2214.0

©Semiconductor Components Industries, LLC, 2014 .

Table 1: Bond Pad Location and Identification from Center of Pad1 (continued)

Pad Number	Pad Name	"X"[1] µm	"Y"[1] µm
45	CLK_P	-5956.0	-2054.0
46	DATA2_N	-5956.0	-1894.0
47	DATA2_P	-5956.0	-1734.0
48	DATA1_N	-5956.0	-1574.0
49	DATA1_P	-5956.0	-1414.0
50	DVDD_PHY1	-5956.0	-1274.0
51	DVDD	-5956.0	-1026.2
52	DGND	-5956.0	-799.2
53	VDD_IO	-5956.0	-683.2
54	EXTCLK	-5956.0	-571.8
55	DVDD	-5956.0	-457.2
56	DGND	-5956.0	-230.2
57	DVDD_PLL1	-5956.0	44.6
58	DVDD_PLL2	-5956.0	269.0

Note: 1. Reference to center of each bond pad from center of bond pad 1.

©Semiconductor Components Industries, LLC, 2014 .

Table 2: Bond Pad Location and Identification from Center of Die (0,0)

Pad Number	Pad Name	"X" µm	"Y" µm
1	DVDD	2978.0	2397.6
2	DGND	2978.0	2193.8
3	TEST	2978.0	2040.6
4	DVDD	2978.0	1817.4
5	DGND	2978.0	1655.6
6	GPI3	2978.0	1511.8
7	GPI2	2978.0	1371.8
8	DVDD	2978.0	1148.6
9	SDATA	2978.0	1032.4
10	SCLK	2978.0	917.8
11	DGND	2978.0	405.2
12	DVDD	2978.0	119.8
13	VPP	2978.0	-73.0
14	VDD_IO	2978.0	-199.4
15	GPIO1	2978.0	-398.6
16	GPIO0	2978.0	-510.6
17	XSHUTDOWN	2978.0	-647.2
18	AGND	2978.0	-921.8
19	VAA_PIX	2978.0	-1098.0
20	ATEST1	2978.0	-1358.4
21	VAA	2978.0	-1494.8
22	AGND	2978.0	-1671.0
23	VAA	2978.0	-1797.2
24	AGND	2978.0	-1973.4
25	VDDIO_ANA	2978.0	-2150.8
26	DVDD_ANA	2978.0	-2356.4
27	DGND_ANA	2978.0	-2559.4
28	DGND_ANA	-2978.0	-2661.6
29	DVDD_ANA	-2978.0	-2458.6
30	VDD_IO	-2978.0	-2253.0
31	AGND	-2978.0	-2075.6
32	VAA	-2978.0	-1899.4
33	AGND	-2978.0	-1788.2
34	ATEST2	-2978.0	-1612.6
35	VAA_PIX	-2978.0	-1403.0
36	AGND	-2978.0	-1226.8
37	DVDD_PHY2	-2978.0	-916.4
38	DATA4_N	-2978.0	-776.4
39	DATA4_P	-2978.0	-616.4
40	DATA3_N	-2978.0	-456.4
41	DATA3_P	-2978.0	-296.4
42	DGND	-2978.0	-136.4
43	VDD_SLVS	-2978.0	23.6
44	CLK_N	-2978.0	183.6
45	CLK_P	-2978.0	343.6

©Semiconductor Components Industries, LLC, 2014 .

Table 2: Bond Pad Location and Identification from Center of Die (0,0)

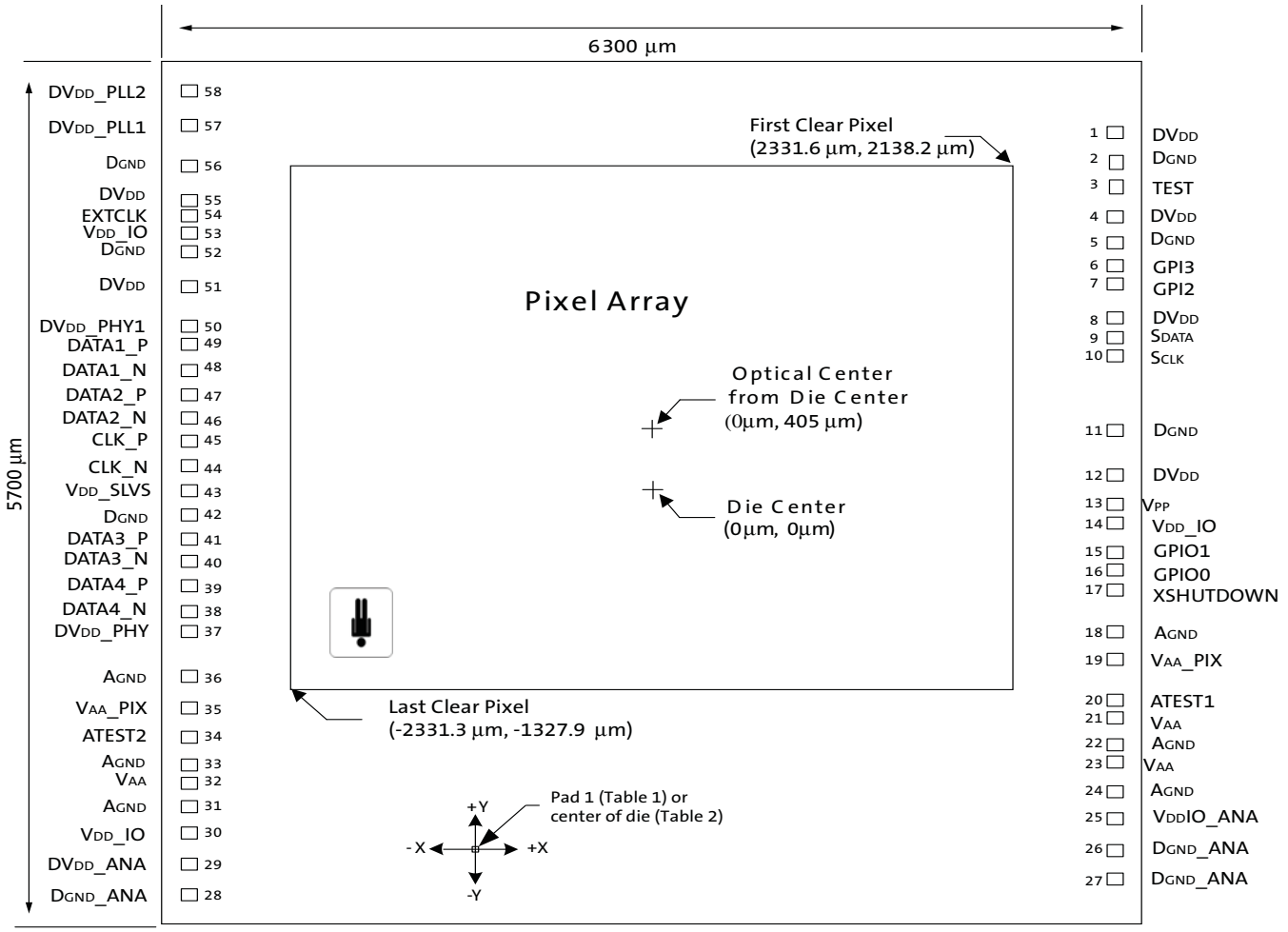
Pad Number	Pad Name	"X" µm	"Y" µm
46	DATA2_N	-2978.0	503.6
47	DATA2_P	-2978.0	663.6
48	DATA1_N	-2978.0	823.6
49	DATA1_P	-2978.0	983.6
50	DVDD_PHY1	-2978.0	1123.6
51	DVDD	-2978.0	1371.4
52	DGND	-2978.0	1598.4
53	VDD_IO	-2978.0	1714.4
54	EXTCLK	-2978.0	1825.8
55	DVDD	-2978.0	1940.4
56	DGND	-2978.0	2167.4
57	DVDD_PLL1	-2978.0	2442.2
58	DVDD_PLL2	-2978.0	2666.6

Note: 1. Reference to center of each bond pad from center of die(0,0).

©Semiconductor Components Industries, LLC, 2014 .

Die Features

Figure 2: Conceptual Die Mechanical Layout



©Semiconductor Components Industries, LLC, 2014 .

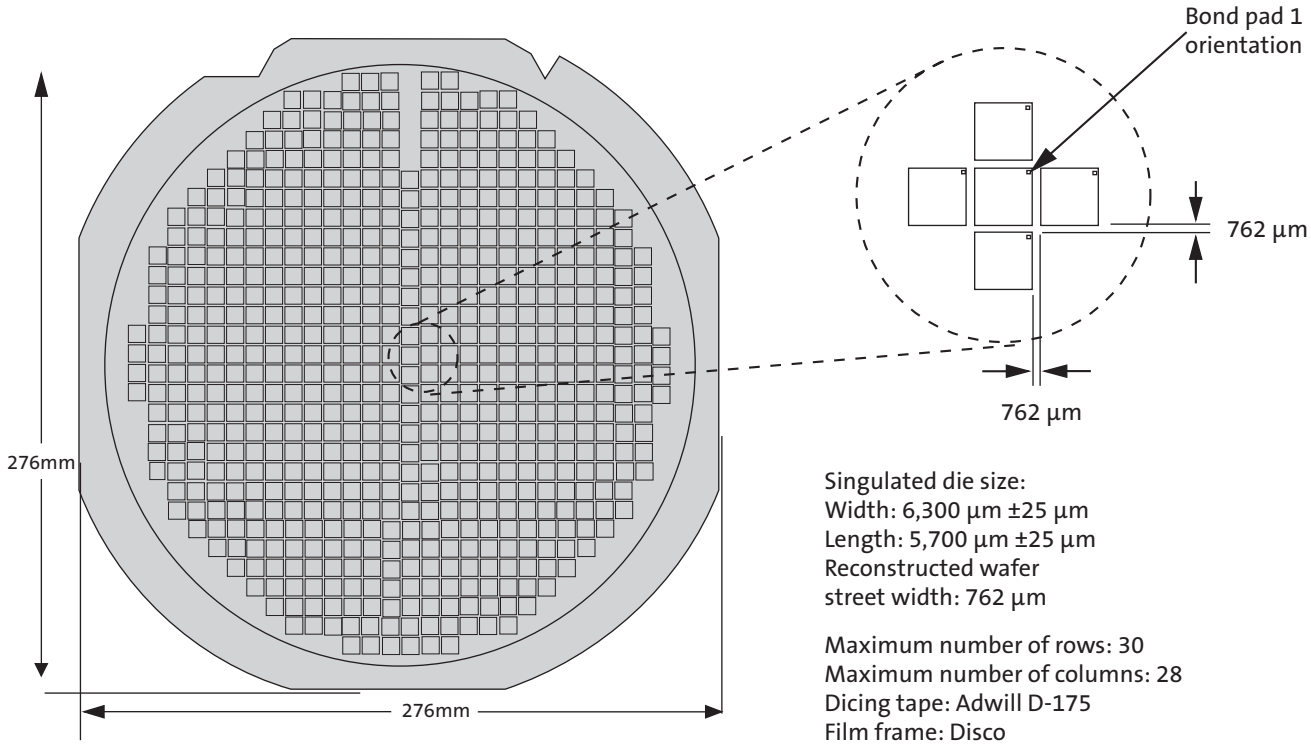
Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm
Die thickness	200µm ± 12µm
Singulated die size (after wafer saw)	6300 ± 25µm
	5700 ± 25µm
Bond pad size (MIN)	96µm x 85µm
Passivation openings (MIN)	88µm x 77µm
Minimum bond pad pitch	100µm
Optical array Optical center from die center: Optical center from center of pad1:	 0µm, 405µm –2978µm, –1992.6µm
First active pixel From die center: From center of pad1:	 2331.6µm, 2138.2µm –646.4 µm, –259.4 µm
Last active pixel From die center: From center of pad1:	 –2331.3µm, –1327.9µm –5309.3µm, –3725.5µm

©Semiconductor Components Industries, LLC, 2014 .

Figure 3: Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 6,300 µm ±25 µm
Length: 5,700 µm ±25 µm
Reconstructed wafer
street width: 762 µm

Maximum number of rows: 30
Maximum number of columns: 28
Dicing tape: Adwill D-175
Film frame: Disco

Maximum total die count: 627

©Semiconductor Components Industries, LLC, 2014 .

Revision History

Rev. 3 . . . . . 11/20/14

- Added VDD_SLVS to and updated notes for Figure 1: “Typical Connections,” on page 4
- Changed DVDD to VDD_SLVS for Pad Number 43 in Table 1: “Bond Pad Location and Identification from Center of Pad1,” on page 5, Table 2: “Bond Pad Location and Identification from Center of Die (0,0),” on page 7, and Figure 2: “Conceptual Die Mechanical Layout,” on page 9.

Rev. 2 . . . . . 11/11/14

- Updated to Preliminary
- Updated to ON Semiconductor template
- Updated “Key Performance Parameters” on page 1
- Updated “Key Performance Parameters (continued)” on page 2
- Updated “Bonding Instructions” on page 3
- Updated Figure 2: “Conceptual Die Mechanical Layout,” on page 9
- Updated Figure 3: “Die Orientation in Reconstructed Wafer,” on page 11

Rev. 1 . . . . . 4/3/14

- Initial release

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC’s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.