REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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PAGE	18	19	20	21	22	23	24	25														
REV STATUS OF PAGES	**REV**																					
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A

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TITLE

MICROCIRCUIT, LINEAR, QUAD CHANNEL DIGITAL ISOLATOR, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**
A	**16236**

DWG NO.
V62/14630

REV

PAGE 1 **OF** 25

AMSC N/A

5962-V102-15

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad channel, digital isolator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14630	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADUM3401	Quad channel, digital isolator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-013-AA	Small outline surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltages (V_{DD1}, V_{DD2}) ..... -0.5 V to +7.0 V 2/
Input voltages (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2}) ..... -0.5 V to V_{DDI} + 0.5 V 2/ 3/
Output voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD}) ..... -0.5 V to V_{DDO} + 0.5 V 2/ 3/
Average output current per pin: 4/
Side 1 (I_{O1}) ..... -18 mA to +18 mA
Side 2 (I_{O2}) ..... -22 mA to +22 mA
Common mode transients (CM_H, CM_L) ..... -100 kV/μs to +100 kV/μs 5/
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 6/

Supply voltages (V_{DD1}, V_{DD2}) ..... 3.135 V to 5.5 V 2/
Input signal rise and fall times ..... 1.0 ms
Operating temperature range (T_A) ..... -55°C to +125°C

1.5 Package characteristics.

Resistance (input to output) (R_{IO}) ..... 10^{12} Ω typical 7/
Capacitance (input to output) (C_{IO}) with f = 1 MHz ..... 2.2 pF typical 7/
Input capacitance (C_I) ..... 4.0 pF typical 8/
Integrated circuit junction to case thermal resistance:
Thermocouple located at center of package underside.
Side 1 (θ_{JCI}) ..... 33°C/W typical
Side 2 (θ_{JCO}) ..... 28°C/W typical

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltages are relative to their respective ground.
3/ V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
4/ See figure 5 for maximum rated current values for various temperatures.
5/ Refers to common mode transients across the insulation barrier. Common mode transients exceeding the absolute maximum ratings can cause latch up or permanent damage.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
7/ Device considered a 2 terminal device; V_{DD1} pin to GND1 pin are shorted together, and GND2 pin to V_{DD2} pin are shorted together.
8/ Input capacitance is from any input data pin to ground.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Thermal derating curve. The thermal derating curve shall be as shown in figure 5.

3.5.6 Data rate graphs. The data rate graphs shall be as shown in figures 6 through 10.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 5 V operation 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications							
Input supply current per channel, quiescent	$I_{DDI (Q)}$		-55°C to +125°C	01		0.83	mA
			+25°C		0.57 typical		
Output supply current per channel, quiescent	$I_{DDO (Q)}$		-55°C to +125°C	01		0.35	mA
			+25°C		0.29 typical		
Total supply current	3/	DC to 2 Mbps					
V_{DD1} supply current	$I_{DD1(Q)}$	DC to 1 MHz logical signal frequency	-55°C to +125°C	01		3.2	mA
			+25°C		2.5 typical		
V_{DD2} supply current	$I_{DD2(Q)}$	DC to 1 MHz logical signal frequency	-55°C to +125°C	01		2.4	mA
			+25°C		1.6 typical		
Total supply current	3/	10 Mbps					
V_{DD1} supply current	$I_{DD1(10)}$	5 MHz logical signal frequency	-55°C to +125°C	01		10.6	mA
			+25°C		7.4 typical		
V_{DD2} supply current	$I_{DD2(10)}$	5 MHz logical signal frequency	-55°C to +125°C	01		6.5	mA
			+25°C		4.4 typical		
DC specifications							
Input leakage per channel	I_I	$0 V \le V_{IX} \le V_{DDX}$	-55°C to +125°C	01	-10	+10	µA
			+25°C		+0.01 typical		
V_{EX} input pull up current	I_{PU}	$V_{EX} = 0 V$	-55°C to +125°C	01	-10		µA
			+25°C		-3 typical		
Tristate leakage current per channel	I_{OZ}		-55°C to +125°C	01	-10	+10	µA
			+25°C		+0.01 typical		
Logic high input threshold	V_{IH}, V_{EH}		-55°C to +125°C	01	2.0		V
Logic low input threshold	V_{IL}, V_{EL}		-55°C to +125°C	01		0.8	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5 V operation 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Logic high output voltages	V_{OAH}, V_{OBH}	I_{OX} = -20 µA, $V_{IX} = V_{IXH}$ 4/ 5/	-55°C to +125°C	01	(V_{DD1} or V_{DD2}) – 0.1		V
			+25°C		5.0 typical		
	V_{OCH}, V_{ODH}	I_{OX} = -4 mA, $V_{IX} = V_{IXH}$ 4/ 5/	-55°C to +125°C		(V_{DD1} or V_{DD2}) – 0.4		
			+25°C		4.8 typical		
Logic low output voltage	V_{OAL}, V_{OBL}	I_{OX} = 20 µA, $V_{IX} = V_{IXL}$ 4/ 6/	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
	V_{OCL}, V_{ODL}	I_{OX} = 400 µA, $V_{IX} = V_{IXL}$ 4/ 6/	-55°C to +125°C			0.1	
			+25°C		0.04 typical		
		I_{OX} = 4 mA, $V_{IX} = V_{IXL}$ 4/ 6/	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Switching specifications.							
Minimum pulse width	PW	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		100	ns
Maximum data rate		C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01	10		Mbps
Propagation delay	t_{PHL}, t_{PLH}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01	20	50	ns
			+25°C		32 typical		
Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		3	ns
Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$ change versus temperature		C_L = 15 pF, CMOS signal levels	+25°C	01	5 typical		ps/°C
Propagation delay skew	t_{PSK}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		15	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5 V operation 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching specifications – continued.							
Channel to channel matching, codirectional channels	t_{PSKCD}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		3	ns
Channel to channel matching, opposing directional channels	t_{PSKOD}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		6	ns
Output propagation delay, disable (high/low to high impedance)	t_{PHZ}, t_{PLZ}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		8	ns
			+25°C		6 typical		
Output propagation delay, enable (high impedance to high/low)	t_{PZH}, t_{PZL}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		8	ns
			+25°C		6 typical		
Output rise/fall time (10% to 90%)	t_R / t_F	C_L = 15 pF, CMOS signal levels	+25°C	01	2.5 typical		ns
Common mode 7/ transient immunity logic high output	$\|CM_H\|$	$V_{IX} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/μs
			+25°C		35 typical		
Common mode 7/ transient immunity logic low output	$\|CM_L\|$	V_{IX} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/μs
			+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.2 typical		Mbps
Dynamic supply current per channel, input	$I_{DDI(D)}$	8/	+25°C	01	0.20 typical		mA/ Mbps
Dynamic supply current per channel, output	$I_{DDO(D)}$	8/	+25°C	01	0.05 typical		mA/ Mbps

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 3.3 V operation 9/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications							
Input supply current per channel, quiescent	$I_{DDI (Q)}$		-55°C to +125°C	01		0.49	mA
			+25°C		0.31 typical		
Output supply current per channel, quiescent	$I_{DDO (Q)}$		-55°C to +125°C	01		0.27	mA
			+25°C		0.19 typical		
Total supply current	3/	DC to 2 Mbps					
V_{DD1} supply current	$I_{DD1(Q)}$	DC to 1 MHz logical signal frequency	-55°C to +125°C	01		1.9	mA
			+25°C		1.4 typical		
V_{DD2} supply current	$I_{DD2(Q)}$	DC to 1 MHz logical signal frequency	-55°C to +125°C	01		1.5	mA
			+25°C		0.9 typical		
Total supply current	3/	10 Mbps					
V_{DD1} supply current	$I_{DD1(10)}$	5 MHz logical signal frequency	-55°C to +125°C	01		5.6	mA
			+25°C		4.1 typical		
V_{DD2} supply current	$I_{DD2(10)}$	5 MHz logical signal frequency	-55°C to +125°C	01		3.3	mA
			+25°C		2.5 typical		
DC specifications							
Input leakage per channel	I_I	$0 V \le V_{IX} \le V_{DDX}$	-55°C to +125°C	01	-10	+10	µA
			+25°C		+0.01 typical		
V_{EX} input pull up current	I_{PU}	$V_{EX} = 0 V$	-55°C to +125°C	01	-10		µA
			+25°C		-3 typical		
Tristate leakage current per channel	I_{OZ}		-55°C to +125°C	01	-10	+10	µA
			+25°C		+0.01 typical		
Logic high input threshold	V_{IH}, V_{EH}		-55°C to +125°C	01	1.6		V
Logic low input threshold	V_{IL}, V_{EL}		-55°C to +125°C	01		0.4	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 3.3 V operation 9/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Logic high output voltages	V_{OAH}, V_{OBH}	I_{OX} = -20 µA, V_{IX} = V_{IXH} 4/ 5/	-55°C to +125°C	01	(V_{DD1} or V_{DD2}) – 0.1		V
			+25°C		3.3 typical		
	V_{OCH}, V_{ODH}	I_{OX} = -4 mA, V_{IX} = V_{IXH} 4/ 5/	-55°C to +125°C		(V_{DD1} or V_{DD2}) – 0.4		
			+25°C		2.8 typical		
Logic low output voltage	V_{OAL}, V_{OBL}	I_{OX} = 20 µA, V_{IX} = V_{IXL} 4/ 6/	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
	V_{OCL}, V_{ODL}	I_{OX} = 400 µA, V_{IX} = V_{IXL} 4/ 6/	-55°C to +125°C			0.1	
			+25°C		0.04 typical		
		I_{OX} = 4 mA, V_{IX} = V_{IXL} 4/ 6/	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Switching specifications							
Minimum pulse width	PW	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		100	ns
Maximum data rate		C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01	10		Mbps
Propagation delay	t_{PHL}, t_{PLH}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01	20	50	ns
			+25°C		38 typical		
Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		3	ns
Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$ change versus temperature		C_L = 15 pF, CMOS signal levels	+25°C	01	5 typical		ps/°C
Propagation delay skew	t_{PSK}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		22	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 3.3 V operation 9/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching specifications – continued.							
Channel to channel matching, codirectional channels	t_{PSKCD}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		3	ns
Channel to channel matching, opposing directional channels	t_{PSKOD}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		6	ns
Output propagation delay, disable (high/low to high impedance)	t_{PHZ}, t_{PLZ}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		8	ns
			+25°C		6 typical		
Output propagation delay, enable (high impedance to high/low)	t_{PZH}, t_{PZL}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		8	ns
			+25°C		6 typical		
Output rise/fall time (10% to 90%)	t_R / t_F	C_L = 15 pF, CMOS signal levels	+25°C	01	3 typical		ns
Common mode 7/ transient immunity logic high output	$\|CM_H\|$	$V_{IX} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/μs
			+25°C		35 typical		
Common mode 7/ transient immunity logic low output	$\|CM_L\|$	V_{IX} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/μs
			+25°C		35 typical		
Refresh rate	fr		+25°C	01	1.1 typical		Mbps
Dynamic supply current per channel, input	$I_{DDI(D)}$	8/	+25°C	01	0.10 typical		mA/ Mbps
Dynamic supply current per channel, output	$I_{DDO(D)}$	8/	+25°C	01	0.03 typical		mA/ Mbps

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5 V / 3.3 V or 3.3 V / 5 V operation 10/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications							
Input supply current per channel, quiescent	$I_{DDI (Q)}$	5 V / 3.3 V operation	-55°C to +125°C	01		0.83	mA
			+25°C		0.57 typical		
		3.3 V / 5 V operation	-55°C to +125°C			0.49	
			+25°C		0.31 typical		
Output supply current per channel, quiescent	$I_{DDO (Q)}$	5 V / 3.3 V operation	-55°C to +125°C	01		0.27	mA
			+25°C		0.29 typical		
		3.3 V / 5 V operation	-55°C to +125°C			0.35	
			+25°C		0.19 typical		
Total supply current	3/	DC to 2 Mbps					
V_{DD1} supply current	$I_{DD1(Q)}$	DC to 1 MHz logical signal frequency, 5 V / 3.3 V operation	-55°C to +125°C	01		3.2	mA
			+25°C		2.5 typical		
		DC to 1 MHz logical signal frequency, 3.3 V / 5 V operation	-55°C to +125°C			1.9	
			+25°C		1.4 typical		
V_{DD2} supply current	$I_{DD2(Q)}$	DC to 1 MHz logical signal frequency, 5 V / 3.3 V operation	-55°C to +125°C	01		1.5	mA
			+25°C		0.9 typical		
		DC to 1 MHz logical signal frequency, 3.3 V / 5 V operation	-55°C to +125°C			2.4	
			+25°C		1.6 typical		
Total supply current	3/	10 Mbps					
V_{DD1} supply current	$I_{DD1(10)}$	5 MHz logical signal frequency, 5 V / 3.3 V operation	-55°C to +125°C	01		10.6	mA
			+25°C		7.4 typical		
		5 MHz logical signal frequency, 3.3 V / 5 V operation	-55°C to +125°C			5.6	
			+25°C		4.1 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5 V / 3.3 V or 3.3 V / 5 V operation 10/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Total supply current	3/	10 Mbps					
V_{DD2} supply current	$I_{DD2(10)}$	5 MHz logical signal frequency, 5 V / 3.3 V operation	-55°C to +125°C	01		3.3	mA
			+25°C		2.5 typical		
		5 MHz logical signal frequency, 3.3 V / 5 V operation	-55°C to +125°C			6.5	
			+25°C		4.4 typical		
Input leakage per channel	I_I	$0 V \le V_{IX} \le V_{DDX}$	-55°C to +125°C	01	-10	+10	µA
			+25°C		+0.01 typical		
V_{EX} input pull up current	I_{PU}	V_{EX} = 0 V	-55°C to +125°C	01	-10		µA
			+25°C		-3 typical		
Tristate leakage current per channel	I_{OZ}		-55°C to +125°C	01	-10	+10	µA
			+25°C		+0.01 typical		
Logic high input threshold	V_{IH}, V_{EH}	5 V / 3.3 V operation	-55°C to +125°C	01	2.0		V
		3.3 V / 5 V operation			1.6		
Logic low input threshold	V_{IL}, V_{EL}	5 V / 3.3 V operation	-55°C to +125°C	01		0.8	V
		3.3 V / 5 V operation				0.4	
Logic high output voltages	V_{OAH}, V_{OBH}	I_{OX} = -20 µA, $V_{IX} = V_{IXH}$ 4/ 5/	-55°C to +125°C	01	(V_{DD1} or V_{DD2}) – 0.1		V
			+25°C		(V_{DD1} or V_{DD2}) typical		
	V_{OCH}, V_{ODH}	I_{OX} = -4 mA, $V_{IX} = V_{IXH}$ 4/ 5/	-55°C to +125°C		(V_{DD1} or V_{DD2}) – 0.4		
			+25°C		(V_{DD1} or V_{DD2}) – 0.2 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5 V / 3.3 V or 3.3 V / 5 V operation 10/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specifications – continued.							
Logic low output voltage	V_{OAL}, V_{OBL}	I_{OX} = 20 μA, V_{IX} = V_{IXL} 4/ 6/	-55°C to +125°C	01		0.1	V
			+25°C		0.0 typical		
	V_{OCL}, V_{ODL}	I_{OX} = 400 μA, V_{IX} = V_{IXL} 4/ 6/	-55°C to +125°C			0.1	
			+25°C		0.04 typical		
		I_{OX} = 4 mA, V_{IX} = V_{IXL} 4/ 6/	-55°C to +125°C			0.4	
			+25°C		0.2 typical		
Switching specifications							
Minimum pulse width	PW	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		100	ns
Maximum data rate		C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01	10		Mbps
Propagation delay	t_{PHL}, t_{PLH}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01	15	50	ns
			+25°C		35 typical		
Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		3	ns
Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$ change versus temperature		C_L = 15 pF, CMOS signal levels	+25°C	01	5 typical		ps/°C
Propagation delay skew	t_{PSK}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		22	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5 V / 3.3 V or 3.3 V / 5 V operation 10/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching specifications – continued.							
Channel to channel matching, codirectional channels	t_{PSKCD}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		3	ns
Channel to channel matching, opposing directional channels	t_{PSKOD}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		6	ns
Output propagation delay, disable (high/low to high impedance)	t_{PHZ}, t_{PLZ}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		8	ns
			+25°C		6 typical		
Output propagation delay, enable (high impedance to high/low)	t_{PZH}, t_{PZL}	C_L = 15 pF, CMOS signal levels	-55°C to +125°C	01		8	ns
			+25°C		6 typical		
Output rise/fall time (10% to 90%)	t_R / t_F	C_L = 15 pF, CMOS signal levels, 5 V / 3.3 V operation	+25°C	01	3 typical		ns
		C_L = 15 pF, CMOS signal levels, 3.3 V / 5 V operation			2.5 typical		
Common mode 7/ transient immunity logic high output	$\|CM_H\|$	$V_{IX} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/µs
			+25°C		35 typical		
Common mode 7/ transient immunity logic low output	$\|CM_L\|$	V_{IX} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V	-55°C to +125°C	01	25		kV/µs
			+25°C		35 typical		
Refresh rate	fr	5 V / 3.3 V operation	+25°C	01	1.2 typical		Mbps
		3.3 V / 5 V operation			1.1 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 5 V / 3.3 V or 3.3 V / 5 V operation 10/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic supply current per channel, input	$I_{DDI(D)}$	5 V / 3.3 V operation 8/	+25°C	01	0.20 typical		mA/ Mbps
		3.3 V / 5 V operation 8/			0.10 typical		
Dynamic supply current per channel, output	$I_{DDO(D)}$	5 V / 3.3 V operation 8/	+25°C	01	0.03 typical		mA/ Mbps
		3.3 V / 5 V operation 8/			0.05 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All voltages are relative to their respective ground. $4.5\ V \le V_{DD1} \le 5.5\ V$ and $4.5\ V \le V_{DD2} \le 5.5\ V$.
Unless otherwise specified, all minimum / maximum specifications apply over the entire recommended operation range.
All typical specifications are at $T_A = 25°C$, $V_{DD1} = V_{DD2} = 5\ V$.

3/ The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. See figures 6 through 8 for information on per channel supply current as a function of data rate for unloaded and loaded conditions. See figures 9 and 10 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for device channel configurations.

4/ I_{OX} is the channel X output current, where X = A, B, C, or D.

5/ V_{IXH} is the input side logic high.

6/ V_{IXL} is the input side logic low.

7/ CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining the $(V_{OUT}) > 0.8\ V_{DD2}$.
CM_L is the maximum common mode voltage slew rate that can be sustained while maintain $V_{OUT} < 0.8\ V$.
The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
The transient magnitude is the range over which the common mode is slewed.

8/ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate.
See figures 6 through 8 for information on per channel supply current for unloaded and loaded conditions.

9/ All voltages are relative to their respective ground. $3.135\ V \le V_{DD1} \le 3.6\ V$ and $3.135\ V \le V_{DD2} \le 3.6\ V$.
Unless otherwise specified, all minimum / maximum specifications apply over the entire recommended operation range.
All typical specifications are at $T_A = 25°C$, $V_{DD1} = V_{DD2} = 3.3\ V$.

10/ All voltages are relative to their respective ground. For 5 V / 3.3 V operation, $4.5\ V \le V_{DD1} \le 5.5\ V$ and $3.135\ V \le V_{DD2} \le 3.6\ V$, and for 3.3 V / 5 V operation, $3.135\ V \le V_{DD1} \le 3.6\ V$ and $4.5\ V \le V_{DD2} \le 5.5\ V$.
Unless otherwise specified, all minimum / maximum specifications apply over the entire recommended operation range.
All typical specifications are at $T_A = 25°C$, $V_{DD1} = 3.3\ V$, $V_{DD2} = 5\ V$ or $V_{DD1} = 5\ V$, $V_{DD2} = 3.3\ V$.

Case X

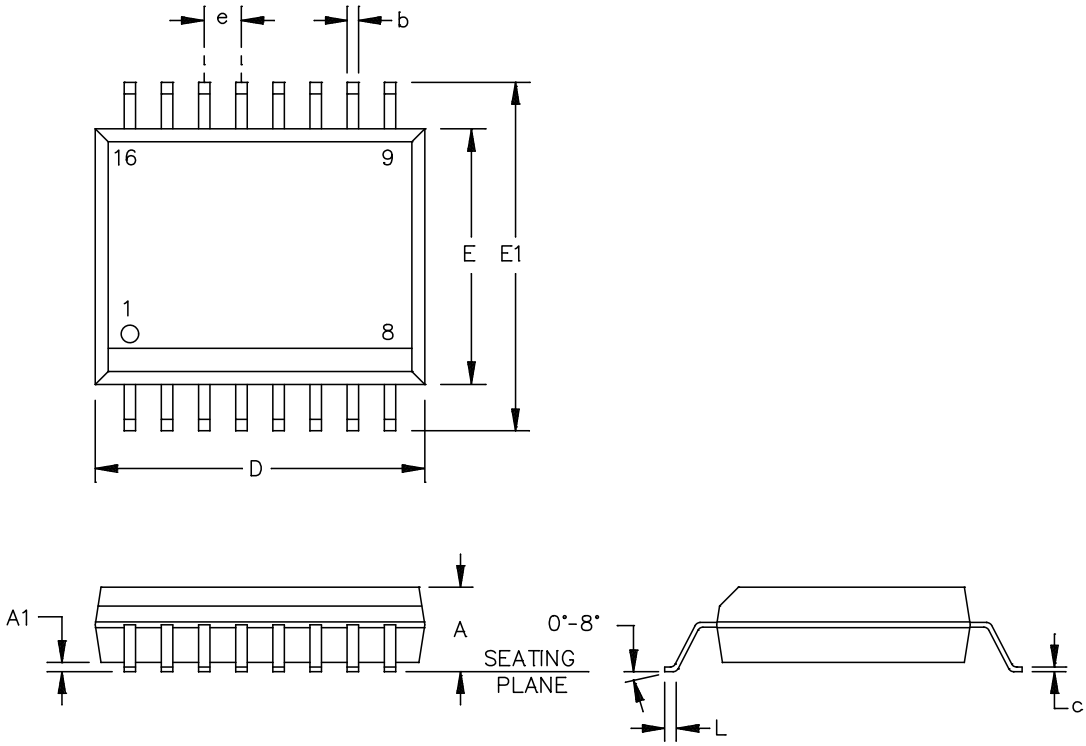

FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0925	0.1043	2.35	2.65
A1	0.0039	0.0118	0.10	0.30
b	0.0122	0.0201	0.31	0.51
c	0.0079	0.0130	0.20	0.33
D	0.3976	0.4134	10.10	10.50
E	0.2913	0.2992	7.40	7.60
E1	0.3937	0.4193	10.00	10.65
e	0.0500 BSC		1.27 BSC	
L	0.0157	0.0500	0.40	1.27
n		16		16

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within JEDEC MS-013 variation AA.

FIGURE 1. Case outline.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{DD1}	Supply voltage for isolator side 1, 3.135 V to 5.5 V.
2	GND1	Ground 1. Ground reference for isolator side 1. See note 1
3	V_{IA}	Logic input A.
4	V_{IB}	Logic input B.
5	V_{IC}	Logic input C.
6	V_{OD}	Logic output D.
7	V_{E1}	Output enable 1. Active high logic input. V_{OD} output is enabled when V_{E1} is high or disconnected. V_{OD} output is disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
8	GND1	Ground 1. Ground reference for isolator side 1. See note 1.
9	GND2	Ground 2. Ground reference for isolator side 2.
10	V_{E2}	Output enable 2. Active high logic input. V_{OA}, V_{OB}, and V_{OC} outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, and V_{OC} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{ID}	Logic input D.
12	V_{OC}	Logic output C.
13	V_{OB}	Logic output B.
14	V_{OA}	Logic output A.
15	GND2	Ground 2. Ground reference for isolator side 2.
16	V_{DD2}	Supply voltage for isolator side 2, 3.135 V to 5.5 V.

NOTE:
1. Both GND1 pins are internally connected and connecting both to GND1 is recommended.
   Both GND2 pins are internally connected and connecting both to GND2 is recommended.
   In noisy environments, connecting output enables (V_{E1} and V_{E2}) to an external logic high or low is recommended.

FIGURE 2. Terminal connections.

Positive logic

V_{IX} input	V_{EX} input	V_{DDI} state	V_{DDO} state	V_{OX} output	Notes
H	H or NC	Powered	Powered	H	
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	Outputs return to the input state within 1 μs of V_{DDI} power restoration.
X	L	Unpowered	Powered	Z	
X	X	Powered	Unpowered	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration if V_{EX} state is H or NC. Outputs return to high impedance state within 8 ns of V_{DDO} power restoration if V_{EX} state is L.

1/ V_{IX} and V_{OX} refer to the input and output signals of a given channel (A, B, C, or D). V_{EX} refers to the output enable signal on the same side as the V_{OX} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

2/ H is high, L is low, X is don't care, and NC is no connect.

3/ In noisy environments, connecting V_{EX} to an external logic high or low is recommended.

FIGURE 3. Truth table.

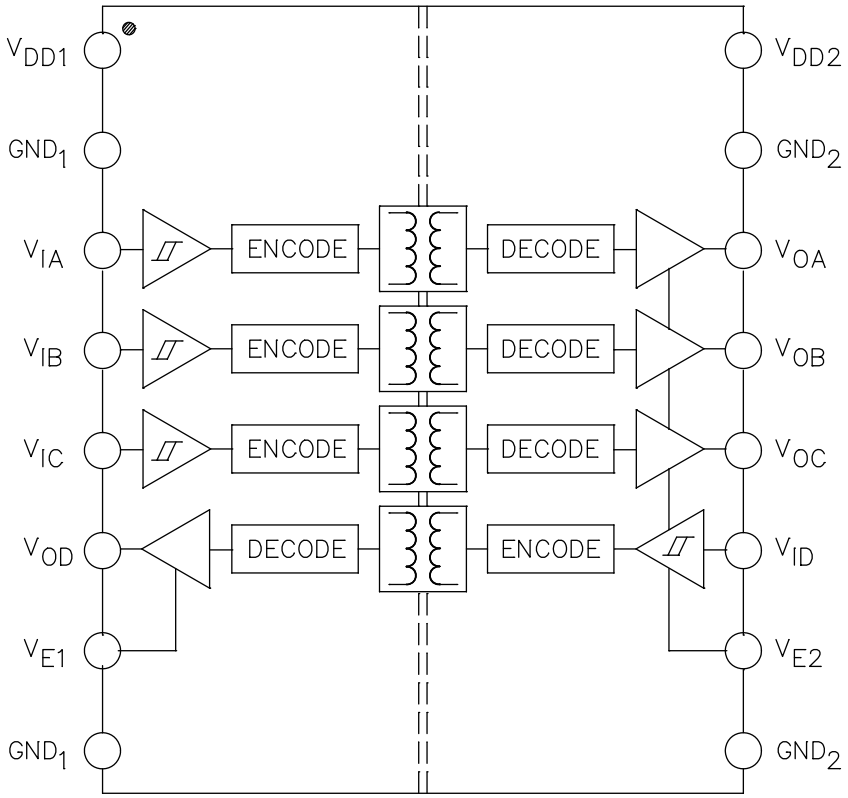

FIGURE 4. Logic diagram.

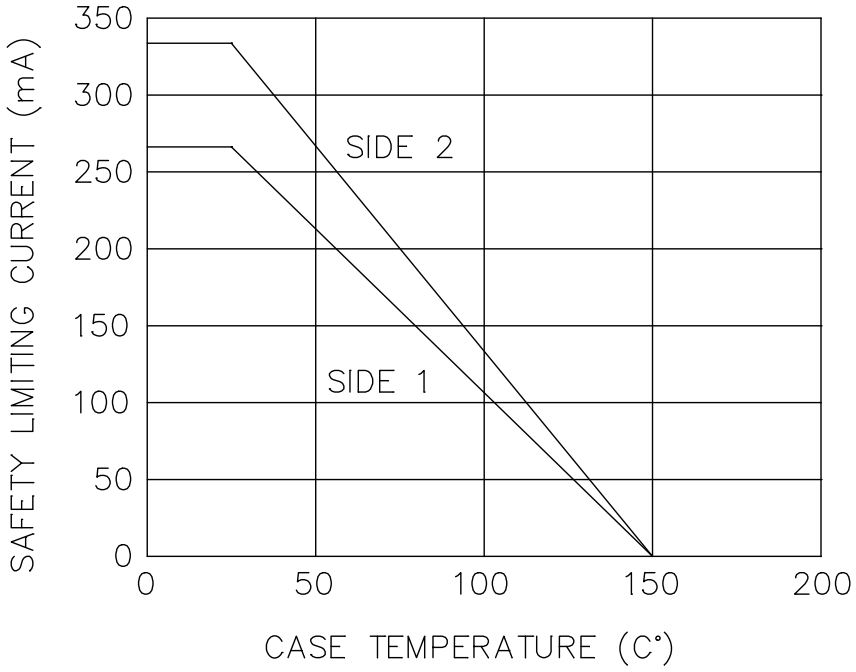

FIGURE 5. Thermal derating curve.

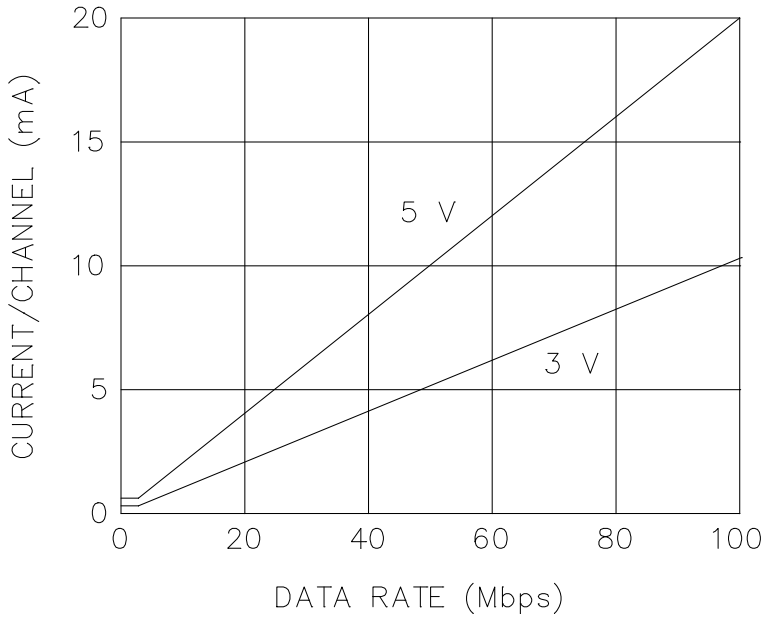

FIGURE 6. Typical input supply current per channel versus data rate (no load).

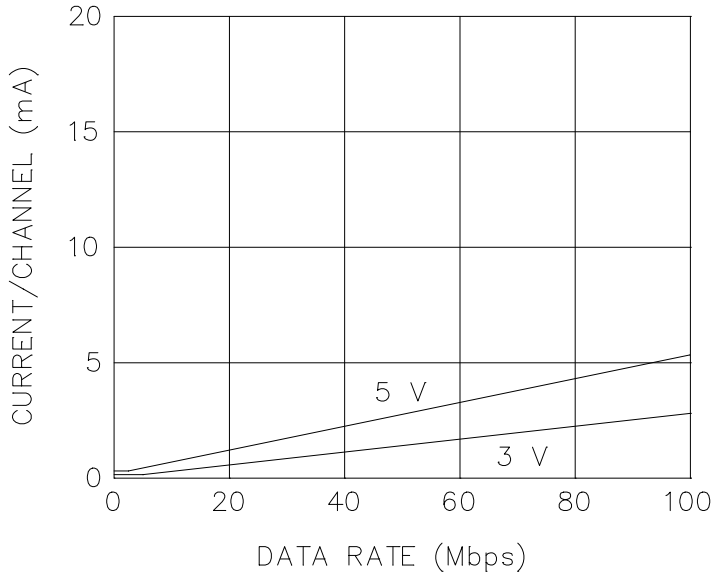

FIGURE 7. Typical output supply current per channel versus data rate (no load).

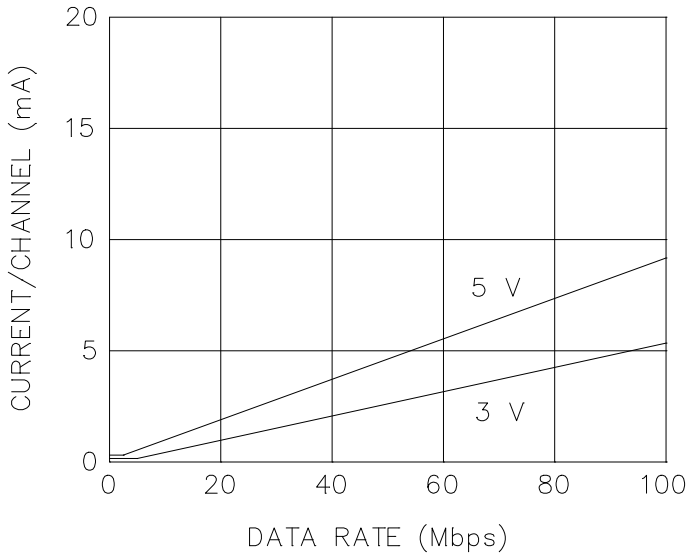

FIGURE 8. Typical output supply current per channel versus data rate (15 pF output load).

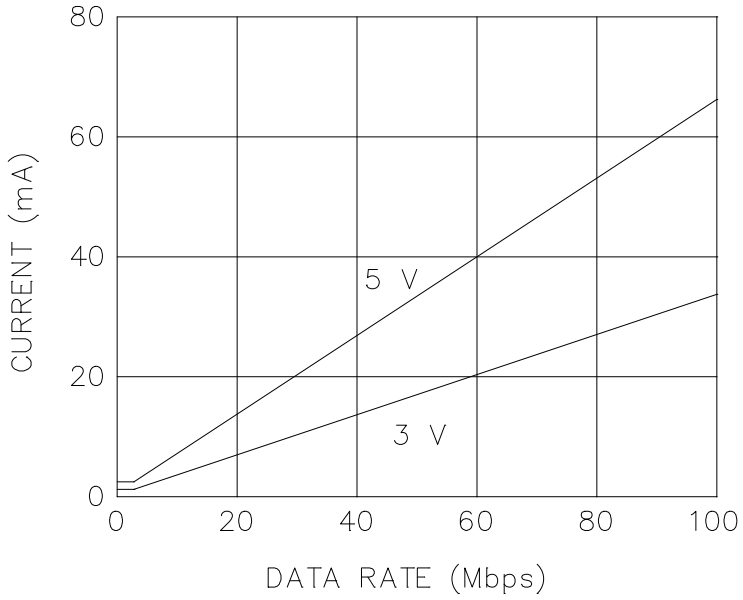

FIGURE 9. Typical VDD1 supply current versus data rate for 5 V and 3.3 V operation.

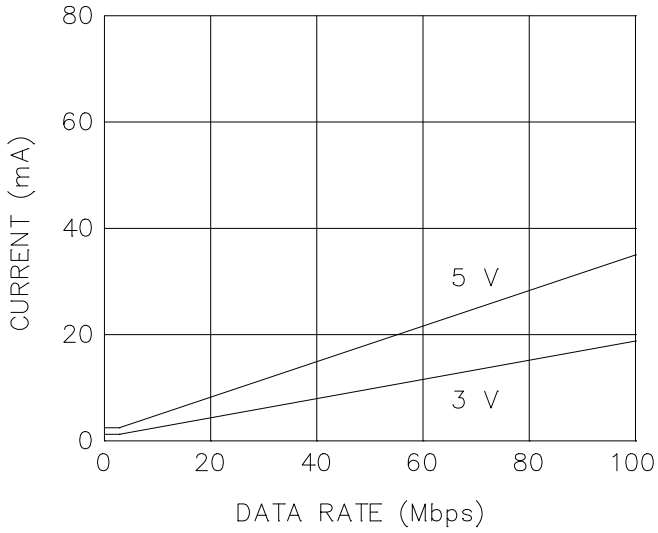

FIGURE 10. Typical VDD2 supply current versus data rate for 5 V and 3.3 V operation.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/14630-01XE	24355	ADUM3401TRWZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland