Automotive Grade

International
IOR Rectifier

AUIR0815S

BUFFER GATE DRIVER IC

Features

- High peak output current > 10A
- Low propagation delay time
- Negative turn off bias can be applied to V_{EE} using an external supply
- Two output pins permit to choose different Ron and Roff resistors.
- Low supply current
- Undervoltage lockout
- Continuous 'on' capability
- Suitable for high power inverter applications in conjunction with an external pre-driver
- Lead-Free, RoHS Compliant
- Automotive qualified

Description

The AUIR0815 buffer gate driver family, in conjunction with a pre-driver stage, is suited to drive a single half bridge in power switching applications. These buffer gate drivers incorporate the ability to enter into a low quiescent current mode.

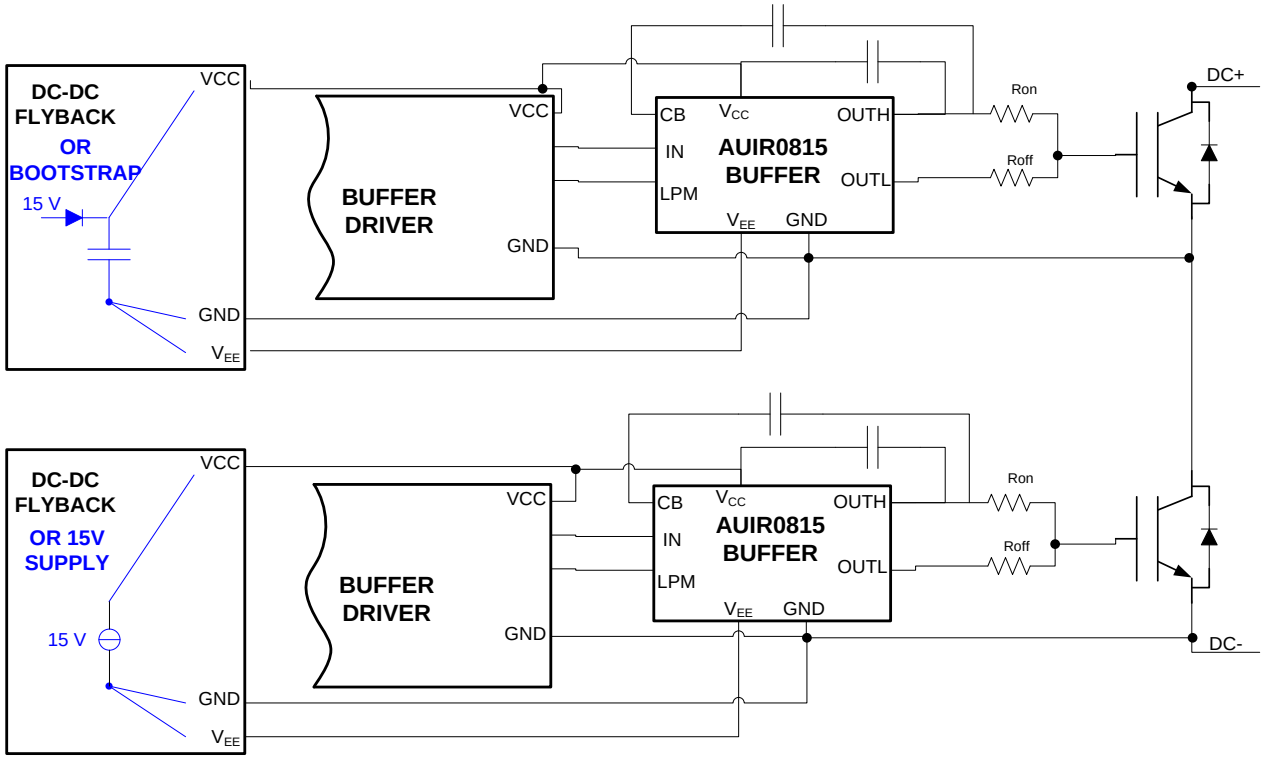
Product Summary

V_{CC} -GND	10V to 30V
GND -V_{EE}	-1V to 20V
Vcc- V_{EE}	10V to 30V
$I_{O\ drive}$	> 10A

Package

8 Pin SOIC

Typical connection



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Qualification Information†

Qualification Level		Automotive (per AEC-Q100††)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8N	MSL2††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M1 (Pass +/-100 V) (per AEC-Q100-003)	
	Human Body Model	Class H1B (+/-1000V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Exceptions to AEC-Q100 requirements, if any, are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package type listed here. Please contact your International Rectifier sales representative for further information.

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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which permanent damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Condition" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to GND unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
GND	to Vcc	-37	0.3	V
V_{EE}	To Vcc	-37	0.3	V
V_{IN}	Logic input voltage to Vcc	- 40	0.3	V
VB	Vbootstrap to OUTPUT	-0.3	5.5	V
LPM	LPM voltage to Vcc	- 40	0.3(*)	V
V_{OUTH}	OUTH Output voltage	Vcc-37	V_{CC} + 0.3	V
V_{OUTL}	OUTL output voltage	V_{EE}-0.2	V_{CC} + 0.3	V
P_D	Package power dissipation @ $T_A \leq 25$ °C	—	1	W
Rth_{JA}	Thermal resistance, junction to ambient	—	80	°C/W
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	°C
T_L	Lead temperature (soldering, 10 seconds)	—	300	°C

(*) LPM is allowed to settle to an higher voltage than specified providing a current limitation of 10uA

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND unless otherwise stated in the table

Symbol	Definition	Min.	Max.	Units
V_{CC-GND}	Gate driver positive supply voltage	6(*)	30	V
GND- V_{EE}	Gate driver negative supply voltage. V_{EE} is Shorted to GND in case of single supply operation	-1	15	
Vcc- V_{EE}	Total supply voltage	10	30	
V_{OUTH}	OUTH Output voltage	Vcc-30	Vcc	
V_{OUTH} - V_{EE}	Voltage difference between OUTH and V_{EE}	-5	—	
V_{IN}	Logic input voltage (IN and LPM)	Vcc-35	V_{CC}	
Cboot	OUTPUT pull up boot capacitor	10	20	nF
Ron	OUTH series resistor to gate	1.5	20	Ohm
Roff	OUTL series resistor to gate	1.5	20	Ohm
Cs	Snubber capacitor between OUTH and VCC	10	24	nF
PWoff	IN 'low' pulse width (**)	2		usec

(*)When 3V< V_{CC-GND} < V_{CC-GND_MIN} 30 Ohm max resistance pulls down OUTL to V_{EE} while OUTH is in HiZ. Guaranteed by design.

(**) V_{CC}-V_{EE}<12V, see also "Role of Cboot and Effect of Short 'Off' Pulses" chapter.

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Static Electrical Characteristics

V_{CC} -GND= 15V; GND-V_{EE} =5V; 15nF connects CB to OUTH; 22nF connects Vcc to OUTH ;-40 °C < T_A < 125 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	V_{CC}-GND supply undervoltage positive going threshold	10.2	11.7	12.8	V	LPM=HIN=1=VCC VE=GND; OUTH pulled to V_{CC}-2V with 100mA current limitation
V_{CCUV-}	V_{CC}-GND supply undervoltage negative going threshold	9.6	10.5	11.4		
V_{CCUVH}	V_{CC}-GND supply undervoltage lockout hysteresis	0.5	1.2	—		
VB_{UV}	Vbootstrap undervoltage (*)	—	4	—	V	
I_{QGG}	GND supply current	—	—	60	uA	IN=X; LPM=X
I_{QEESW}	V_{EE} supply current, IN switching	2	4	10	mA	IN switches at 10kHz 50% duty cycle; LPM=1
I_{QEE0}	V_{EE} supply current, IN=0	—	—	8.0	mA	steady state with IN=0 and LPM=1
I_{QEE025}	V_{EE} supply current, IN=0	—	—	6.5	mA	steady state with IN=0 and LPM=1 , T=25^C
I_{QEE1}	V_{EE} supply current, IN=1	—	—	3	mA	steady state with IN=1 and LPM=1
I_{QEELQ0}	V_{EE} supply current, LPM=0, IN=0	—	—	2	mA	steady state with IN=0 and LPM=0
I_{QEELQ1}	V_{EE} supply current, LPM=0, IN=1	—	—	1.5	mA	steady state with IN=1 and LPM=0
I_{QEEUV}	V_{EE} supply current, V_{CC}<V_{CCUV-}	—	—	1.8	mA	steady state with IN=X, LPM=X, V_{CC}<V_{CCUV-}
I_{QOUTL1}	Current flowing into OUTL	—	—	1.5	uA	IN=1; LPM=1 ; OUTL-GND=15V; OUTH disconnected
I_{QB}	Current into CB pin	—	—	1	mA	IN=1; LPM=1 ;CB-OUTH=5V
I_{QOUTH0}	Current flowing out from OUTH	—	—	3.5	mA	steady state with IN=0 and LPM=1, V(OUTH)=V_{EE}, OUTL disconnected
I_{BOUTH}	Current flowing out from CB, bootstrap discharged	—	20	40	mA	steady state, CB shorted to OUTH, IN=0 and LPM=1, V(OUTH)=V_{EE}, OUTL disconnected
I_{OUTH+}	OUTH high short circuit pulsed current	10	—	—	A	10A current pulse with PW<10usec
I_{OUTL-}	OUTL low short circuit pulsed current	10	—	—	A	

(*)When CB-OUTH< VB_{UV} the power nmos pulling up OUTH is turned off. The high level on OUTH is kept by a parallel PMOS (see also block diagram).

Pins: IN, LPM

V_{CC} -GND= 15V; GND-V_{EE} =5V; 15nF connects CB to OUTH; 22nF connects Vcc to OUTH; -40 °C < T_A < 125 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{INH\ vcc}$	Logic "1" IN input voltage to V_{CC}	-3.5	-2.5	-1.0	V	V_{CC}-GND> V_{CCUV-}
$V_{INL\ vcc}$	Logic "0" IN input voltage to V_{CC}	-5.5	-4.5	-3.5		
V_{INhis}	Logic IN input hysteresis	1	2	3.3		
$V_{LPMH\ vcc}$	Logic "1" LPM input voltage to V_{CC}	-3	-2.5	-1.4	V	V_{CC}-GND> V_{CCUV-}
$V_{LPML\ vcc}$	Logic "0" LPM input voltage to V_{CC}	-3.8	-3	-2.5		
V_{LPMhis}	Logic LPM input hysteresis	0.25	-	1.8		
I_{IN15}	Current flowing out from IN when V_{CC}-IN=15V	40	90	180	uA	IN=GND
I_{LPM15}	Current flowing out from LPM V_{CC}-LPM=15V	10	25	50	uA	LPM=GND

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Pins: OUTH,OUTL

V_{CC} -GND= 15V; GND-V_{EE} =5V; 15nF connects CB to OUTH; 22nF connects Vcc to OUTH; -40 °C < T_A < 125 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Rup_OUTH25	Rdson pull up transistor OUTH	—	90	120	mOhm	10A current pulse with PW<10usec T_A=25^C
Rdw_OUTL25	Rdson pull down transistor OUTL	—	180	240		
Rup_OUTH	Rdson pull up transistor OUTH	—	—	180		10A current pulse with PW<10usec
Rdw_OUTL	Rdson pull down transistor OUTL	—	—	320		
I_{PMOS}	OUTH Pull up current when bootstrap cap is discharged	5	20	30	mA	IN=1 LPM=1, CB-OUTH=2.5V, OUTH pulled to VCC-1.5V

AC Electrical Characteristics

V_{CC} -GND= 15V; GND-V_{EE} =5V; 15nF connects CB to OUTH; 22nF connects Vcc to OUTH ;Ron= 5 Ohm , Roff = 5 Ohm , C_{LOAD}=100nF , -40 °C < T_A < 125 °C unless otherwise specified.
Propagation is from INPUT at GND or V_{CC} to 10% voltage variation of output
RISE FALL TIME is delay from 10% to 90% output swing

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn on propagation delay IN-OUTH	—	250	400	ns	
t_{off}	Turn off propagation delay IN-OUTL	—	250	350		
t_r	Turn on rise time OUTH	—	—	260		
t_f	Turn off fall time OUTL	—	—	150		
t_{rLQ}	Turn on rise time OUTH in Low Quiescent Currrent Mode	—	—	1000	ns	V_{EE}=GND, LPM=0, V_{CC} rises above V_{CCUV+}; C_{LOAD}=100nF Ron= 5 Ohm, Roff = 5 Ohm
t_{fLQ}	Turn off fall time OUTL in Low Quiescent Currrent Mode	—	—	1000	ns	V_{EE}=GND, LPM=0, V_{CC} falls below V_{CCUV-+}; C_{LOAD}=100nF Ron= 5 Ohm, Roff = 5 Ohm
PW_{ON}	IN high pulse width (*)	500	—	—	ns	No C_{LOAD}, -40 °C < T_A < 125 °C
PW_{OFF}	IN low pulse width (*)	500	—	—	ns	No C_{LOAD}, -40 °C < T_A < 125 °C

(*) IN pulse width lower than PW_{ONMIN} (PW_{OFFMIN}) min can be filtered

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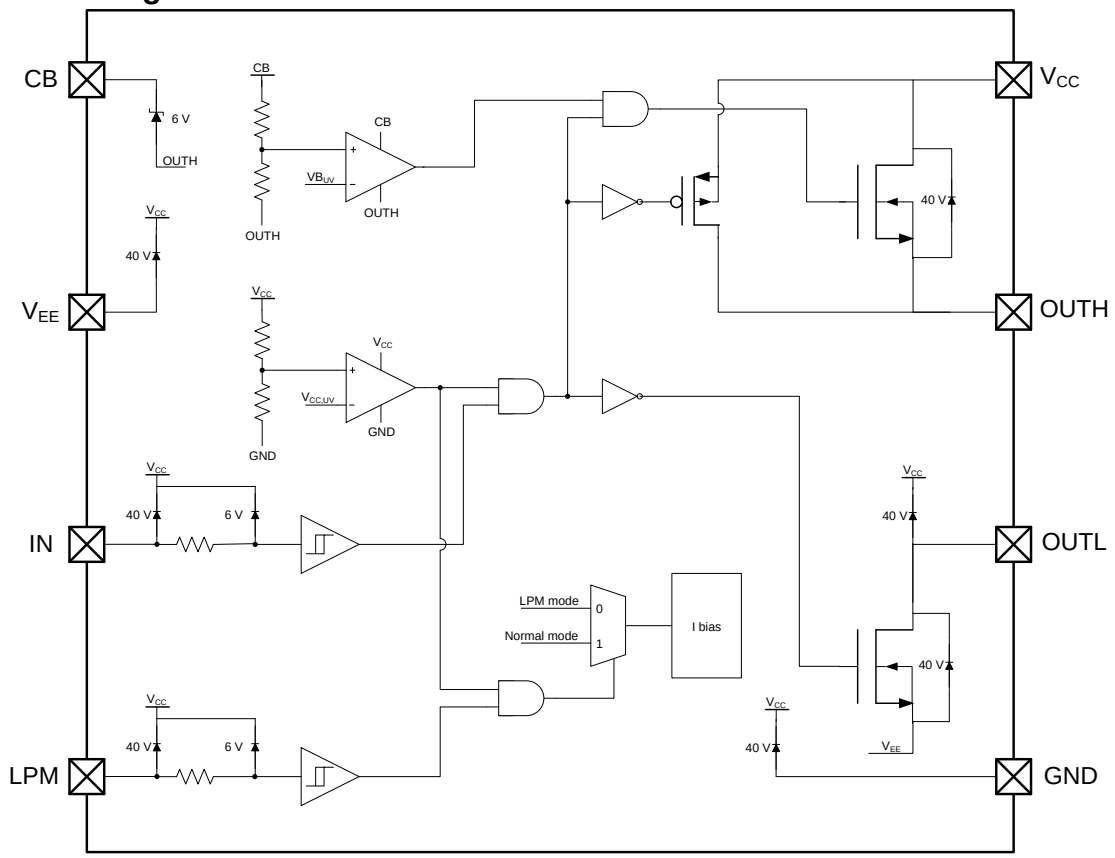
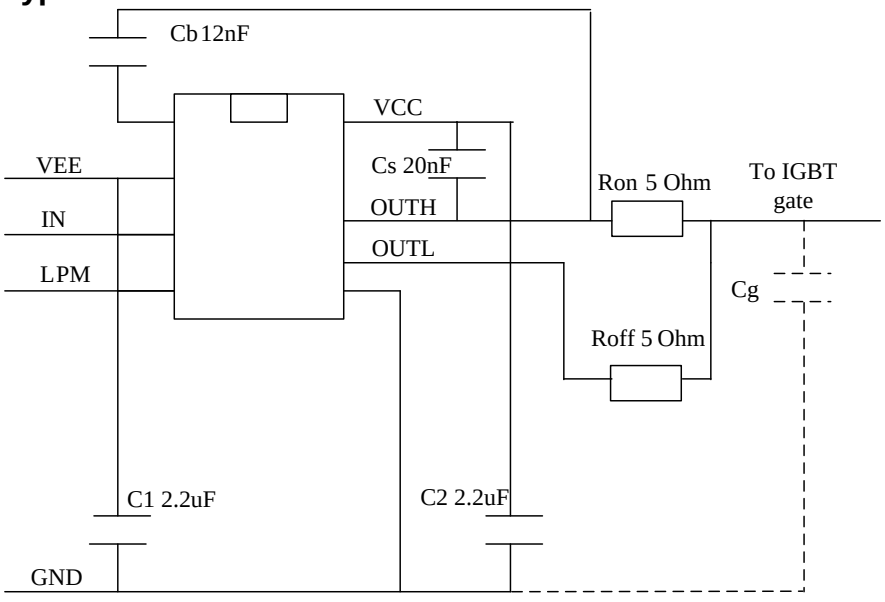
Block Diagram:



Typical connection



It is recommended:

- to have a capacitance Cs connected between OUTH and VCC to limit dv/dt in OUTH node (mandatory if Vcc-Vee>15V). See Recommended Operating Condition for Cs value.
- to avoid the condition with OUTH directly shorted to OUTL
- Use ceramic capacitor for C1 and C2 with value > 20* Cgate

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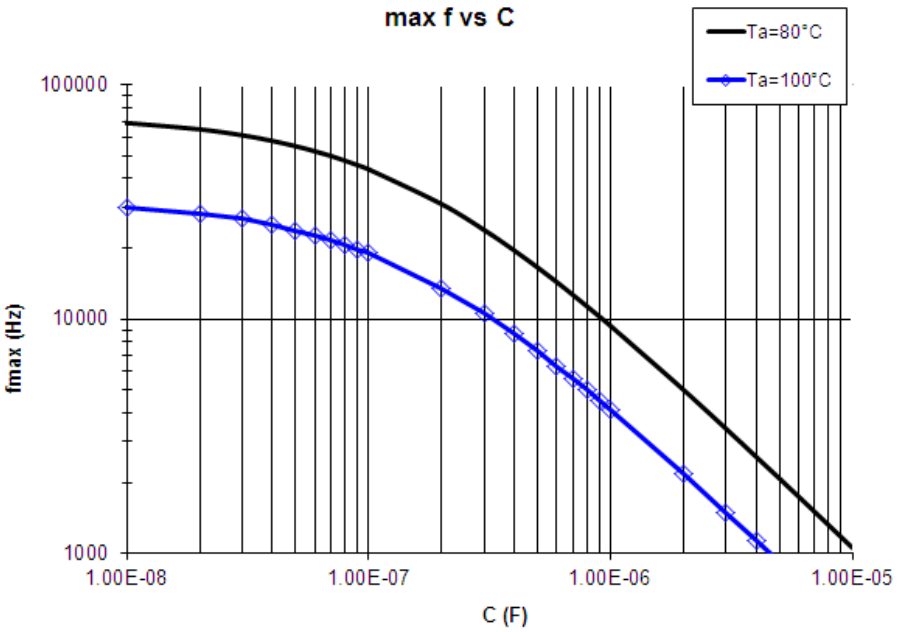
Application Information And Additional Details



Recommended maximum switching frequency when driving a capacitance C with a 3 Ohm external resistor.
Cs=20nF is connected between OUTH and Vcc.
Vcc-V_{EE}=24V.

Truth Table

Vcc	IN	LPM	Status/Comment
V_{CC-GND_MIN} to V_{CCUV}	-	-	OUTL = V_{EE}, OUTH in HiZ → IGBT OFF; Low Quiescent Current Mode is active.
V_{CCUV} to 30V	0	1	OUTL = V_{EE}, OUTH in HiZ → IGBT OFF;
V_{CCUV} to 30V	1	1	OUTL in HiZ, OUTH = Vcc → IGBT ON;
V_{CCUV} to 30V	0	0	OUTL = V_{EE}, OUTH in HiZ → IGBT OFF; Low Quiescent Current Mode is active
V_{CCUV} to 30V	1	0	OUTL in HiZ, OUTH = Vcc → IGBT ON; Low Quiescent Current Mode is active

Role of Cboot and Effect of Short 'Off' Pulses

Cboot capacitance, connected between OUTH and CB acts as a bootstrap supplying the circuitry driving the low rdson (R_{up_OUTH}) pull-up nmos connected between Vcc and OUTH.
In the application, when IN is low, OUTH is tied to VEE and Cboot is charged to around 6V.
At IN rising the pullup nmos is turned on and it is able to provide a low impedence path between VCC and OUTH.
Maintaining IN high, Cboot get discharged and therefore the pull-up nmos is turned off but the parallel pmos (see Block diagram) remains on maintaining OUTH tied to VCC.
Cboot discharge rate is I_{QB}/Cboot, typically it takes about 250 usec for a complete discharge.
In case Cboot get discharged, the subsequent off pulse width must be long enough to recharge Cboot above the bootstrap under-voltage threshold VB_{UV}. to allow the turn on of the pull-up nmos when IN rises again. Short Off pulse width can lead to a situation, after the pulse, with too low IGBT Vge voltage, worst case is for low values of V_{CC}-V_{EE}, that is just above V_{CCUV}-. Even though it is allowed, at higher values of Vcc-VEE, to reduce the off pulse width below PWoff min, it is suggested to keep the off pulse width above 1usec in every working condition.

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Examples of system schematics with HVIC

This section shows how IR High Voltage IC (HVIC) gate drivers can be used to drive the AUIR0815.

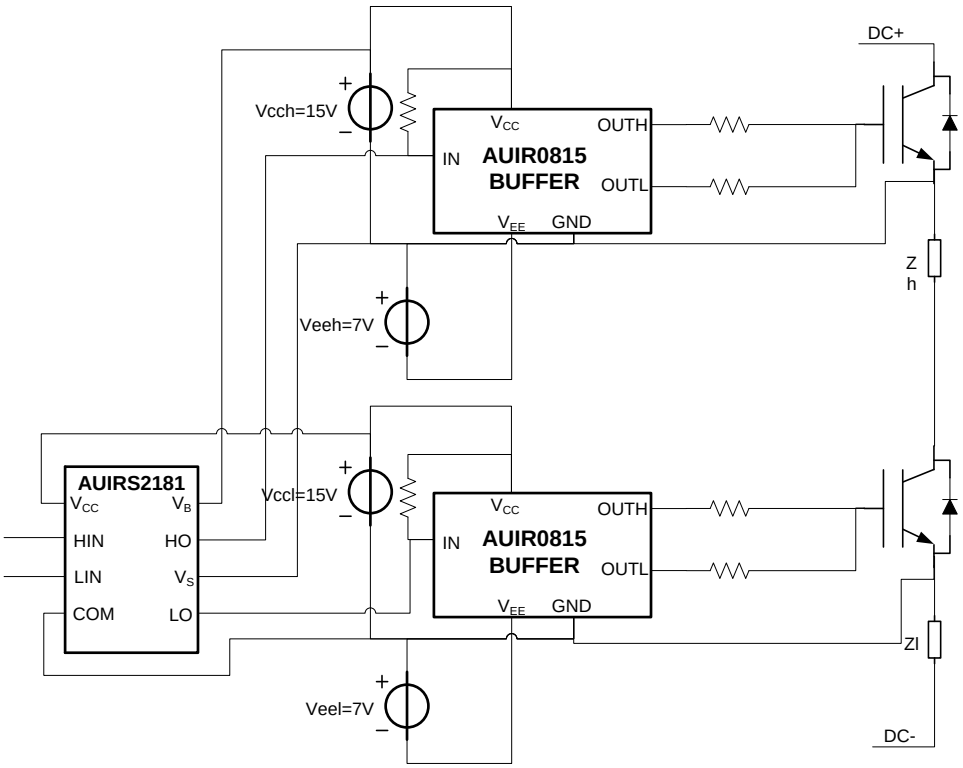
All the examples refer to an inverter leg, showing the floating voltage sources Vcch and Veeh to supply the high side AUIR0815 and Vccl and Veel to supply the low side AUIR0815.

All the examples show 7V floating voltage sources to provide a negative Vge to turn off each IGBT.
In case a negative Vge is not required these voltage sources can be replaced with a short circuit.

In case of three phase inverters, each of the high side AUIR0815 must have separated and isolated voltage supplies.
Only one DC power supply can be shared for the low sides AUIR0815 supplies (to be connected between AUIR0815 Vcc and GND pins) and the corresponding drivers supplies (to be connected between HVIC Vcc and Vss=COM) pins.

Normally high di/dt occurs at low side switch turn on. This causes voltage spikes at low side IGBT emitter node, because of the inductive impedance Zl, and the system must be robust to this.
A better immunity to the above transients can be obtained using one separate low side DC power supply for each low side.

Example 1: using the AUIRS2181, high and low side driver with COM and no VSS pin.



Example 1

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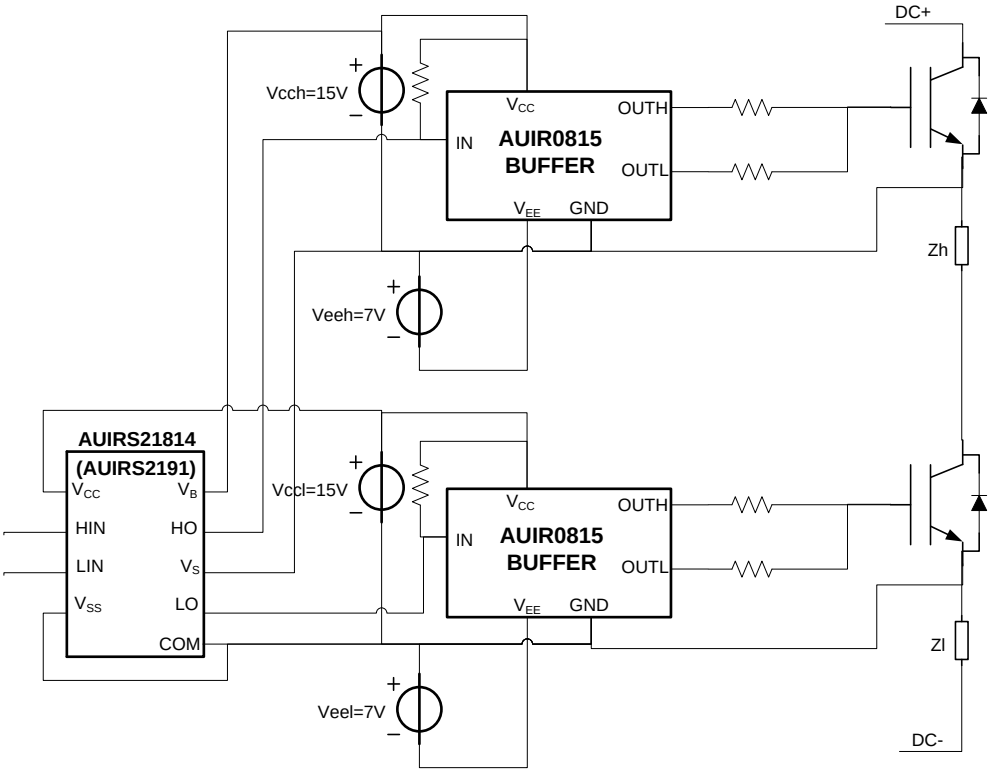
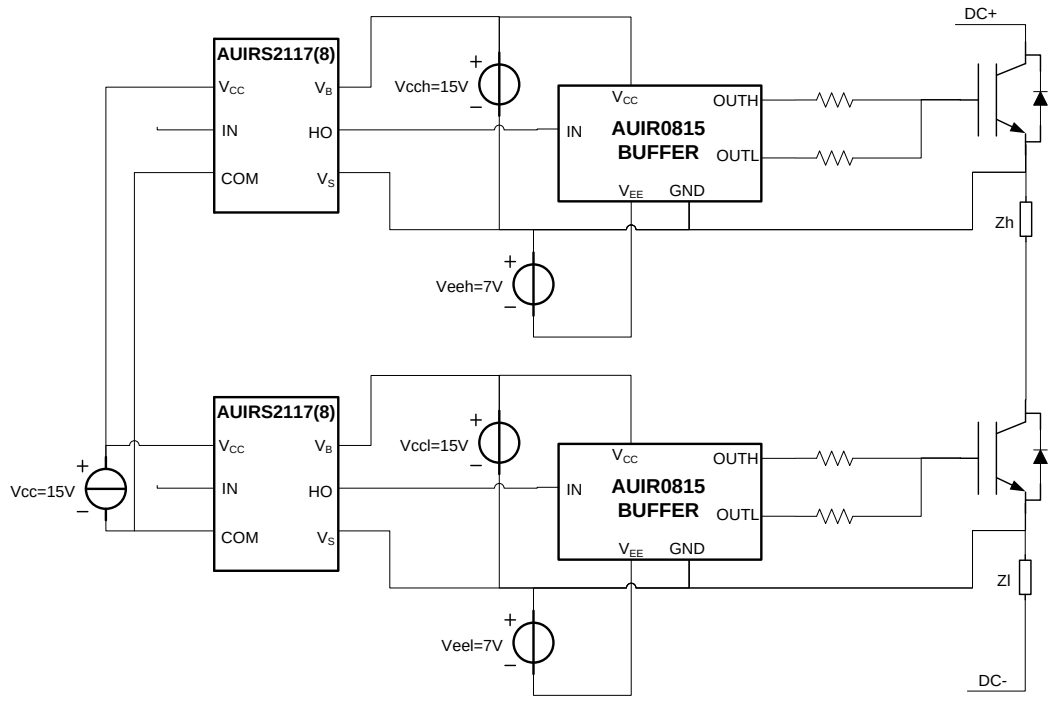
Example 2: using the AUIRS21814 (or the AUIRS2191), high and low side driver with COM pin and VSS pin.



Example 2

Example 3: using the AUIRS2117(8), single channel driver.
COM can be shorted to the Vs of the low side.



Example 3

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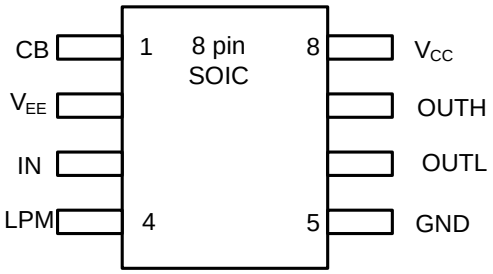
Lead Assignments



Lead Definitions

Symbol	Description
V_{CC}	Positive supply
IN	Logic input for OUT
LPM	Logic input, for Low Power Mode: LPM=0 activates the Low Quiescent Current Mode
GND	Ground
OUTH	Power Output (pull up)
OUTL	Power Output (pull down)
C_B	Boot capacitor
V_{EE}	Negative supply pin (short to GND in case of single supply operation)

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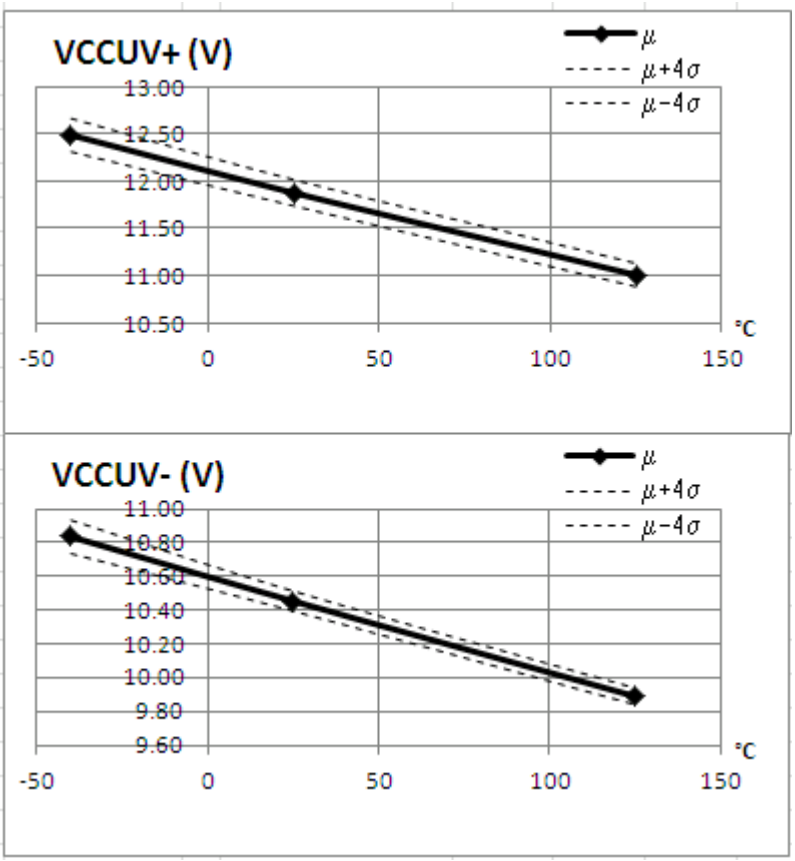
Parameter Temperature Trends

Figures illustrated in this chapter provide information on the experimental performance of the IC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).



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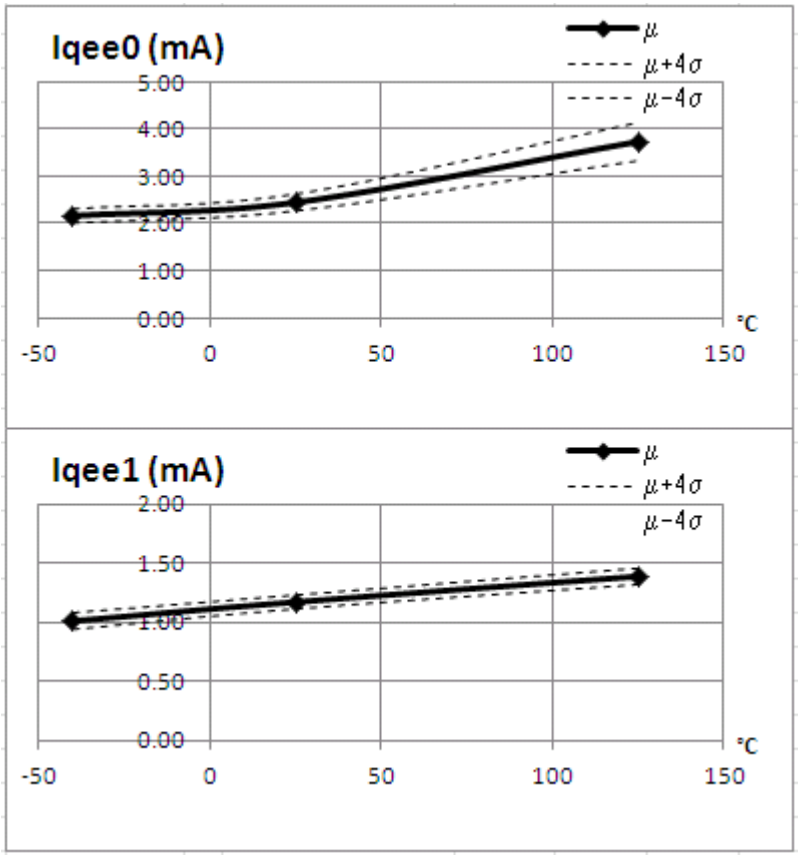

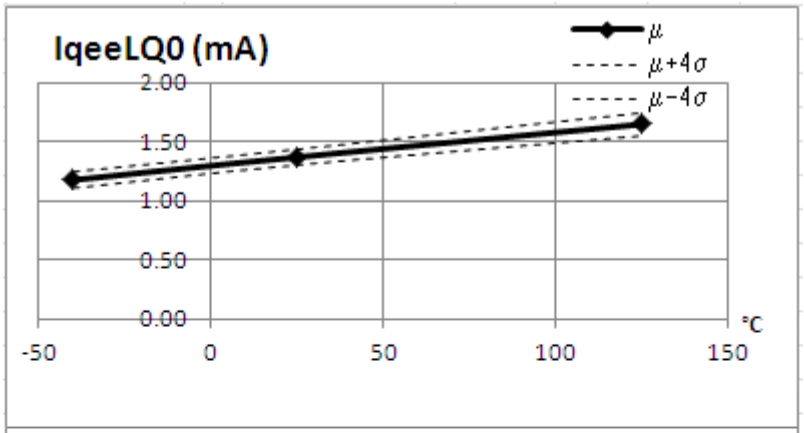

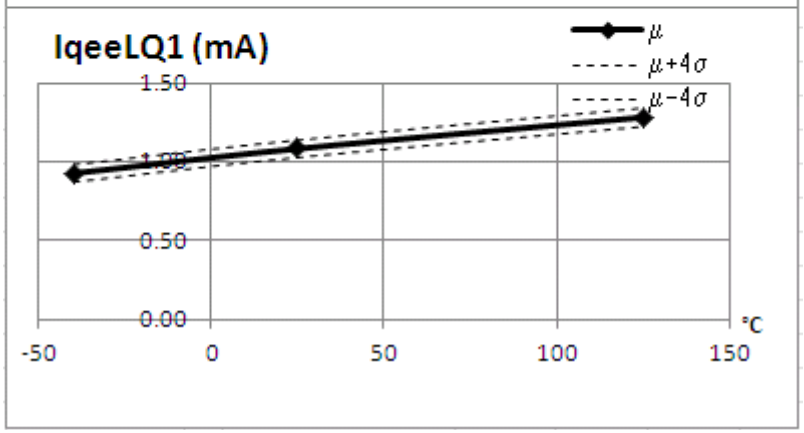

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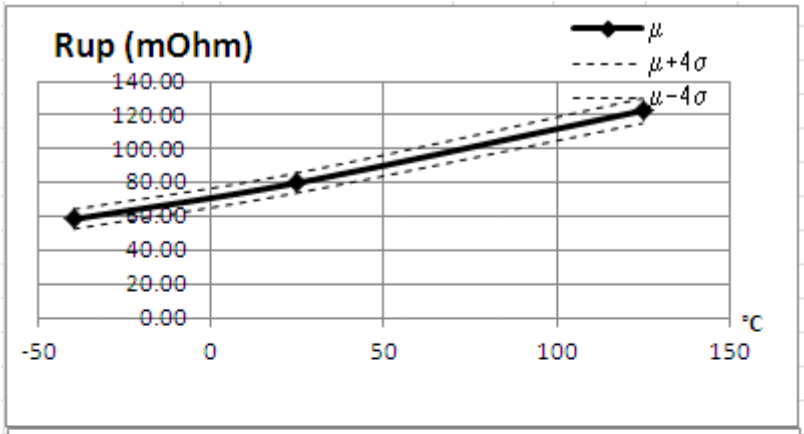

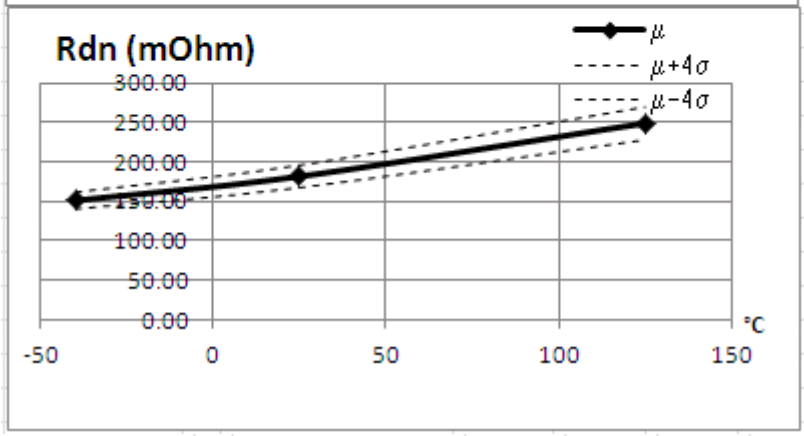

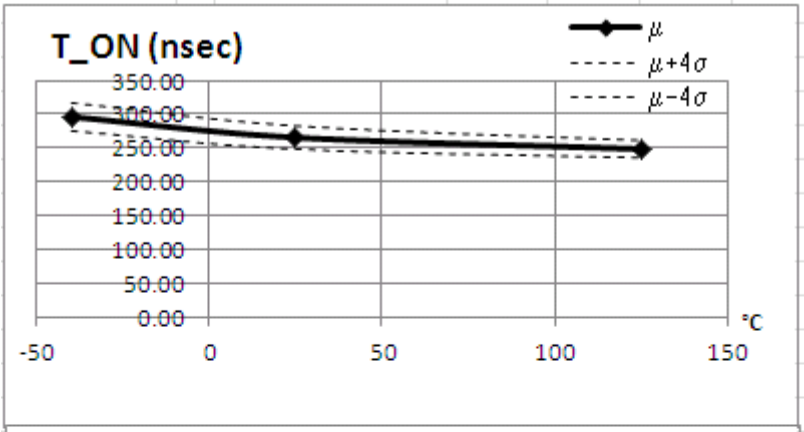

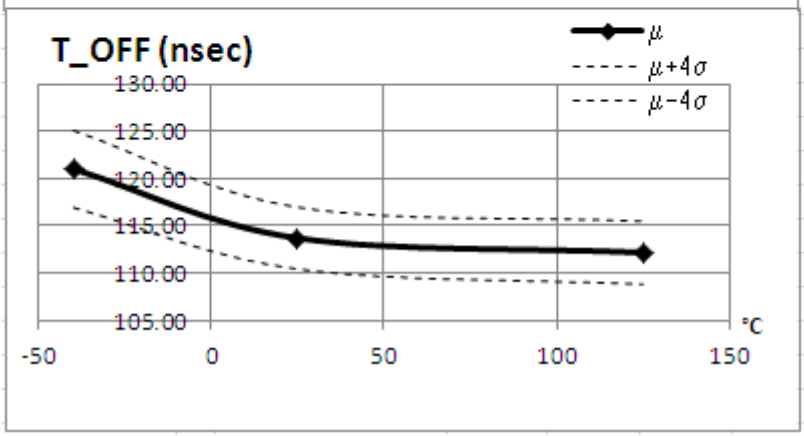

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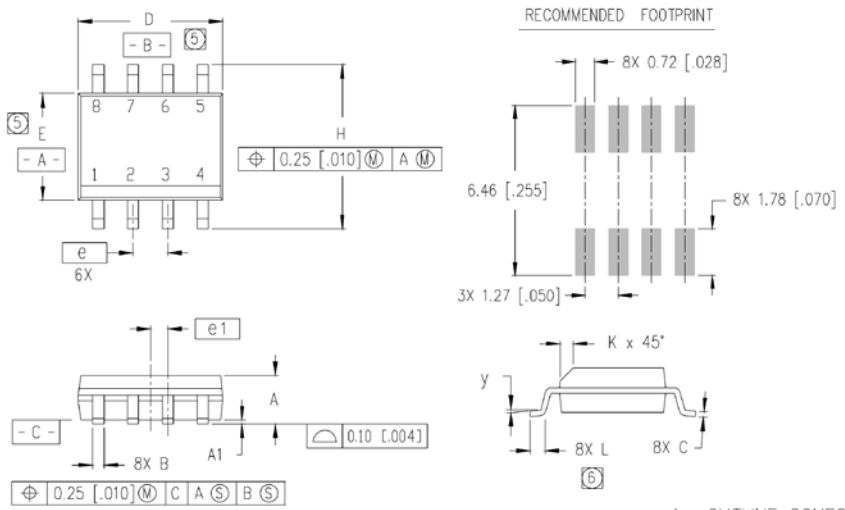
Case Outline



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

(6) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

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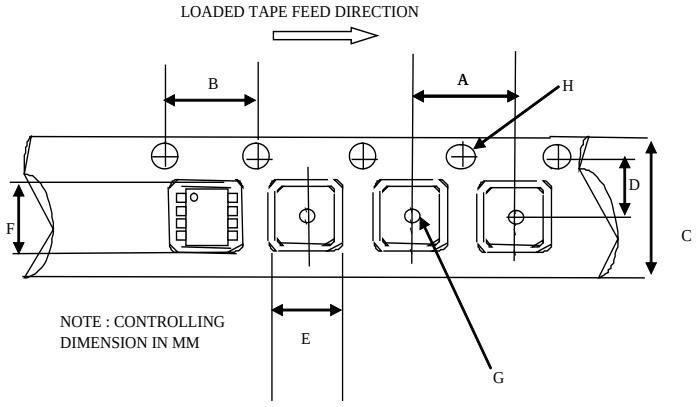
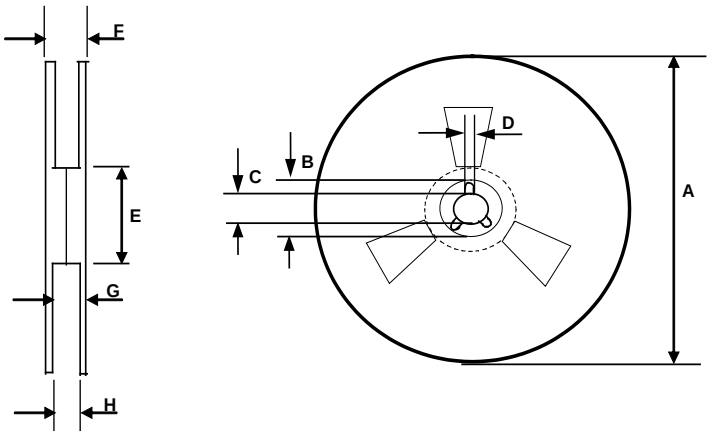
Tape and Reel: SOIC8



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

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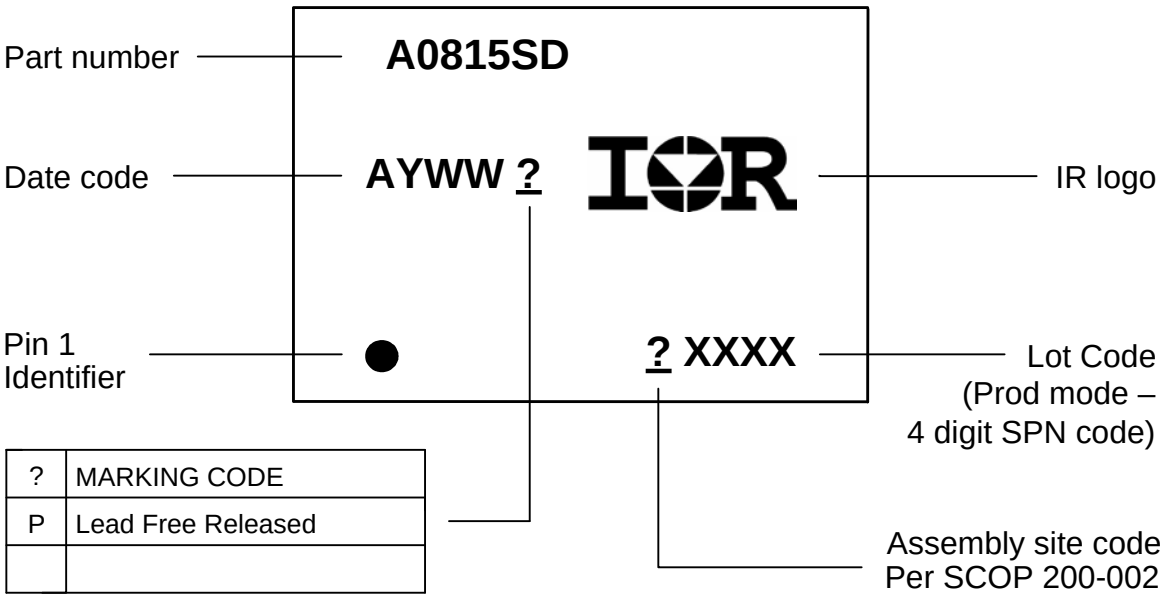
Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIR0815S	SOIC8	Tube/Bulk	95	AUIR0815S
		Tape and Reel	2500	AUIR0815STR

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Revision History

Date	Comment
Dec. 2, 2009	-V_E pin name changed into V_{EE}; note1 modified; VEE-VCC 40V diode added in block diagram; current consumption table parameters modified;
Feb 24, 2010	St. El. Ch: I_{QOUTL1} parameter added; I_{QOUTH0} max=2mA; I_{QB} max=0.5mA; I_{BOUTH}=60mA; I_{QEE0}max=6mA; I_{QEE1}max=3mA; I_{QB} definition corrected; I_{QEESW} value deleted; Rec. Op. Con.:Cboot=10nF..20nF AC El Char: Rise Fall time definition modified; Ssd= 100us typ
Feb 24b, 2010	Soft shutdown function removed (SSD_{IN}/EN pin renamed EN); Rup dc max value deleted; Typ connection; I_{QGG} and I_{QEEEN0}
Feb 25, 2010	$OUTL_{CLAMP}$ function added: changes in I_{QOUTL1}, I_{QEE1}; added Vcl, tcl1, tcl2
Apr 23, 2010	$OUTL_{CLAMP}$ function removed: I_{QOUTL1}=1uA typ, I_{QEE1}=3mA typ; Vcl, tcl1 and tcl2 removed. Change in EN pin functionality, now it is a low quiescent current mode input: front end page description; Abs Max Rat EN Max note added; Rec Op Cond: note added to specify pulldown 30 Ohm max for Vcc down to 3V. Static el char: change in EN and IN thresholds and Rin. I_{QEELQ} and I_{QEEUV} parameters introduced to specify consumption in Low Quiescent Current Mode (EN=1 or Vcc< Vcc_{UV-}). Truth Table modified to define V_{CCUV} and low quiescent current mode conditions Lead Definition modified to specify new EN function. AC Electr Char: Tr and Tf specified for Low Quiescent Current Mode.
May 15, 2010	EN pin renamed into LPM. Over temperature protection removed Block diagram: • Diode OUTL-Vcc added, • IN and LPM input stage detailed drawing added. Static El Char: • IN and LPM input impedance spec modified • note added to define VB_{UV}. • $I_{QEELEN0}$ parameter removed because already covered by I_{QEELQ}, • I_{QGG} Test Conditions changed from IN=0; LPM=1 into IN=X; LPM=X, • LPM input thresholds lowered by 1V • Rup renamed I_{PMOS}. Ac El Char: • t_{EN} parameter removed, • max values added for t_{on}, t_{off}, t_r, t_f. Rec. Op. Cond.: GND-VEE min changed from 0V to -1V.
Jun 25, 2010	I_{BOUTH}, I_{IN15}, parameters change; added PW_{ON} and PW_{OFF} parameters;
Mar 01, 2011	Update in test conditions for I_{OUTH+}, I_{OUTL}, Rup_OUTH, Rdw_OUTL. I_{QEELQ} split into I_{QEELQ0} and I_{QEELQ1} I_{BOUTH} redefined as current flowing out from CB (and not OUTH). Truth Table corrected to show how LPM does not affect the functionality. Update of heading for absolute maximum ratings Update of chart with max f vs C. Abs Max Rat: V_{OUTH} = Vcc-37V min; V_{OUTL} = V_{EE}-0.2V min. Rec Op Con: V_{OUTH} = Vcc-30V min; V_{OUTH} - V_{EE} = -5V min;
Mar 02, 2011	Static and dynamic el. Char: parameter limits reviewed for matching full temp range. Values in blue are still older datasheet version target value at T=25^C. Added recommendation to avoid direct short between OUTH and OUTL. Added preliminary parameter temperature trend paragraph. I_{PMOS} test condition corrected.
Jun 22, 2011	Vccuv thresholds modified; typ connection diagram: diode removed and snubber capacitance added; maxf vc C chart updated taking into account Cs=20nF as snubber capacitance
Jun 27, 2011	Matched delay outputs front page note deleted; Rec Op Cond Vcc-GND max changed from 20V to 30V. AC El Cher: tofftyp changed from 150ns to 250ns.Vccuv+ and Toff charts modified.
Aug 26, 2011	Added paragraph explaining role of Cboot. Cs snubber capacitor added in Recommended Operating Conditions and in default test set-up. V_{CCUV+}: Min from 10.6V to 10.2V ; V_{CCUV-}:Min from 9.7V to 9.6V ; V_{CCUVH}:Min from 0.8V to 0.5V ; I_{QEESW}: Max from 8mA to 10mA ; I_{QOUTH0}: Max from 3mA to 3.5mA ; $V_{INH\ vcc}$: Max from -1.5 V to -1V; $V_{LPMH\ vcc}$: Max from -2.5 V to -1.5V; V_{LPMhis}: Max from 1 V to 1.8V; I_{PMOS}: Min from 10mA to 5mA; t_{on}: Max from 380ns to 400ns; t_{off}: Max from 300ns to 350ns; t_r: Max from 150ns to 250ns;
Sep 6, 2011	Changes in typ connection recommandations; maxf vs C chart update; $V_{LPML\ vcc}$ Min Change from -3.5Vto -3.8V. Temperature charts updated.
Sept. 7, 2011	Corrected part number on header; added RoHS compliant & Automotive qualified to front page; deleted preliminary and added automotive grade on front page top header; added qual info page; added tape and reel info; added part marking; added ordering info; added important notice

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Oct 10, 2011	Rec Op Cond: Added description of Vouth and Vouth-Vee
Oct 17, 2011	Rec Op Cond: added " Guaranteed by design" in note under the table; Sta. El. Char. table: V_{CCUVH} Min changed from 0.5V to 0.3V. Pins: IN, LPM table: V_{INhis} Max changed from 3V to 3.3V; $V_{LPMH\ vcc}$ Max changed from -1.5V to -1.4V AC El Char table: t_r Max changed from 250ns to 260ns
Oct 19, 2011	Sta. El. Char. table: V_{CCUVH} Min changed back from 0.3V to 0.5V.
Oct 26, 2011	Revised MSL rating to MSL-2
Jan 20th, 2012	Application section added: Examples of system with HVIC
Jan 24th, 2012	"Examples of system schematics with HVIC" modified; block diagram updated.
October 24th 2012	Added Effect of Short 'Off' Pulses part in application info and minimum PWoff in recommended op cond. Front page typ connection, snubber cap added. Examples of system schematics with HVIC: added pullup resistors at IN in Ex1 and Ex2

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