AMBA Timer

Data Sheet

ARM®

ARM DDI 0049C

AMBA Timer
Data Sheet

Release Information

The following changes have been made to this book.

Change History

Date	Issue	Confidentiality	Change
December 1995	A	Non-Confidential	Created
January 1996	B	Non-Confidential	Minor edits
April 1997	C	Non-Confidential	Minor edits

Proprietary Notice

Confidentiality Status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

Product Status

The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

Contents
AMBA Timer Data Sheet

Chapter 1
AMBA Timer

This module contains two free-running counter/timers. It is connected to the *Advanced Peripheral Bus* (APB).

This chapter contains the following sections:

1.1 Overview

The Timer module connects to the Advanced Peripheral Bus. Figure 1-1 shows a block diagram of this module.

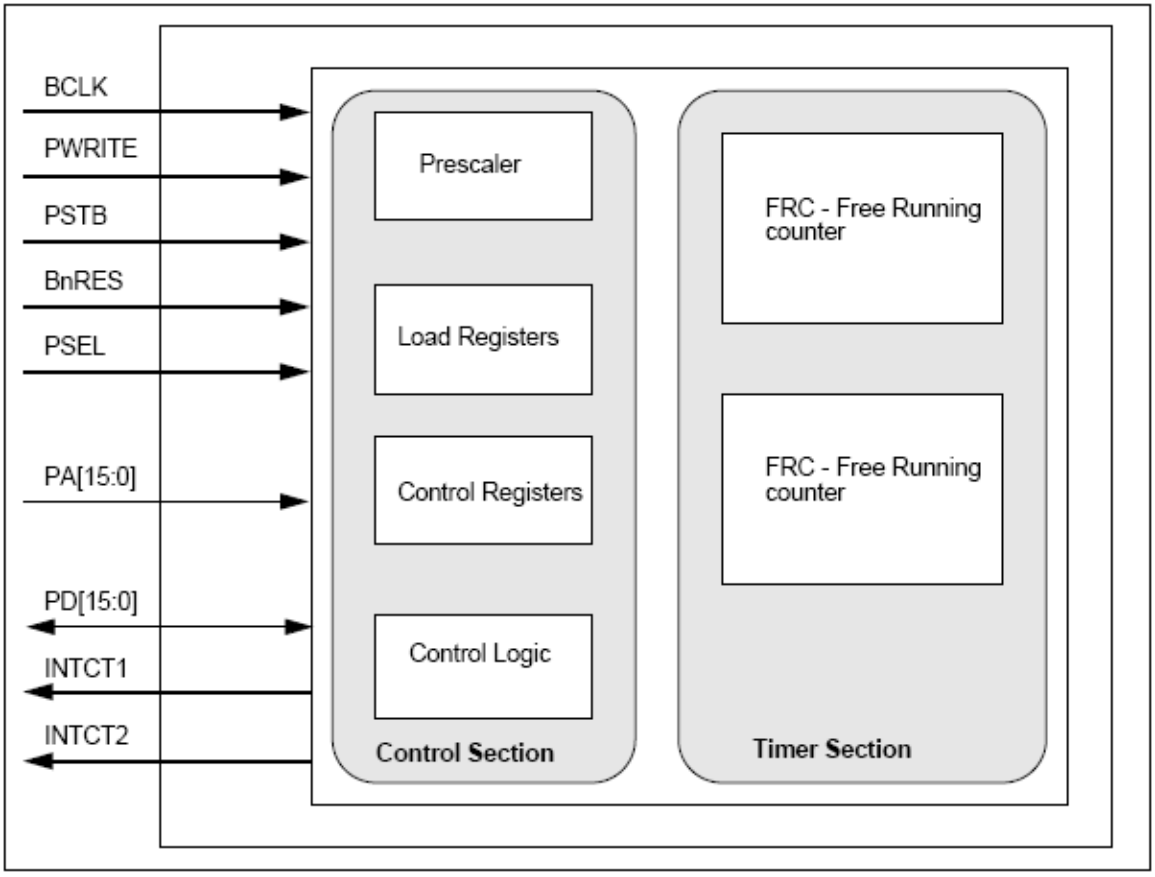


Figure 1-1 Timer module block diagram

This implementation consists of two major sections comprising:

- all the control logic
- two instantiations of the free-running counters (FRCs).

The timer module has a series of memory-mapped locations that allow the state of the timer module to be read from and written to via the APB.

1.2 Hardware Interface and Signal Description

Table 1-1 APB signal descriptions

Name	Type	Source/Destination	Description
BCLK	In		System (bus) clock. This clock times all bus transfers. The clock has two distinct phases—phase 1 in which **BCLK** is LOW and phase 2 in which **BCLK** is HIGH.
PA[15:0]	In	APB Bridge	This is the peripheral address bus, which is used by individual peripherals for decoding register accesses to that peripheral. The addresses become valid before **PSTB** goes HIGH and remains valid after **PSTB** goes LOW.
PD[15:0]	InOut	APB Peripherals, BD bus	This is the bidirectional peripheral data bus. The data bus is driven by this block during read cycles (when **PWRITE** is LOW).
PSTB	In	APB Bridge	This strobe signal is used to time all accesses on the peripheral bus. The falling edge of **PSTB** is coincident with the falling edge of **BCLK**.
PWRITE	In	APB Bridge	When HIGH, this signal indicates a write to a peripheral, and when LOW, a read from a peripheral. This signal has the same timing as the peripheral address bus. It becomes valid before **PSTB** goes HIGH and remains valid after **PSTB** goes LOW.
PSEL	In	APB Bridge	When HIGH, this signal indicates the timer module has been selected by the APB bridge. This selection is a decode of the ASB system address bus. See *AMBA Peripheral Bus Controller* (ARM DDI 0044) for more details.
INTCT1	Out	APB peripherals	Active HIGH interrupt signal to the Interrupt Controller module. This signal indicates that an interrupt has been generated in timer 1.
INTCT2	Out	APB peripherals	Active HIGH interrupt signal to the Interrupt Controller module. This signal indicates that an interrupt has been generated in timer 2.
BnRES	In	Reset Controller	Active LOW bus reset signal.

Writes to the Timer module are generated from the Peripheral Bus Controller module. Figure 1-2 summarizes this.

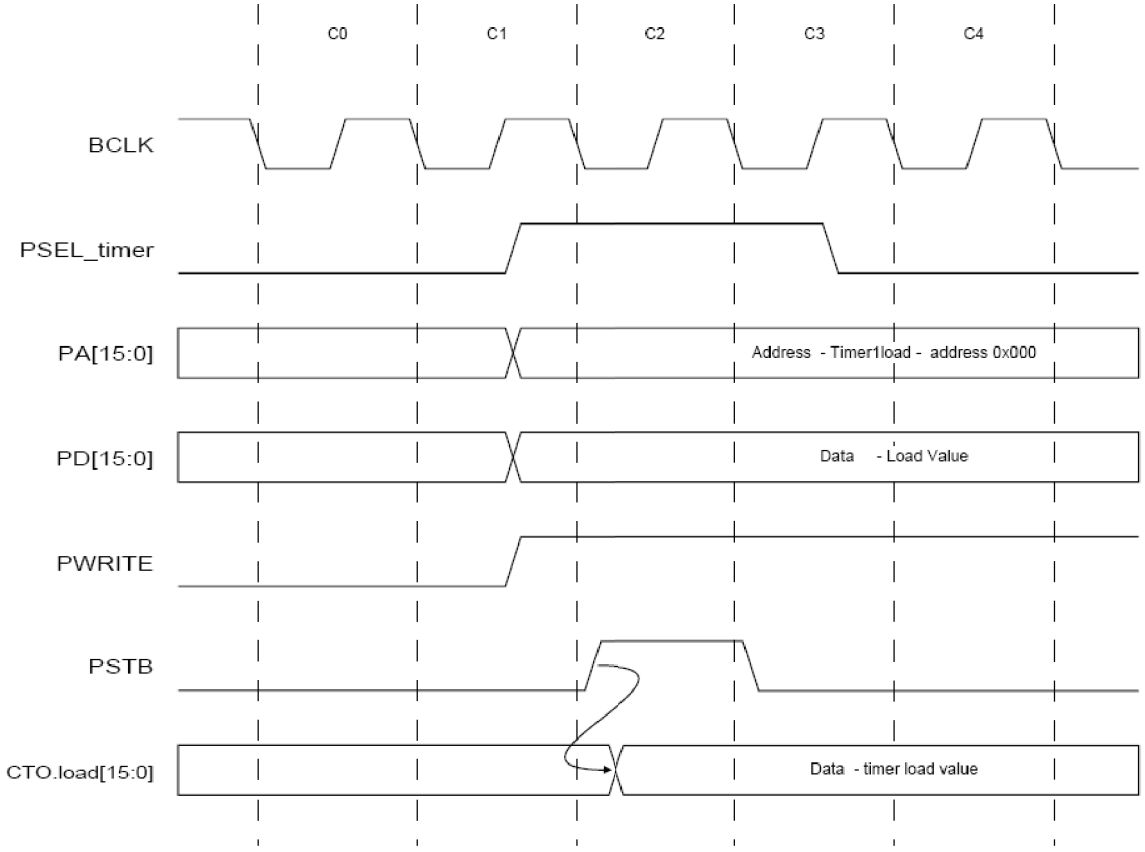


Figure 1-2 Timer module APB write cycle

1.3 Timer Introduction

Two timers are defined as the minimum provided within a system, although this may be expanded easily. The same principle of simple expansion has been applied to the register configuration, allowing more complex timers to be used; these are, from the programmer's model, compatible with those already defined.

Two modes of operation are available:

Free-running mode

The timer wraps after reaching its zero value, and continues to count down from the maximum value.

Periodic timer mode

The counter generates an interrupt at a constant interval.

1.4 Timer Operation

The timer is loaded by writing to the load register and, if enabled, counts down to zero. When zero is reached, an interrupt is generated. The interrupt may be cleared by writing to the Clear register.

After reaching a zero count, if the timer is operating in free-running mode it continues to decrement from its maximum value. If periodic timer mode is selected, the timer reloads from the load register and continues to decrement. In this mode the timer effectively generates a periodic interrupt. The mode is selected by a bit in the Control register.

At any point, the current timer value may be read from the Value register.

The timer is enabled by a bit in the control register. At reset, the timer is disabled, the interrupt is cleared and the Load register is undefined. The mode and prescale value is also undefined.

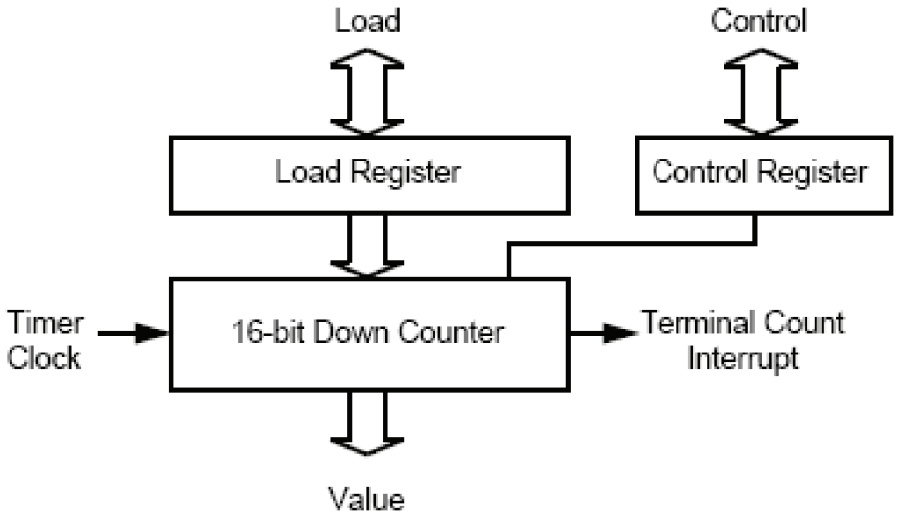


Figure 1-3 Timer operation

The timer clock is generated by a prescale unit. The timer clock may be one of:

- the system clock
- the system clock divided by 16, generated by 4 bits of prescale
- the system clock divided by 256, generated by a total of 8 bits of prescale.

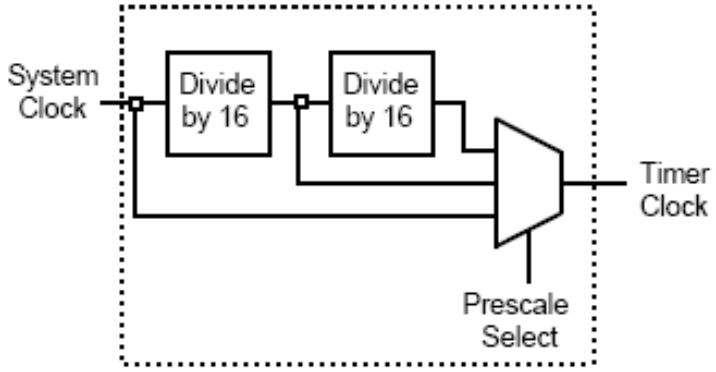


Figure 1-4 Prescale unit

1.5 Timer Memory Map

The base address of the timers is not fixed and may be different for any particular system implementation. However, the offset of any particular register from the base address is fixed.

Table 1-2 Memory map of the timer APB peripheral

Address	Read Location	Write Location
TimerBase	Timer1Load	Timer1Load
TimerBase + 0x04	Timer1Value	Reserved
TimerBase + 0x08	Timer1Control	Timer1Control
TimerBase + 0x0C		Timer1Clear
TimerBase + 0x20	Timer2Load	Timer2Load
TimerBase + 0x24	Timer2Value	Reserved
TimerBase + 0x28	Timer2Control	Timer2Control
TimerBase + 0x2C		Timer2Clear
Test Registers		
TimerBase + 0x10	Timer1Test	Timer1Test
TimerBase + 0x30	Timer2Test	Timer2Test

1.6 Timer Register Descriptions

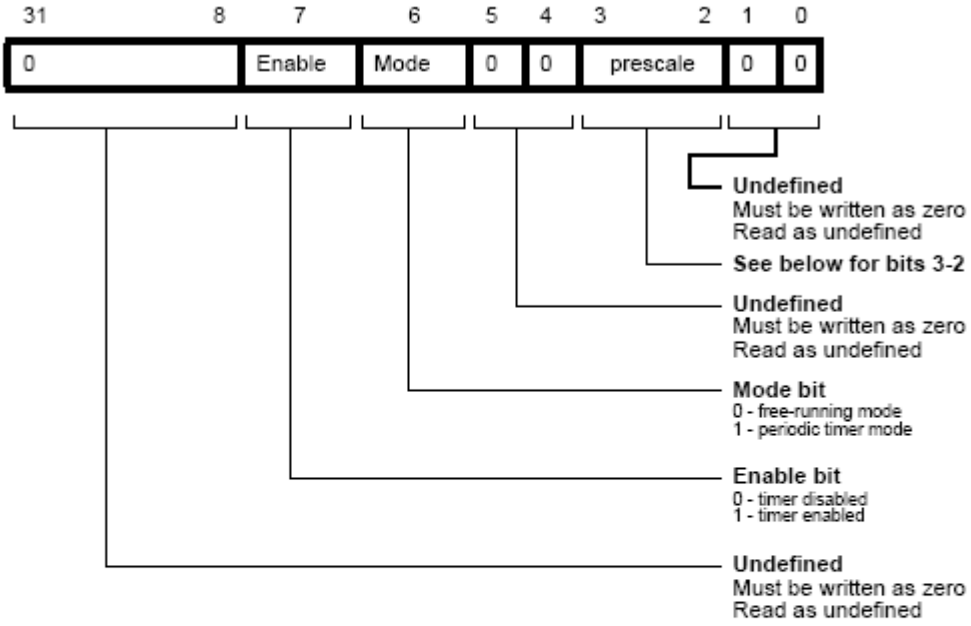
Load Read-write register. (Timer1Load, Timer2Load). The Load register contains the initial value of the timer and is also used as the reload value in periodic timer mode. When writing to this register the top 16 bits should be written as 0; when reading, the top 16 bits are undefined.

Value Read-only register. (Timer1Value, Timer2Value). The Value location gives the current value of the timer. When reading this location, the top 16 bits are read as undefined.

Clear Write-only register. (Timer1Clear, Timer2Clear). Writing to the Clear location clears an interrupt generated by the counter timer.

Control Read-write register. (Timer1Control, Timer2Control). The Control register provides enable/disable, mode and prescale configurations for the timer.

Figure 1-5 on page 1-10 defines the operation of the Control register.



Bit 3	Bit 2	Clock divided by	Stages of prescale
0	0	1	0
0	1	16	4
1	0	256	8
1	1	Undefined	

Figure 1-5 The Control register

1.7 Test Register

Two special registers are provided for validation purposes: Timer1Test and Timer2Test. These locations should not be accessed during normal operation.

Both registers are read-write and are 2 bits wide:

Table 1-3 Test register bit functions

Bit	Name	Function
0	test	Counter Test Mode
1	clksel	Test Clock Select

When the Counter Test Mode bit is set, the 16-bit counter of the selected timer is divided into four separate 4-bit counters that continually loop round from 15 to 0. This ensures the correct counting sequence is performed. Clearing this bit (default) brings the selected timer back to normal operation.

When the Test Clock Select bit is set in any of the two test registers, a special test clock (**PSTB** ANDed with **PSEL**) is fed into the prescale unit instead of the system clock. Clearing this bit (default) selects the system clock as the prescale clock input (normal operation).

