FINAL

Am29F010

1 Megabit (131,072 x 8-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% read, write, and erase**
  - Minimizes system level power consumption
- **Compatible with JEDEC-standard commands**
  - Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin PLCC/LCC
  - 32-pin TSOP
  - 32-pin DIP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - 45 ns maximum access time
- **Sector erase architecture**
  - 8 equal size sectors of 16K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Embedded Erase™ Algorithms**
  - Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  - Automatically programs and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - 20 mA typical active read current
  - 30 mA typical program/erase current
  - 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector Protection**
  - Hardware method disables any combination of sectors from program or erase operations

GENERAL DESCRIPTION

The Am29F010 is a 1Mbit, 5.0 V-only Flash memory organized as 128K bytes of 8 bits each. The Am29F010 is offered in a 32-pin package which allows for upgrades to 4 Mbit densities in the same pin out. This device is designed to be programmed or erased in-system with the standard system 5.0 V V_{CC} supply. 12.0 V V_{PP} is not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The Am29F010 offers access times between 45 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The Am29F010 is entirely pin and command set compatible with JEDEC standard 1 Mbit E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The Am29F010 is programmed by executing the program command sequence. This will invoke the Embedded Program algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than 0.3 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase algorithm which is an internal algorithm that automatically preprograms the array if it is not already

PRODUCT SELECTOR GUIDE

Family Part No:	Am29F010				
Ordering Part No: V_{CC} = 5.0 V ± 5%	-45				
Read Voltage V_{CC} = 5.0 V ± 10%		-55	-70	-90	-120
Max Access Time (ns)	45	55	70	90	120
$\overline{CE}$ ($\overline{E}$) Access (ns)	45	55	70	90	120
$\overline{OE}$ ($\overline{G}$) Access (ns)	25	30	30	35	50

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programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. The entire memory is typically erased and verified in three seconds (including pre-programming).

Any individual sector is typically erased and verified in 1.3 seconds (including pre-programming).

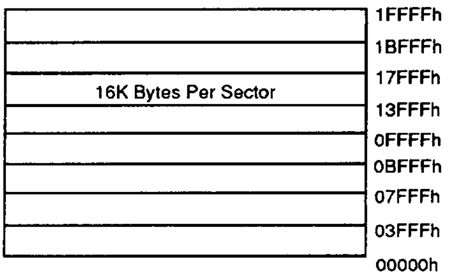
This device also features a sector erase architecture. The sector mode allows for 16K byte blocks of memory to be erased and reprogrammed without affecting other blocks. The Am29F010 is erased when shipped from the factory.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ7 or by the Toggle Bit feature on DQ6. Once the program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F010 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

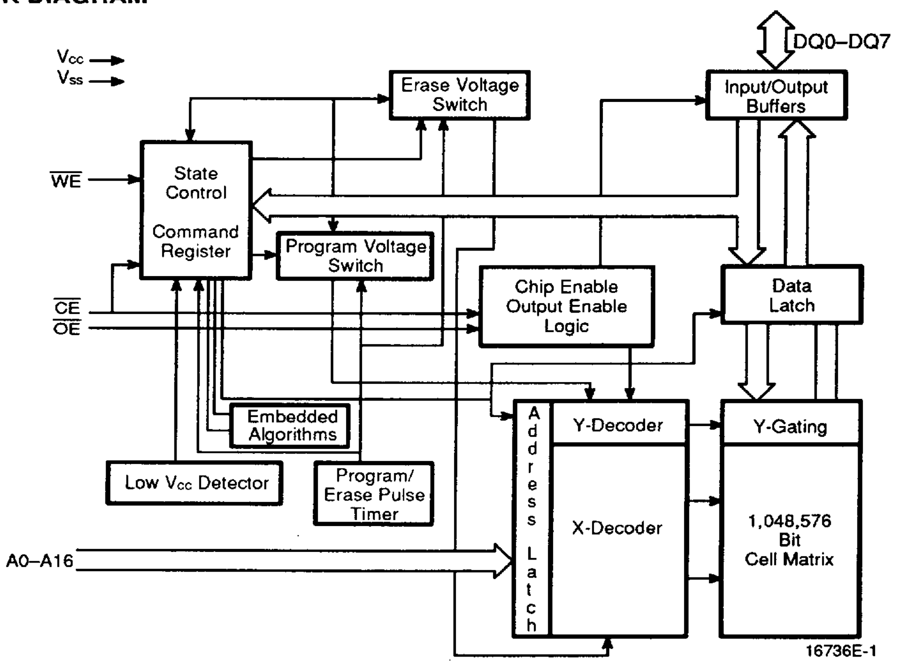
Flexible Sector-Erase Architecture

- 16K bytes per sector
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable



16736E-2

BLOCK DIAGRAM



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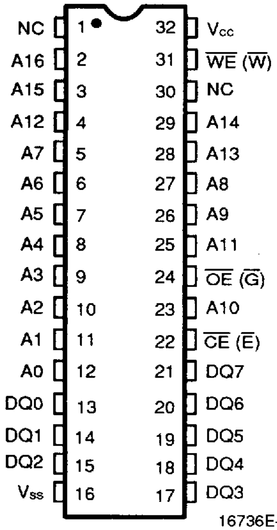
0257528 0032421 311

CONNECTION DIAGRAMS

CERDIP/PDIP



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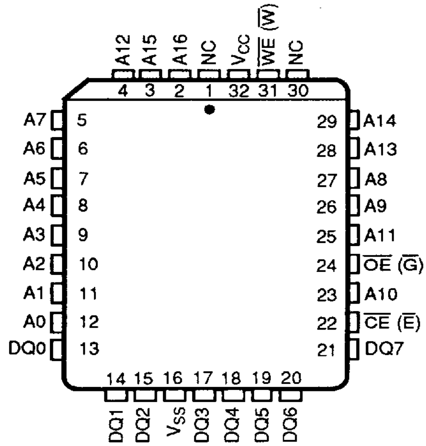
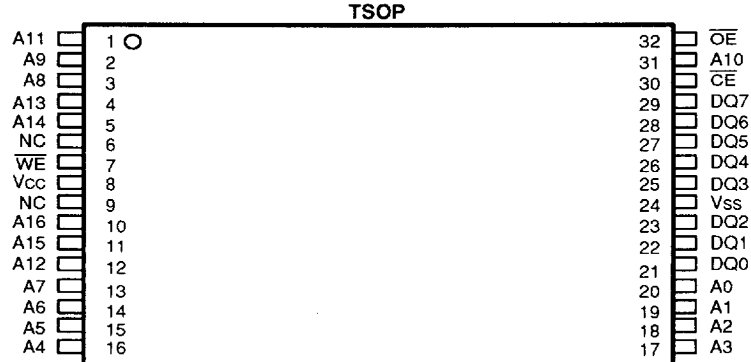
PLCC/LCC



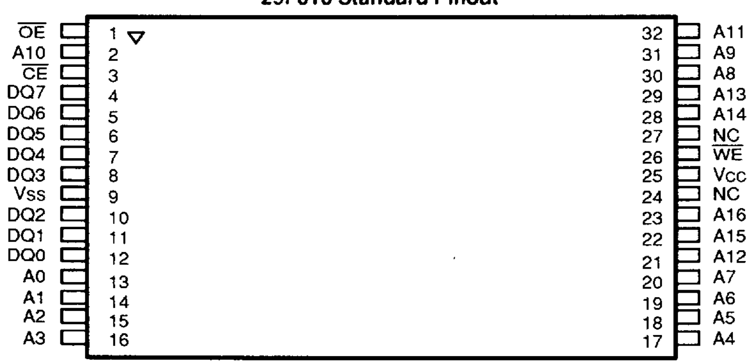
16736E-4

TSOP



29F010 Standard Pinout

16736E-5



29F010 Reverse Pinout

16736E-6

LOGIC SYMBOL

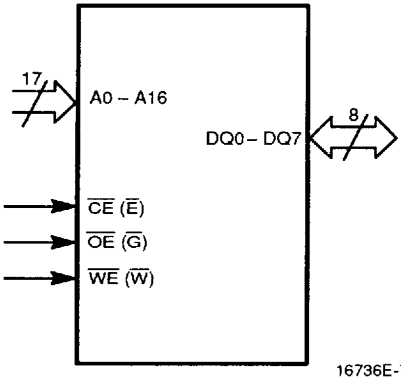


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Table 1. Am29F010 Pin Configuration

Pin	Function
A0–A16	Address Inputs
DQ0–DQ7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10% or ± 5%)
NC	No Internal Connection

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM29F010 -45 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
E = 32-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 032)
F = 32-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR 032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29F010
1 Megabit (128K x 8-Bit) CMOS Flash Memory
5.0 V Program and Erase
16K Byte Sectors

Valid Combinations	
AM29F010-45	JC, EC, FC
AM29F010-55	PC, PI, JC, JI, EC, EI, FC, FI
AM29F010-70 AM29F010-90 AM29F010-120	PC, PI, JC, JI, PCB, PIB, JCB, JIB, PE, PEB, JE, JEB, EC, EI, FC, FI, EE, EEB, FE, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

AM29F010 -70 /B X A

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CD 032)
U = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLR 032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29F010
1 Megabit (128K x 8-Bit) CMOS Flash Memory
5.0 V Program and Erase
16K Byte Sectors

Valid Combinations	
AM29F010-70	/BXA, /BUA
AM29F010-90	
AM29F010-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Table 2. Am29F010 User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A9	I/O
Auto-Select Manufacturer Code (1)	L	L	H	L	L	V_{ID}	Code
Auto-Select Device Code (1)	L	L	H	H	L	V_{ID}	Code
Read	L	L	H	A0	A1	A9	D_{OUT}
Standby	H	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A9	D_{IN} (2)
Enable Sector Protect	L	V_{ID}	L	X	X	V_{ID}	X
Verify Sector Protect (3)	L	L	H	L	H	V_{ID}	Code

Legend:

L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels

Notes:

1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tables 3 and 4.*
2. *Refer to Table 4 for valid D_{IN} during a write operation.*
3. *Refer to the section on Sector Protection*

Read Mode

The Am29F010 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Standby Mode

The Am29F010 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at Vcc + 0.5 V), when the current consumed is less than 100 µA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0 and A1.

The manufacturer and device codes may also be read via the command register, for instances when the Am29F010 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 4 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacture's code (AMD=01H) and byte 1 (A0 = V_{IH}) the device identifier code (Am29F010=20H). These two bytes are given in the table below. All identifiers for manufactures and device will exhibit odd parity with the MSB (DQ7) defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be V_{IL} (see Table 3).

Table 3. Am29F010 Autoselect and Sector Protection Verify Codes

Type	A16	A15	A14	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	X	X	X	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Am29F010 Device Code	X	X	X	V_{IL}	V_{IH}	20H	0	0	1	0	0	0	0	0
Sector Protection Verify	Sector Addresses			V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

**Outputs 01H at protected sector addresses. Outputs 00H at unprotected sector addresses.*

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F010 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 7). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (see AMD's *ExpressFlash Service* section in the data book).

To activate this mode, the programming equipment must force V_{ID} on address pin A9 and control pin $\overline{OE}$. The sector addresses (A16, A15, and A14) should be set to the sector to be protected. Table 4 defines the sector addresses for each of the eight (8) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Reading the device at a particular sector address (A16, A15 and A14) will produce 01H at data outputs (DQ0–DQ7) for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A0 and A1, are don't care. Address location 02H is reserved to verify sector protection of the device. Address pin A1 must be held at V_{IH} and A0 at V_{IL} (please refer to Table 3). Address location 00H and 01H are reserved for autoselect codes. If a verify of the sector protection circuitry were done at these addresses, the device would output the manufacturer and device codes respectively.

Table 4. Sector Addresses Table

	A16	A15	A14	Addr Range
SA0	0	0	0	00000h-03FFFh
SA1	0	0	1	04000h-07FFFh
SA2	0	1	0	08000h-0BFFFh
SA3	0	1	1	0C000h-0FFFFh
SA4	1	0	0	10000h-13FFFh
SA5	1	0	1	14000h-17FFFh
SA6	1	1	0	18000h-1BFFFh
SA7	1	1	1	1C000h-1FFFFh

It is also possible to determine if a sector is protected in the system by writing the autoselect command. Performing a read operation at particular sector addresses (A16, A15, A14) and with A1 = V_{IH} and A0 = V_{IL} (other addresses are a don't care) will produce 01H data if those sectors are protected. (Please refer to Table 3). Otherwise the device will read 00H for an unprotected sector. Please refer to the section on Sector Protection Algorithms for more details.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Table 5 defines these register command sequences.

Table 5. Am29F010 Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H	00H/01H	01H/20H				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H

Notes:

1. *Address bit A15 = X = Don't Care. Write Sequences may be initiated with A15 in either state.*
2. *Address bit A16 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).*
3. *Bus operations are defined in Table 2.*
4. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A16, A15, A14 will uniquely select any sector.
5. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XXX0H retrieves the manufacturer code of 01H. A read cycle from address XXX1H returns the device code 20H (see Table 3). A read cycle from address XXX2H returns information as to which sectors are protected. All manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so will hang up the device, or result in an apparent success according to the data polling algorithm. However, a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time-out of 80 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command (30H) to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µs time-out window, the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is stil open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase during this period will reset the device to read mode, ignoring the previous command string. Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 100 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read mode. $\overline{Data}$ Polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Write Operation Status

Table 6. Hardware Sequence Flags

	Status	DQ7	DQ6	DQ5	DQ3	DQ2–DQ0
In Progress	Auto-Programming	$\overline{DQ7}$	Toggle	0	0	Reserved for future use
	Program/Erase in Auto Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto-Programming	$\overline{DQ7}$	Toggle	1	0	Reserved for future use
	Program/Erase in Auto-Erase	0	Toggle	1	1	

Note: *DQ4 for AMD internal use only.*

DQ7
Data Polling

The Am29F010 features Data Polling as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During the Embedded Programming Algorithm, an attempt to read the device will produce complement data of the data last written to DQ7. Upon completion of the Embedded Programming Algorithm an attempt to read the device will produce the true data last written to DQ7. Data Polling is valid after the rising edge of the fourth WE pulse in the four write pulse sequence.

During the Embedded Erase Algorithm, DQ7 will be "0" until the erase operation is completed. Upon completion data at DQ7 is "1". For chip erase, the Data Polling is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. For sector erase, the Data Polling is valid after the last rising edge of the sector erase WE pulse.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 6).

See Figure 11 for the Data Polling timing specifications and diagrams.

DQ6
Toggle Bit

The Am29F010 also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (OE toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth WE pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase WE pulse. The Toggle Bit is active during the sector time out.

It should be noted that either CE or OE toggling will cause DQ6 to toggle. See Figure 12 for the Toggle Bit timing specifications and diagrams.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The CE circuit will partially power down the device under these conditions (to approximately 2 mA). The OE and WE pins will control the output disable functions as described in Table 2.

If this failure condition occurs during the sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for additional program or erase operations. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute the program or erase command sequence.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused (other sectors are still functional and can be reused). The device must be reset to use other sectors.

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the system never reads valid data on the DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used. The device must be reset to continue using the device.

DQ3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence is completed.

If Data Polling or the Toggle Bit indicates that the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

PARALLEL DEVICE ERASURE

Since the device is completely self-timed, devices can be erased or programmed in parallel without consideration of other devices in the system.

Data Protection

The Am29F010 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features described below to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{cc} power-up and power-down, a write cycle is locked out for V_{cc} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{cc} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

Sectors of the Am29F010 may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

EMBEDDED ALGORITHMS

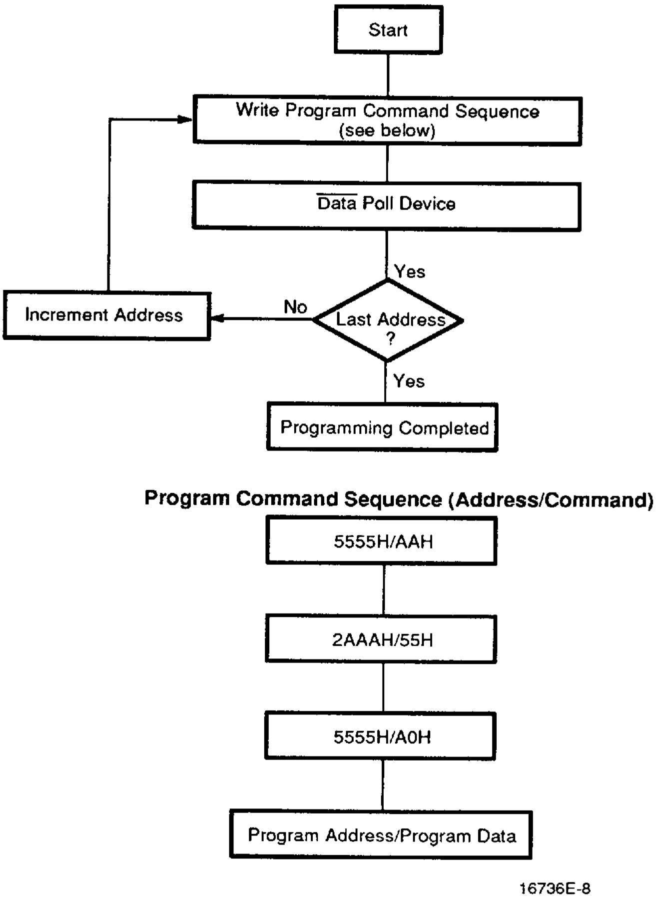


Figure 1. Embedded Programming Algorithm

Table 7. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Embedded Programming Algorithm	Valid Address/Data Sequence
Read		$\overline{\text{Data}}$ Polling to Verify Programming

EMBEDDED ALGORITHMS

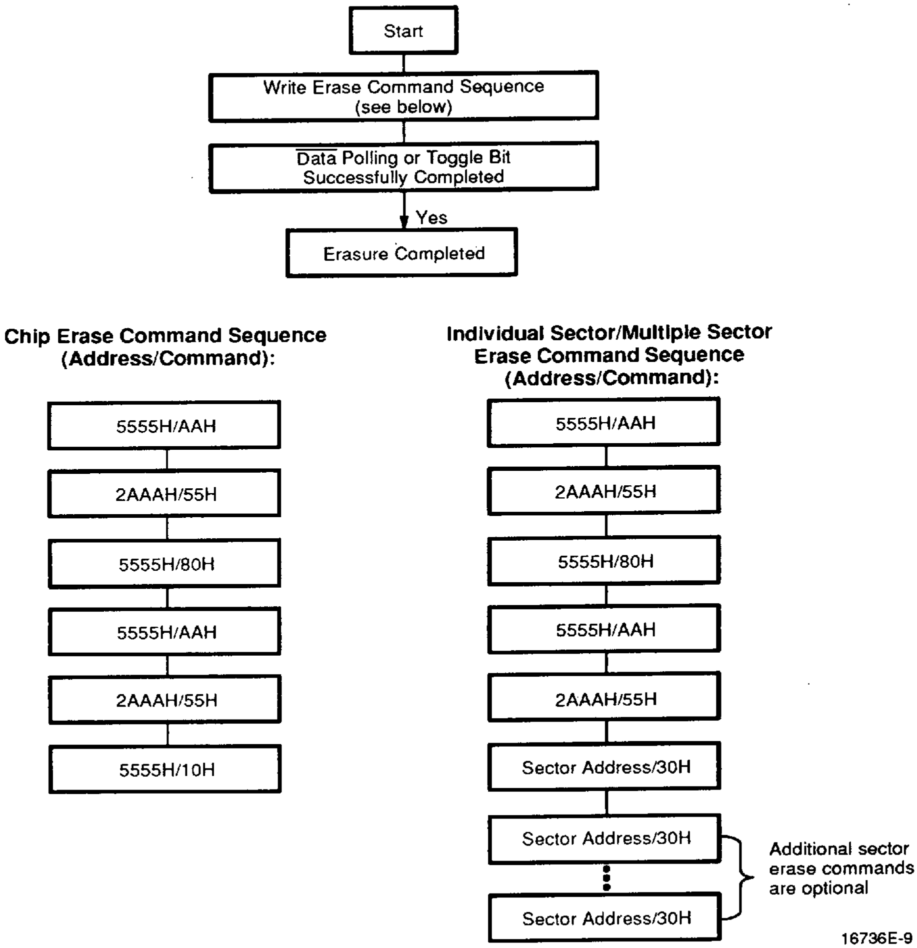
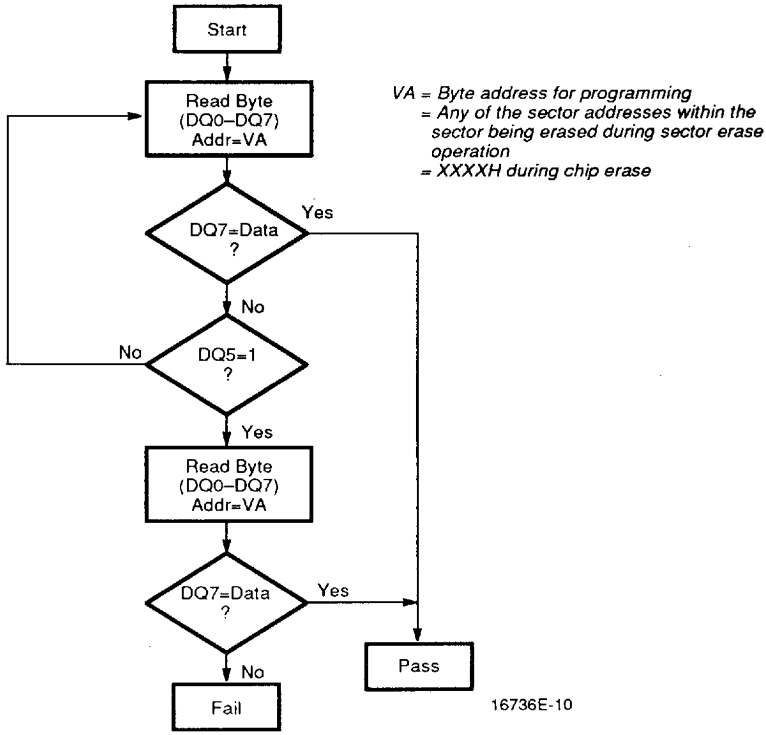


Figure 2. Embedded Erase Algorithm

Table 8. Embedded Erase Algorithm

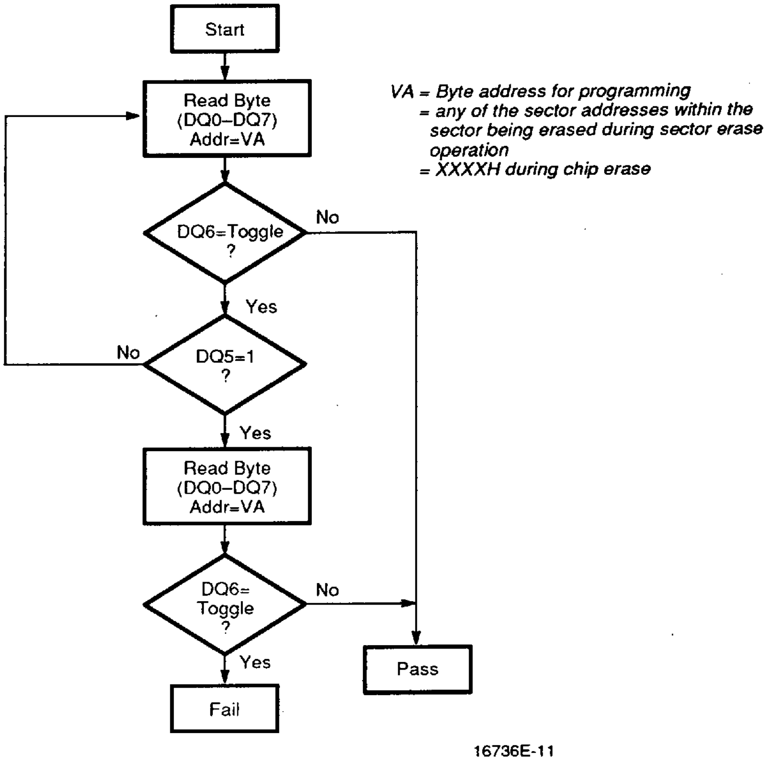
Bus Operations	Command Sequence	Comments
Standby		
Write	Embedded Erase Algorithm	
Read		Data Polling to Verify Erasure



Note:

1. DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure 3. $\overline{\text{Data}}$ Polling Algorithm



Note:

1. DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 4. Toggle Bit Algorithm

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages .... −65°C to +150°C
Plastic Packages .... −65°C to +125°C

Ambient Temperature
with Power Applied .... −55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 (Note 1) .... −2.0 V to +7.0 V

V_{CC} (Note 1) .... −2.0 V to +7.0 V

A9 (Note 2) .... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ...... 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 pin is −0.5 V. During voltage transitions, A9 may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) .... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) .... −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) .... −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) .... −55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am29F010-45 .... +4.75 V to +5.25 V

V_{CC} for Am29F010-55, 70, 90, 120 .... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

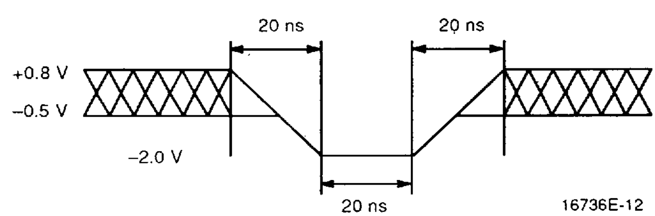


Figure 5. Maximum Negative Overshoot Waveform

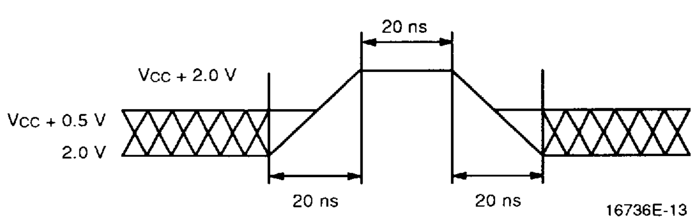


Figure 6. Maximum Positive Overshoot Waveform

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max		± 1.0	µA
I_{LIT}	A9 Input Load Current	V_{CC} = V_{CC} Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max		± 1.0	µA
I_{CC1}	V_{CC} Active Current for Read (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		30	mA
I_{CC2}	V_{CC} Active Current for Program or Erase (Notes 2, 3)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		50	mA
I_{CC3}	V_{CC} Standby Current	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{IH}		1.0	mA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{ID}	A9 Voltage for Autoselect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, V_{CC} = V_{CC} Min		0.45	V
V_{OH}	Output High Level	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min	2.4		V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{SS}$ to V_{CC}		± 1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{SS}$ to V_{CC}		± 1.0	µA
I_{CC1}	V_{CC} Active Current for Read (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
I_{CC2}	V_{CC} Active Current for Program or Erase (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.5$ V		100	µA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		0.7 V_{CC}	V_{CC} +0.5	V
V_{ID}	A9 Voltage for Autoselect	$V_{CC} = 5.0$ V	11.5	12.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 12.0$ mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH1}		$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}		V
V_{OH2}	Output High Voltage	$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min	V_{CC}–0.4		V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		V

Notes:

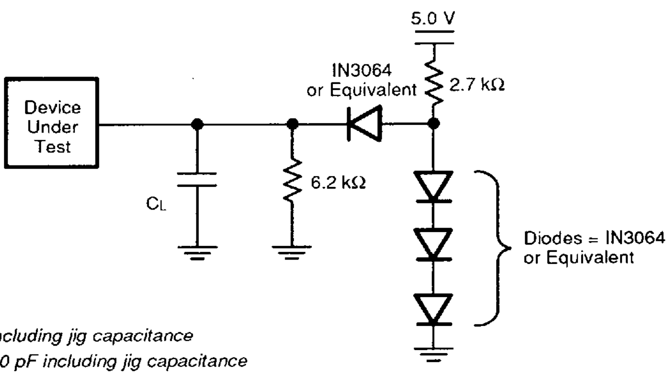
1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

AC CHARACTERISTICS—READ ONLY OPERATIONS CHARACTERISTICS

Parameter Symbols JEDEC	Parameter Symbols Standard	Description	Test Setup		-45 (1)	-55 (2)	-70 (2)	-90 (2)	-120 (2)	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)		Min	45	55	70	90	120	ns
t_{AVQV}	t_{ACC} (max)	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	45	55	70	90	120	ns
t_{ELQV}	t_{CE} (max)	Chip Enable to Output	$\overline{OE} = V_{IL}$	Max	45	55	70	90	120	ns
t_{GLQV}	t_{OE} (max)	Output Enable to Output		Max	25	30	30	35	50	ns
t_{EHQZ}	t_{DF} (max)	Chip Enable to Output High Z (Notes 3, 4)		Max	10	15	20	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 3, 4)		Max	10	15	20	20	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Max	0	0	0	0	0	ns

Notes:

1. *Test Conditions:*
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level
   Input: 1.5 V
   Output: 1.5 V
2. *Test Conditions:*
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level
   Input: 0.8 and 2.0 V
   Output: 0.8 and 2.0 V
3. *Output driver disable time.*
4. *Not 100% tested.*



Note:

For –45: C_L = 30 pF including jig capacitance
For all others: C_L = 100 pF including jig capacitance

16736E-14

Figure 7. Test Conditions

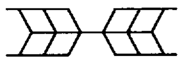
AC CHARACTERISTICS—WRITE/ERASE/PROGRAM OPERATIONS

Parameter Symbol JEDEC	Parameter Symbol Standard	Description		-45	-55	-70	-90	-120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 4)	Min	45	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	35	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	20	20	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time: Read (Note 4)	Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time: Toggle and $\overline{\text{Data}}$ Polling (Note 4)	Min	10	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	Min	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	Min	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	25	30	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Min	14	14	14	14	14	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (Note 1)	Min	2.2	2.2	2.2	2.2	2.2	sec
	t_{VCS}	V_{CC} Set Up Time (Note 4)	Min	50	50	50	50	50	µs
	t_{VLHT}	Voltage Transition Time (Notes 2, 4)	Min	4	4	4	4	4	µs
	t_{WPP}	Write Pulse Width (Note 2)	Min	10	10	10	10	10	ms
	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Notes 2, 4)	Min	4	4	4	4	4	µs
	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Notes 3, 4)	Min	4	4	4	4	4	µs

Notes:

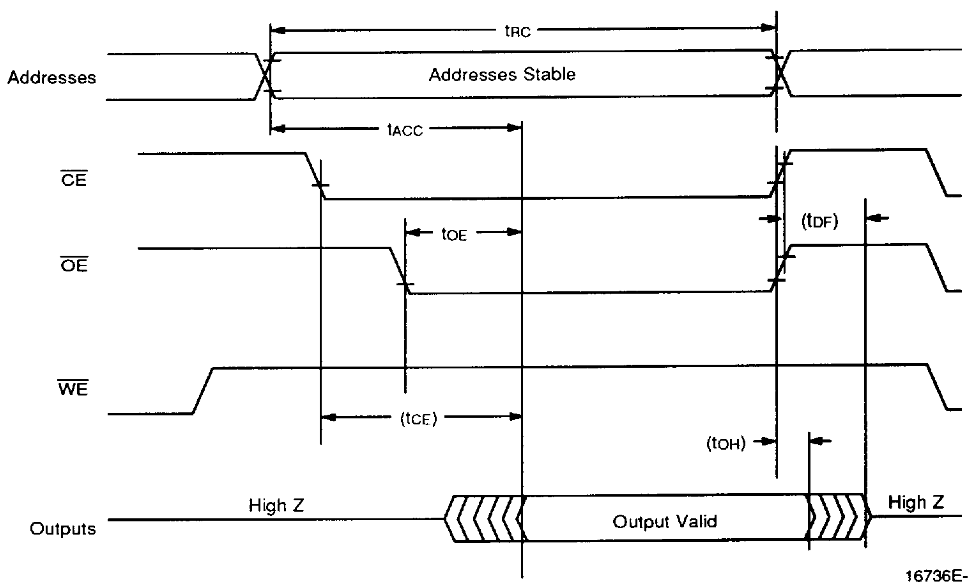
1. *This also includes the preprogramming time.*
2. *These timings are for Sector Protect/Unprotect operations.*
3. *This timing is only for Sector Unprotect.*
4. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

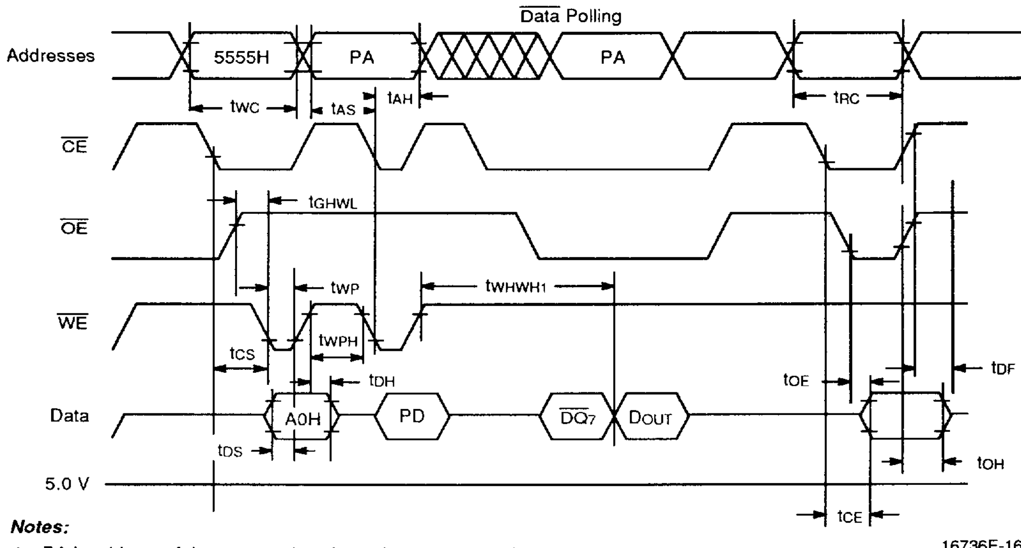
SWITCHING WAVEFORMS



16736E-15

Figure 8. AC Waveforms for Read Operations

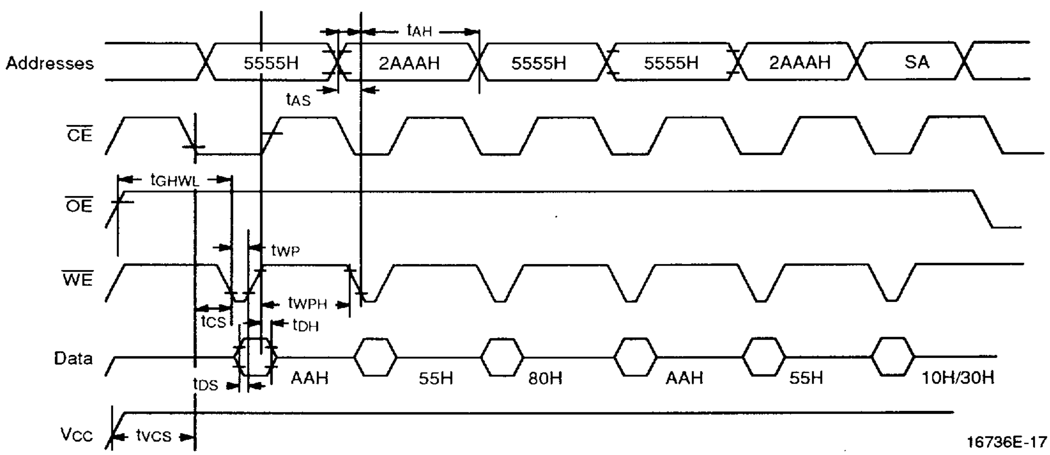
SWITCHING WAVEFORMS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *DQ7 is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 9. Program Operation Timings



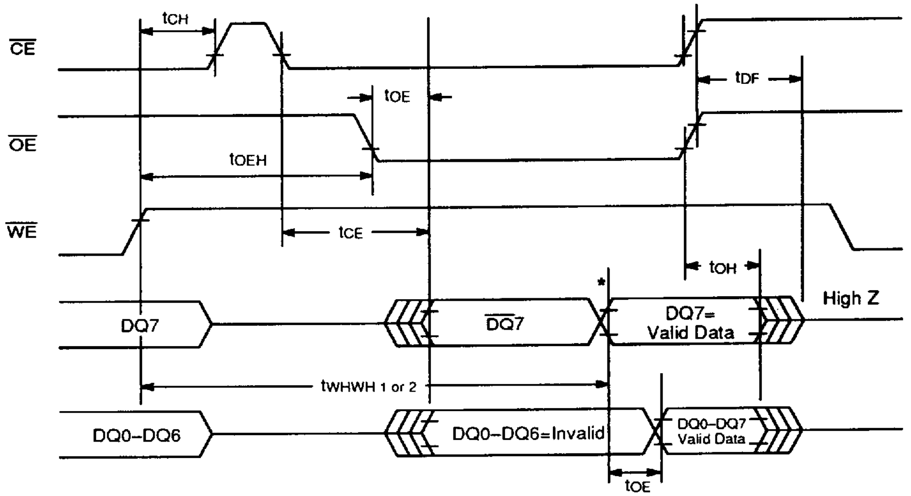
Note:

1. *SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.*

Figure 10. AC Waveforms Chip/Sector Erase Operations

0257528 0032442 046

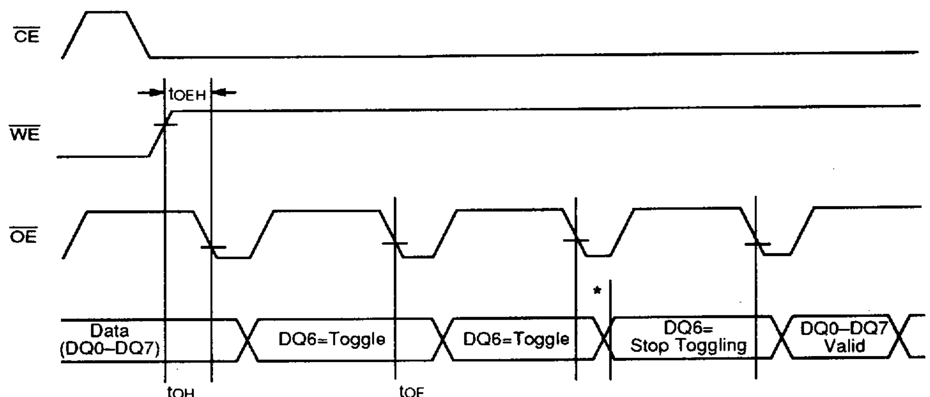
SWITCHING WAVEFORMS



**DQ7=Valid Data (The device has completed the Embedded operation).*

16736E-18

Figure 11. AC Waveforms for Data Polling During Embedded Algorithm Operations



16736E-19

Note:

**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 12. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

SECTOR PROTECTION ALGORITHMS

Sector Protection

The Am29F010 features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The sector addresses should be set using higher address lines A16, A15, and A14. The protection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH} (A9 remains high at V_{ID}). Reading the device at address location XXX2H, where the higher order addresses (A16, A15, and A14) define a particular sector, will produce 01H at data outputs (DQ0–DQ7) for a protected sector.

Sector Unprotect

The Am29F010 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pins $\overline{OE}$, $\overline{CE}$, and address pin A9. The address pins A6, A7, and A12 should be set to A7 = A12 = V_{IH}, and A6 = V_{IL}. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command. Performing a read operation at address location XXX2H, where the higher order addresses (A16, A15, and A14) define a particular sector address, will produce 00H at data outputs (DQ0–DQ7) for an unprotected sector.

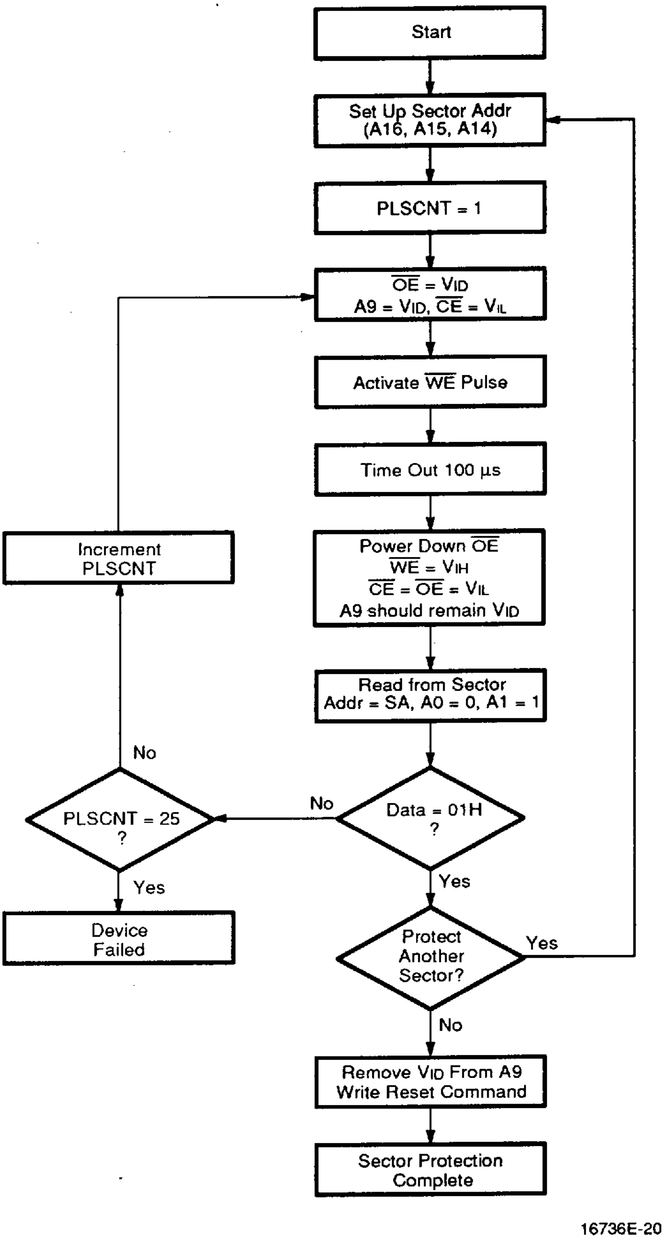
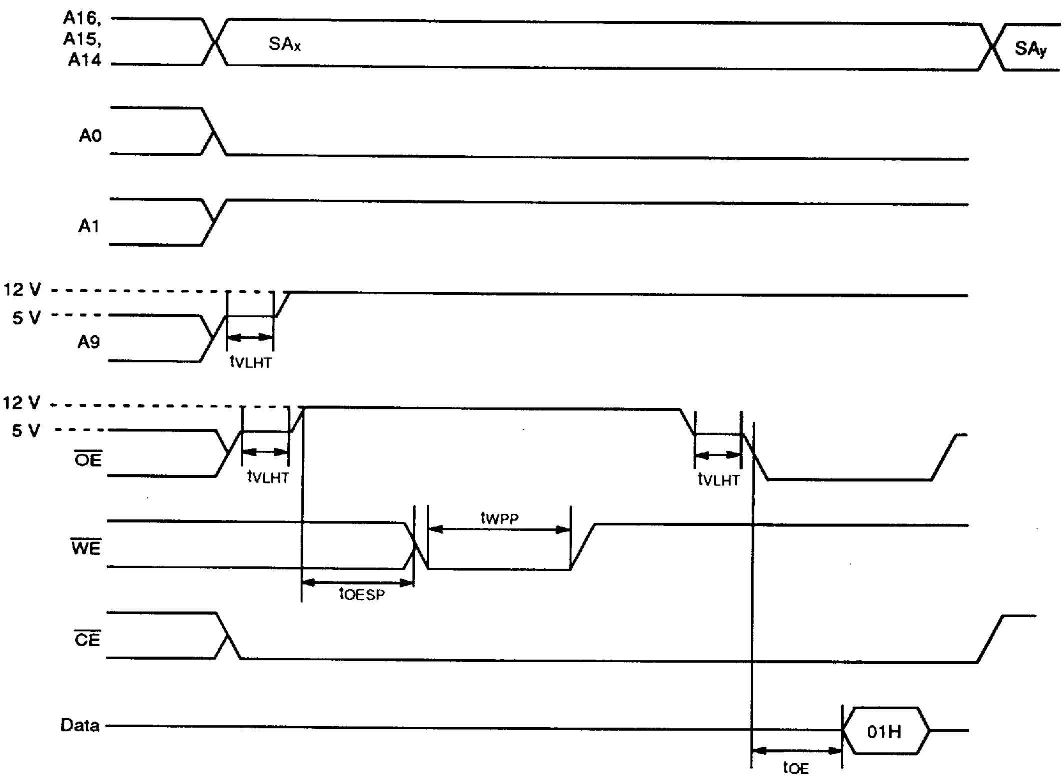


Figure 13. Sector Protection Algorithm

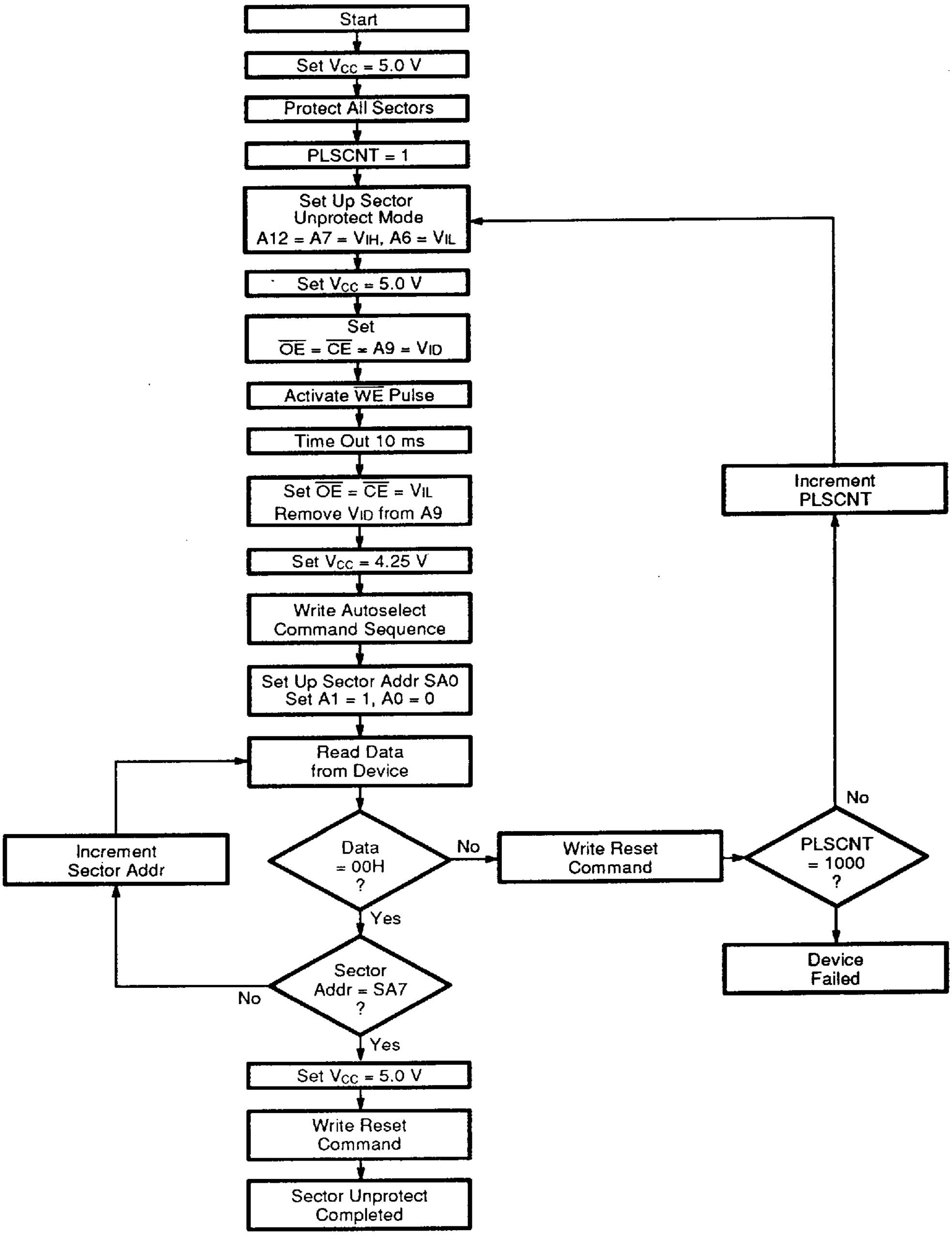
SWITCHING WAVEFORMS



SAx = Sector Address for initial sector
SAy = Sector Address for next sector

16736E-22

Figure 14. AC Waveforms for Sector Protection



Notes:
SA0 = Sector Address for initial sector
SA7 = Sector Address for last sector
Please refer to Table 4 for details.

Figure 15. Sector Unprotect Algorithm

SWITCHING WAVEFORMS

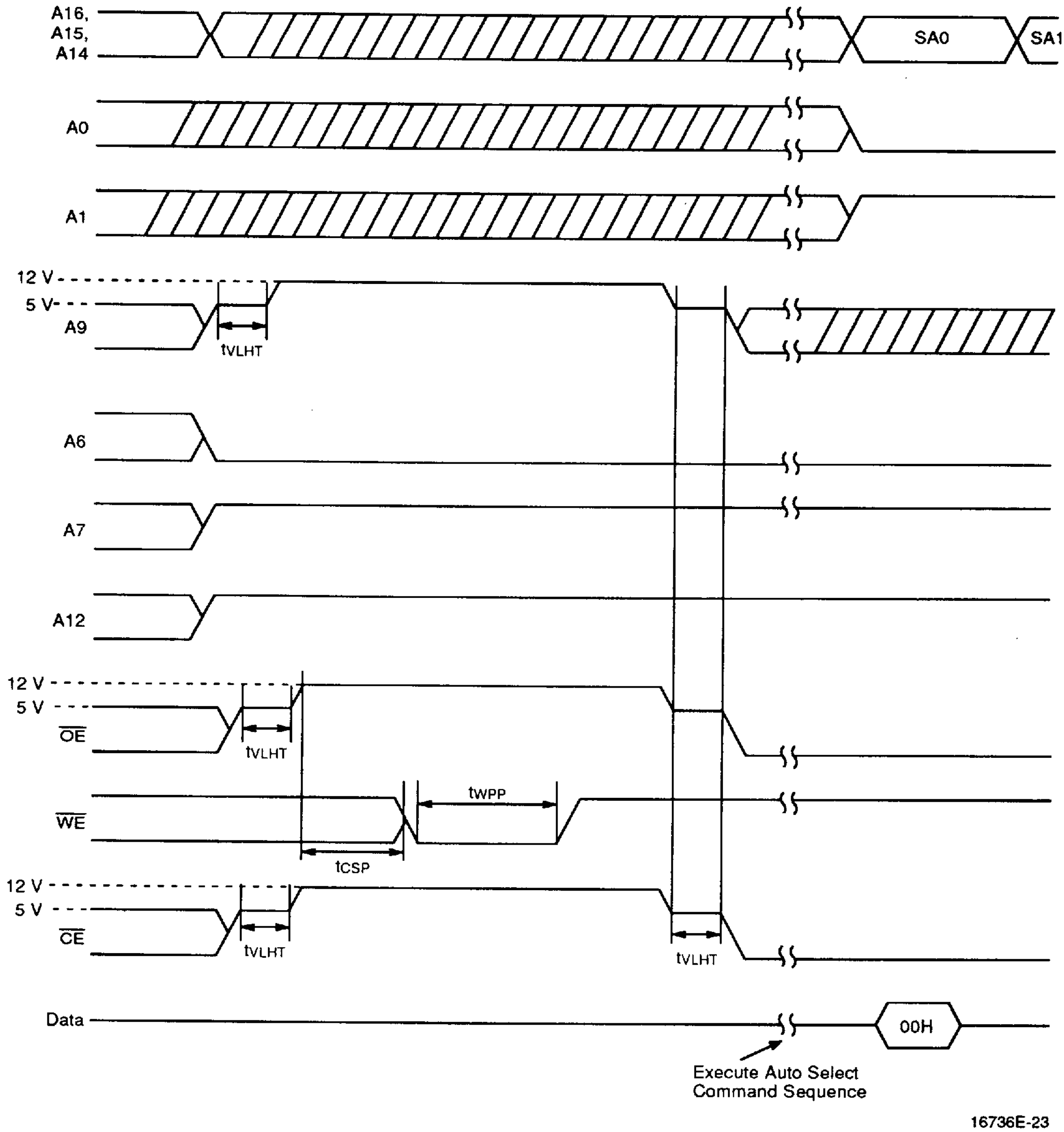


Figure 16. AC Waveforms for Sector Unprotect

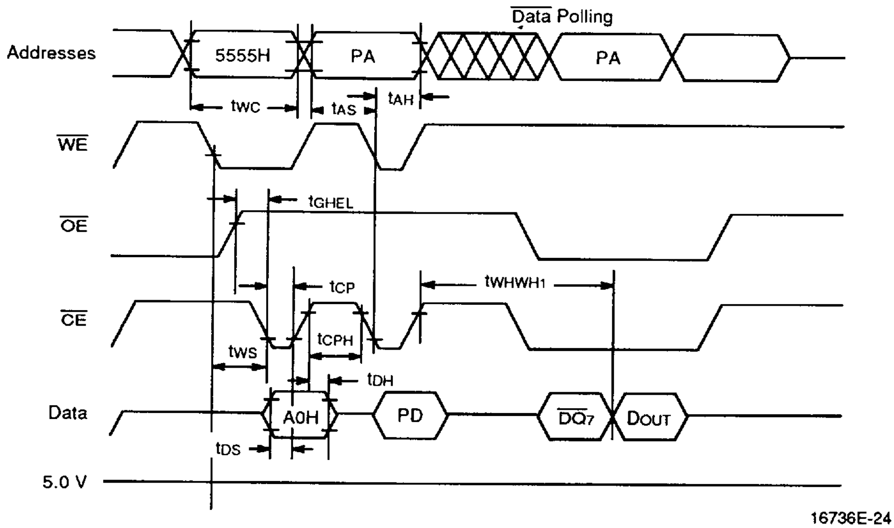
AC CHARACTERISTICS—WRITE/ERASE/PROGRAM OPERATIONS

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbol JEDEC	Parameter Symbol Standard	Description			-45	-55	-70	-90	-120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)		Min	45	55	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	20	20	30	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 2)	Min	0	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling (Note 2)	Min	10	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min	0	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min	0	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min	25	30	35	45	50	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Min	14	14	14	14	14	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (Note 1)		Min	2.2	2.2	2.2	2.2	2.2	sec
	t_{VCS}	V_{CC} Set Up Time (Note 2)		Min	2	2	2	2	2	µs

Notes:

1. *This also includes the preprogramming time.*
2. *Not 100% tested.*



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 17. Alternate $\overline{CE}$ Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE (Note 2)

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Chip/Sector Erase Time		1	10 (Note 1)	sec	Excludes 00H programming prior to erasure
Sector Programming Time		0.3		sec	
Chip Programming Time		2	12.5	sec	Excludes system-level overhead
Erase/Program Cycles	100,000	1,000,000		Cycles	
Byte Program Time		14		µs	
			60 (Notes 3, 4)	ms	

Notes:

1. *The Embedded Algorithm allows for 60 second erase time for military temperature range operations.*
2. *The Embedded Algorithms allow for a longer chip program and erase time. However, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.*
3. *DQ5 = "1" only after a byte takes longer than 60 ms to program.*
4. *A minimal number of bytes may require significantly more programming pulses then the typical byte. The majority of bytes will program within one or two pulses. This is demonstrated by the Typical and Maximum Chip Programming Times listed above.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9)	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
Current.	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

LCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

PDIP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

Data Sheet Revision Summary for Am29F010

Title

Data sheet is now Final, and not Preliminary.

Specify "1 Megabit" density.

General Description

Include statement "Am29F040 is erased when shipped from factory."

Write Operation Status, Table 6. Hardware Sequence Flags

Remove listing of DQ4 and made DQ4 as AMD's internal use only.

Remove paragraph on DQ4, Hardware Sequence Flag.

DC Characteristics TTL/NMOS Compatible

Add parameter I_{LIT}: "A9 Input Load Current"

Delete parameter I_{OS}: Output Short Curcuit Current.

DC Characteristics: CMOS Compatible

Add parameter I_{LIT}: "A9 Input Load Current."

Delete parameter I_{OS}: Output Short Curcuit Current.

AC Characteristics: Write/Erase/Program Operations

Correct t_{VCS}: V_{CC} Set Up Time from 2 m to 50 m.

Figure 13. Sector Protect Algorithm Flow Chart

Correct Time Out value from 10 m to 100 m.