Photometric Sensor for Gesture and Proximity

Data Sheet

ADUX1020

FEATURES

- Multifunction photometric sensor and signal conditioning
- Fully integrated AFE, ADC, LED driver, and timing core
- Usable for multiple optical measurement applications, including gesture control and proximity sensing
- Enables an ambient light rejection capability using both optical and analog filtering
- On-chip programmable flexible current sink for external LED
- High sensitivity and signal-to-noise ratio (SNR)
- High resolution position measurement
- Gesture recognition with 0.5 cm to 15 cm range
- Proximity sensing to 20 cm
- 400 kHz I²C interface
- Gesture/proximity works under infrared (IR) transparent glass or other materials
- Simple integration with optics; no need for precise alignment and no lens is required
- Low power operation
- 1.8 V analog/digital core
- 8-lead, 2 mm × 3 mm, 0.65 mm height LFCSP

APPLICATIONS

- Gesture for user interface (UI) control in portable devices
- Industrial/automation monitoring
- Presence detection
- Angle sensing

GENERAL DESCRIPTION

The ADUX1020 is a highly efficient photometric sensor with an integrated 14-bit analog-to-digital converter (ADC) and a 20-bit burst accumulator that works in concert with a flexible light emitting diode (LED) driver. It is designed to modulate a LED and measure the corresponding optical return signal. The digital engine includes circuitry and control for data aggregation and proximity detection.

The data output and device configuration use a 1.8 V I²C interface. The control circuitry includes flexible LED pulse width and period generation combined with synchronous detection. This circuitry is complemented by a low noise, low power, and wide dynamic range configurable analog front end (AFE), clock generation, LED driver, and digital logic for position and smart sample mode (event driven x, y coordinates, relative z data). This complete AFE features ambient light rejection, avoiding corruption due to external interference.

One inexpensive standard surface mount, broad angle or narrow angle IR LED (depending upon application) is required. This LED mounts externally to the ADUX1020.

Packaged in a small, clear mold, 2 mm × 3 mm, 8-lead LFCSP, the ADUX1020 is specified over an operating temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

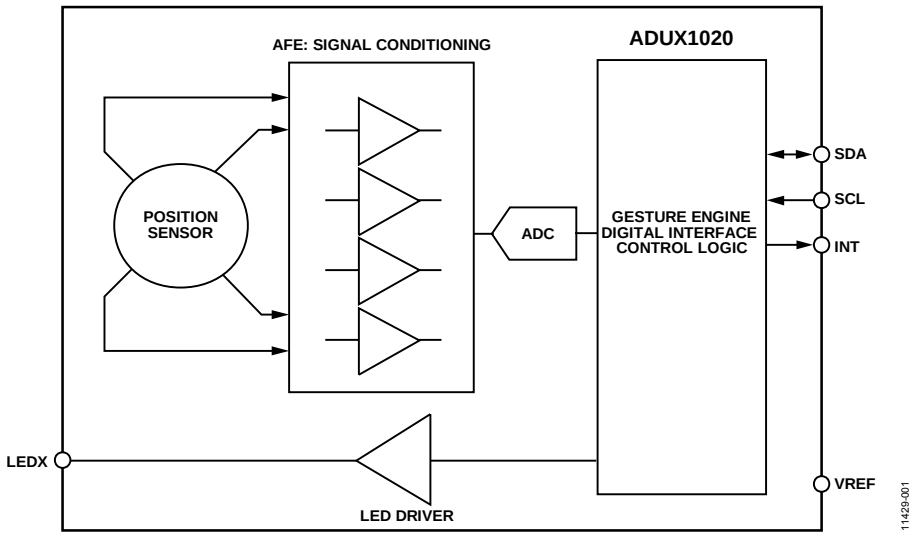

Figure 1.

Rev. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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- ADUX1020: Photometric Sensor for Gesture and Proximity Data Sheet

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- UG-1022: Evaluating the ADUX1020 Photometric Sensor for Gesture and Proximity

Reference Materials

Press

- Analog Devices' Optical Sensor Improves Reliability of Gesture Recognition Applications

Design Resources

- ADUX1020 Material Declaration
- PCN-PDN Information
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REVISION HISTORY

6/2016—Revision A: Initial Version

SPECIFICATIONS

TEMPERATURE AND POWER SPECIFICATIONS

Table 1. Operating Conditions

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE RANGE						
Operating Range			−40		+85	°C
Storage Range			−65		+150	°C
POWER SUPPLY VOLTAGES						
Input Supply Voltage	V_{DD}		1.7	1.8	1.9	V
Supply Voltage for the LEDs	V_{LED}	V_{LED} depend on the LED selected		3.3		V

V_{DD} = 1.8 V, ambient temperature, unless otherwise noted.

Table 2. Current Consumption

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TOTAL POWER CONSUMPTION		See the Calculating Current Consumption section				µW
V_{DD} STANDBY MODE CURRENT	$IV_{DD\_STANDBY}$			3.5		µA
SUPPLY CURRENT						
1.8 V V_{DD} Peak	IV_{DD_PEAK}	Continuous maximum rate AFE operation		<10		mA
1.8 V V_{DD} Average	IV_{DD_AVG}	See the Calculating Current Consumption section	30		10,000	µA
Example V_{DD} Average		LED_OFFSET = 25 µs, LED_PERIOD = 19 µs, LED_PULSES = 8, LED peak current = 250 mA				
		1 Hz data rate; proximity mode		6		µA
		50 Hz data rate; proximity mode		116		µA
		820 Hz data rate; sample/gesture mode		1965		µA
Average V_{LED}	I_{LED_AVG}	See the Calculating Current Consumption section	1		20,000	µA
Example V_{LED} Average		Peak LED current = 250 mA, LED_PULSE width = 3 µs				
1 Pulse (Proximity)		1 Hz data rate		1		µA
		50 Hz data rate		38		µA
		820 Hz data rate		615		µA
8 Pulses (Sample/Gesture)		50 Hz data rate		300		µA
		820 Hz data rate		4920		µA

PERFORMANCE SPECIFICATIONS

V_{DD} = 1.8 V, T_A = full operating temperature range, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPTICAL SENSOR					
Wavelength		845		960	nm
Field of View				120	Degrees
Gesture Recognition Range	50 Hz update rate, 5 mA total current, hand sized target	0.5		15	cm
Proximity	5 Hz update rate	0.5		20	cm
DATA AQUISITION					
Resolution	Single pulse		13		Bits
Output Data Rate		0.1		1400	Hz
LED DRIVER					
LED Current Slew Rate[1]	T_A = 25°C, I_{LED} = 70 mA				
Rise	Slew rate control setting = 0		131		mA/µs
	Slew rate control setting = 7		74		mA/µs
Fall	Slew rate control setting = 0		490		mA/µs
	Slew rate control setting = 7		84		mA/µs
LED Peak Current	LED pulse enabled	8		250	mA
Driver Compliance Voltage	Voltage above ground, LEDX pin required for controlled LED driver operation	0.2			V

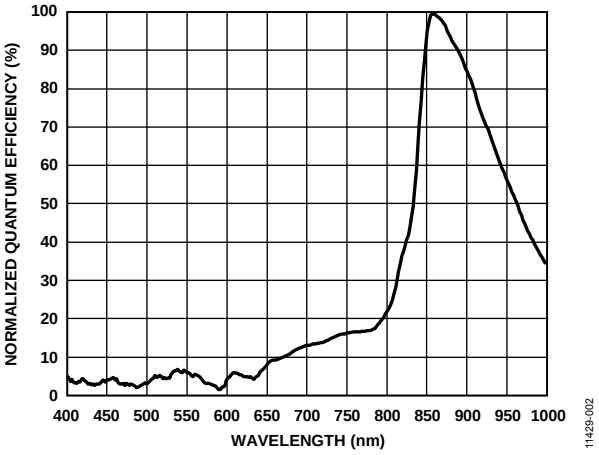

Figure 2. Normalized Quantum Efficiency of Combined Optical Filter and Silicon Detector

ANALOG SPECIFICATIONS

V_{DD} = 1.8 V, T_A = full operating temperature range, unless otherwise noted. AFE offset is correctly compensated as explained in the AFE Operation section.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PULSED SIGNAL CONVERSIONS, 3 µs WIDE LED PULSE[1]	4 µs wide AFE integration; Register 0x13 = 0xADA5				
ADC Resolution[2]	Transimpedance amplifier (TIA) feedback resistor				
	50 kΩ		0.82		nA/LSB
	100 kΩ		0.41		nA/LSB
	200 kΩ		0.2		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	50 kΩ		6.7		µA
	100 kΩ		3.35		µA
	200 kΩ		1.67		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	50 kΩ		18.5		µA
	100 kΩ		9.25		µA
	200 kΩ		4.63		µA
FULL SIGNAL CONVERSIONS[3]					
TIA Saturation Level of Pulsed Signal and Ambient Level	TIA feedback resistor				
	50 kΩ		25.2		µA
	100 kΩ		12.6		µA
	200 kΩ		6.3		µA
SYSTEM PERFORMANCE					
Total Output Noise Floor	Normal mode, per pulse, per channel, no LED				
	50 kΩ, referred to ADC input		2.4		LSB rms
	50 kΩ, referred to peak input signal for 3 µs LED pulse		2.0		nA rms
	50 kΩ, saturation SNR per pulse per channel		70.6		dB
	100 kΩ, referred to ADC input		3.4		LSB rms
	100 kΩ, referred to peak input signal for 3 µs LED pulse		1.4		nA rms
	100 kΩ, saturation SNR per pulse per channel		67.6		dB
	200 kΩ, referred to ADC input		5.5		LSB rms
	200 kΩ, referred to peak input signal for 3 µs LED pulse		1.1		nA rms
	200 kΩ, saturation SNR per pulse per channel		63.5		dB
DC Power Supply Rejection Ratio (DC PSRR)			−37		dB

[1] This saturation level applies to the ADC only and, therefore, includes only the pulsed signal. Any nonpulsatile signal is removed prior to the ADC stage.
[2] ADC resolution is given for a single pulse when the AFE offset is correctly compensated as explained in the AFE Operation section. If using multiple pulses, divide by the number of pulses.
[3] This saturation level applies to the full signal path and, therefore, includes both the ambient signal and the pulsed signal.

DIGITAL SPECIFICATIONS

V_{DD} = 1.7 V to 1.9 V, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS (SCL, SDA)						
Input Voltage						
High Level	V_{IH}	Proper operation to V_{DD} only	0.7 × V_{DD}		3.6	V
Low Level	V_{IL}				0.3 × V_{DD}	V
Input Current						
High Level	I_{IH}		−10		+10	µA
Low Level	I_{IL}		−10		+10	µA
Input Capacitance	C_{IN}			10		pF
LOGIC OUTPUTS						
Output Voltage		2 mA output current				
INT High Level	V_{OH}		V_{DD} − 0.5		V_{DD}	V
INT Low Level	V_{OL}				0.5	V
SDA Low Level	V_{OL1}				0.2 × V_{DD}	V
Current						
Maximum INT Pin	I_{INT}	Source or sink		6		mA
SDA Low Level Output	I_{OL}	V_{OL1} = 0.6 V	6			mA

TIMING SPECIFICATIONS

Table 6. I²C Timing Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
I²C PORT[1]		See Figure 3				
SCL Frequency				400		kHz
SCL Minimum Pulse Width High	t_1		600			ns
SCL Minimum Pulse Width Low	t_2		1300			ns
Start Condition Hold Time	t_3		600			ns
Start Condition Setup Time	t_4		600			ns
SDA Setup Time	t_5		100			ns
SCL and SDA Rise Time	t_6				1000	ns
SCL and SDA Fall Time	t_7				300	ns
Stop Condition Setup Time	t_8		600			ns

[1] Guaranteed by design.

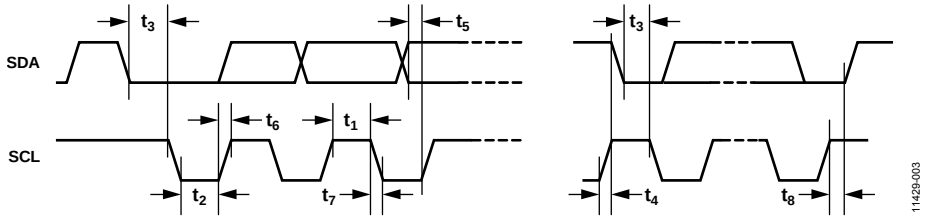

Figure 3. I²C Timing

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VDD to AGND/DGND	−0.3 V to +3.9 V
INT to DGND	−0.3 V to +3.9 V
LEDX to AGND	−0.3 V to +3.6 V
SCL to DGND	−0.3 V to +3.9 V
SDA to DGND	−0.3 V to +3.9 V
Junction Temperature	150°C
ESD	
Human Body Model (HBM)	1500 V
Charged Device Model (CDM)	1250 V
Machine Model (MM)	100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-8-17[1]	59.25	4.01	°C/W

[1] Test Condition: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

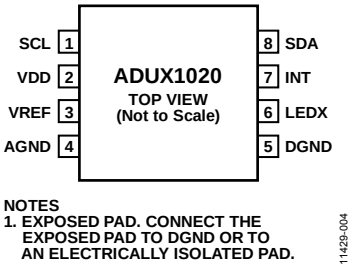

Figure 4. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	SCL	Digital input	Serial Clock for I²C Communication.
2	VDD	Supply	1.8 V Supply Input.
3	VREF	Input	Reference Voltage. Bypass this pin with a 1 µF to 4 µF capacitor from VREF to AGND.
4	AGND	Supply	Analog Ground.
5	DGND	Supply	Digital Ground.
6	LEDX	Analog input	LED Current Sink.
7	INT	Digital output	Interrupt Output.
8	SDA	Digital bidirectional	Serial Data.
	EPAD	Not applicable	Exposed Pad. Connect the exposed pad to DGND or to an electrically isolated pad.

TYPICAL PERFORMANCE CHARACTERISTICS

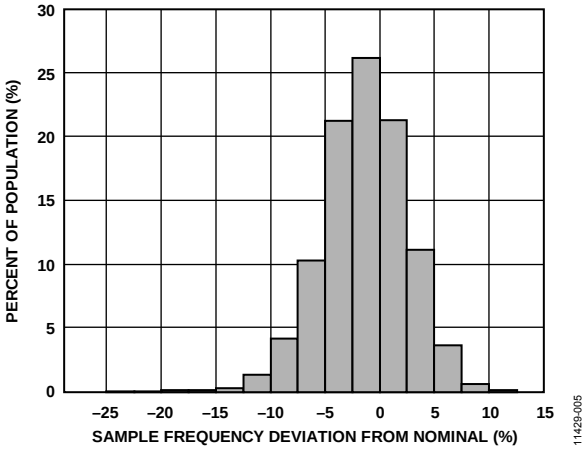

Figure 5. 32 kHz Clock Frequency Distribution (Typical Setting After Calibration: Register 0x18 = 0x2612)

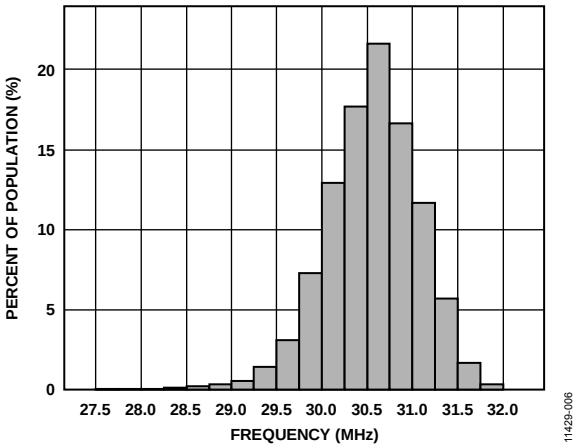

Figure 6. 32 MHz Clock Frequency Distribution (Default Settings Before User Calibration: Register 0x1A = 0x425E)

THEORY OF OPERATION

The ADUX1020 operates as a gesture and proximity optical sensor system, stimulating an LED and measuring the incident angle of returning light. It is a highly integrated system including an optical sensor, analog signal processing block, digital signal processing block, and I²C communication port. The optical sensor employed in this device is a photodiode that measures the angle of incident light and produces a highly linear output for a wide range of input angles.

The ADUX1020 can be configured in one of the following four modes by the command from the host processor through I²C port.

- Idle mode
- Standby mode
- Proximity mode
- Sample/gesture mode

IDLE MODE

The ADUX1020 enters idle mode automatically after power-up, and it stays in this low power mode until it receives a command from the host processor to move to any of the three other modes.

STANDBY MODE

Standby mode is a power saving mode in which no data collection occurs. This mode is the lowest power mode without cutting the external power supply. In this mode, all register values are retained. To place the device in standby mode, write 0x0 to Register 0x45, Bits[3:0]. No I²C acknowledge (ACK) generates for this write. Any write to this address causes the device to leave standby mode.

PROXIMITY MODE

When the ADUX1020 is configured for proximity mode, it pulses the LED based on the proximity configuration settings including update rate, peak LED current, and number of pulses. Proximity detection is performed by measuring the intensity of the light reflected from objects over the LED and sensor. This intensity is the sum of the four channels of the sensor. The ADUX1020 can generate an interrupt for a specific intensity event. An event is defined as the point when the intensity signal meets certain intensity threshold criteria. Two thresholds in proximity mode allow hysteresis: an on event and an off event threshold.

The value in Register 0x2A defines the threshold for an on event, and the ADUX1020 generates an interrupt when the intensity of the received light becomes higher than this value.

The value in Register 0x2B defines the threshold for an off event, and the ADUX1020 generates an interrupt when the intensity of the received light becomes lower than this value.

Upon receiving the interrupt, the host processor can read the intensity from the output buffer of the ADUX1020. It can also read the x and y coordinates of the detected object. The data format of the first in, first out (FIFO) output of the ADUX1020, can be specified using Register 0x45.

To place the device in proximity mode, write 0x1 to Register 0x45, Bits[3:0].

SAMPLE/GESTURE MODE

In sample/gesture mode, the ADUX1020 uses a second set of configuration registers and transmits LED pulses based on the configuration including update rate, peak LED current, and number of pulses, similar to the proximity mode. The LED signaling in the proximity and sample modes are similar except that a higher update rate is typically required for sample mode.

The ADUX1020 captures the coordinate samples for gesture interpretation, triggered by the events defined in Register 0x3E and Register 0x40.

When the start of a potential gesture is detected, the ADUX1020 can generate an interrupt. This feature allows the host processor to sleep while awaiting gesture activity.

The event that triggers an interrupt can be either absolute intensity or derivative of the intensity signal, and the ADUX1020 can generate an interrupt signal so that the host processor can sleep while awaiting gesture activity.

To place the device in sample mode, write 0x8 to Register 0x45, Bits[3:0].

USE OF MULTIPLE MODES

The ADUX1020 can programmatically enter sample/gesture mode when a certain input threshold in proximity mode is reached. The threshold, specified by a 16-bit number, can be set in Register 0x2C. To enable this behavior, write 1 to Register 0x45, Bit 10 and start the device in proximity mode.

ADJUSTABLE SAMPLING FREQUENCY

Register 0x40 controls the sampling frequency settings of the ADUX1020 for sample/gesture mode and proximity mode, and Register 0x18, Bits[5:0] further tune this clock for greater accuracy. The sampling frequency is governed by an internal 32 kHz sample rate clock that also drives the transition of the internal state machine. The maximum sampling frequency is 1.4 kHz. Note that the state machine continues until the desired number of LED pulses and periods between pulses has completed during the full sample. In addition, the programmed pulse train may not fit within a full sample period. The maximum sample frequency for sample/gesture mode is determined by

$$f_{SAMPLE,\ MAX} = 1/(t_{GEST} + t_A + t_{SLEEP}) \quad (1)$$

where:
t_{GEST} is the time required for a complete sample in sample/gesture mode.
t_A is the compute time for sample/gesture mode, defined in Table 10.
t_{SLEEP} is the minimum sleep time required between samples, defined in Table 10.

The maximum sample frequency for proximity mode is similar and determined by the following:

$$f_{SAMPLE,\ MAX} = 1/(t_{PROX} + t_B + t_{SLEEP}) \quad (2)$$

where:
t_{PROX} is the time required for a complete sample in proximity mode.
t_B is the compute time for proximity mode, defined in Table 10.
t_{SLEEP} is the minimum sleep time required between samples, defined in Table 10.

The timing parameters for sample/gesture and proximity mode are as follows:

$$t_{PROX} = LED\_OFFSET\_PROX + LED\_PULSES\_PROX \times LED\_PERIOD\_PROX \quad (3)$$

$$t_{GEST} = LED\_OFFSET\_GEST + LED\_PULSES\_GEST \times LED\_PERIOD\_GEST \quad (4)$$

Calculate the LED period with the following equation:

$$LED\_PERIOD,\ minimum = 2 \times AFE\_WIDTH + 11 \quad (5)$$

t_A and t_B are fixed and based on the computation time for each mode. See Table 10 for the definitions of LED_OFFSET_GEST, LED_OFFSET_PROX, LED_PERIOD_GEST, LED_PERIOD_PROX, t_A, t_B, and t_{SLEEP}.

NORMAL MODE OPERATION AND DATA FLOW

In the proximity, and sample/gesture modes, the ADUX1020 follows a specific pattern set up by the state machine. This pattern follows:

1. LED pulse and sample. The ADUX1020 pulses external LEDs. The response of the optical sensor to the reflected light is measured by the ADUX1020. Each data sample is constructed from the sum of n individual pulses, where n is user configurable between 1 and 63.
2. Intersample averaging. If desired, the logic can average n samples, from 2 to 32 in powers of 2, to produce output data. New output data is saved to the output registers every N samples.
3. Data read. The host processor reads the converted results from the data register or the FIFO.
4. Repeat.

LED Pulse and Sample

At each sampling period, the LED driver drives a series of LED pulses, as shown in Figure 7. The magnitude, duration, and number of pulses are programmable over the I²C interface. Each LED pulse coincides with a sensing period so that the sensed value represents the total charge acquired on the photodiode in response to only the corresponding LED pulse. Charge, such as ambient light, that does not correspond to the LED pulse is rejected.

After each LED pulse, the sensor output relating the pulsed LED signal is sampled and converted to a digital value by the 14-bit ADC. Each subsequent conversion within a sampling period is summed with the previous result. Up to 63 pulse values from the ADC can be summed in an individual sampling period. There is a 16-bit maximum range for each sampling period.

Averaging

The ADUX1020 offers sample accumulation and averaging functionality to increase signal resolution.

Within a sampling period, the AFE can sum up to 63 sequential pulses. This accumulated data of N pulses is stored as 20-bit values and can be read out directly by using the output registers or indirectly using the FIFO configuration (only as 16-bit values).

When using the averaging feature set up by Register 0x46 (decimation), subsequent samples can be averaged in groups of powers of 2. The user can select from 2, 4, 8, 16, or 32 samples to be averaged together. Sample data is still acquired by the AFE at the sampling frequency, f_{SAMPLE} (Register 0x40), but new data is written to the registers at the rate of f_{SAMPLE}/N every N^{th} sample. This new data consists of the sum of the previous N samples. The full 20-bit sum is stored in the output registers. However, before sending this data to the FIFO, a divide by N operation occurs (bit shift). This divide operation maintains bit depth to prevent clipping of the 16-bit FIFO.

Use this between sample averaging to lower the noise while maintaining 16-bit resolution. If the pulse count registers are kept to 8 or less, the 16-bit width is never exceeded. Therefore, when using Register 0x46 to average subsequent pulses, many pulses can be accumulated without exceeding the 16-bit word width, which can reduce the number of FIFO reads required by the host processor.

Data Read

The host processor reads output data from the ADUX1020, via the I²C protocol, from the data registers or from the FIFO. New output data is made available every N samples, where N is the user configured power of 2 averaging factor. The averaging factors for proximity and sample/gesture are configurable independently of each other. If they are the same, both time slots can be configured to save data to the FIFO. If the two averaging factors are different, only one time slot can save data to the FIFO; data from the other time slot can be read from the output registers.

The data read operations are described in more detail in the Reading Data section.

AFE OPERATION

The timing within each pulse burst is important for optimizing the operation of the ADUX1020. Figure 7 shows the timing waveforms for a single time slot as an LED pulse response propagates through the analog block of the AFE. Graph A shows the ideal LED pulsed output, the filtered LED response (Graph B) shows the output of the analog integrator, and Graph C illustrates an optimally placed integration window (see Figure 7). When programmed to the optimized value, the full signal of the filtered LED response can be integrated. The AFE integration window is then applied to the output of the band-pass filter (BPF), and the result is sent to the ADC and summed for N pulses.

Table 10. LED Timing and Sample Timing Parameters

Parameter	Register	Bits	Test Conditions/Comments	Min	Typ	Max	Unit
LED_OFFSET_GEST	0x20	[5:0]	Delay from AFE power-up to LED rising edge	23		63	µs
LED_OFFSET_PROX	0x22	[5:0]	Delay from AFE power-up to LED rising edge	23		63	µs
LED_PERIOD_GEST[1]	0x21	[7:0]	Time between LED pulses in sample/gesture mode, AFE_WIDTH_GEST = 4 µs	19		63	µs
LED_PERIOD_PROX[1]	0x23	[7:0]	Time between LED pulses in proximity mode, AFE_WIDTH_PROX = 4 µs	19		63	µs
t_A			Compute time for sample/gesture mode		68		µs
t_B			Compute time for proximity mode		20		µs
t_{SLEEP}			Sleep time between sample periods	200			µs

[1] Setting the LED_PERIOD_x less than the specified minimum value can cause invalid data captures.

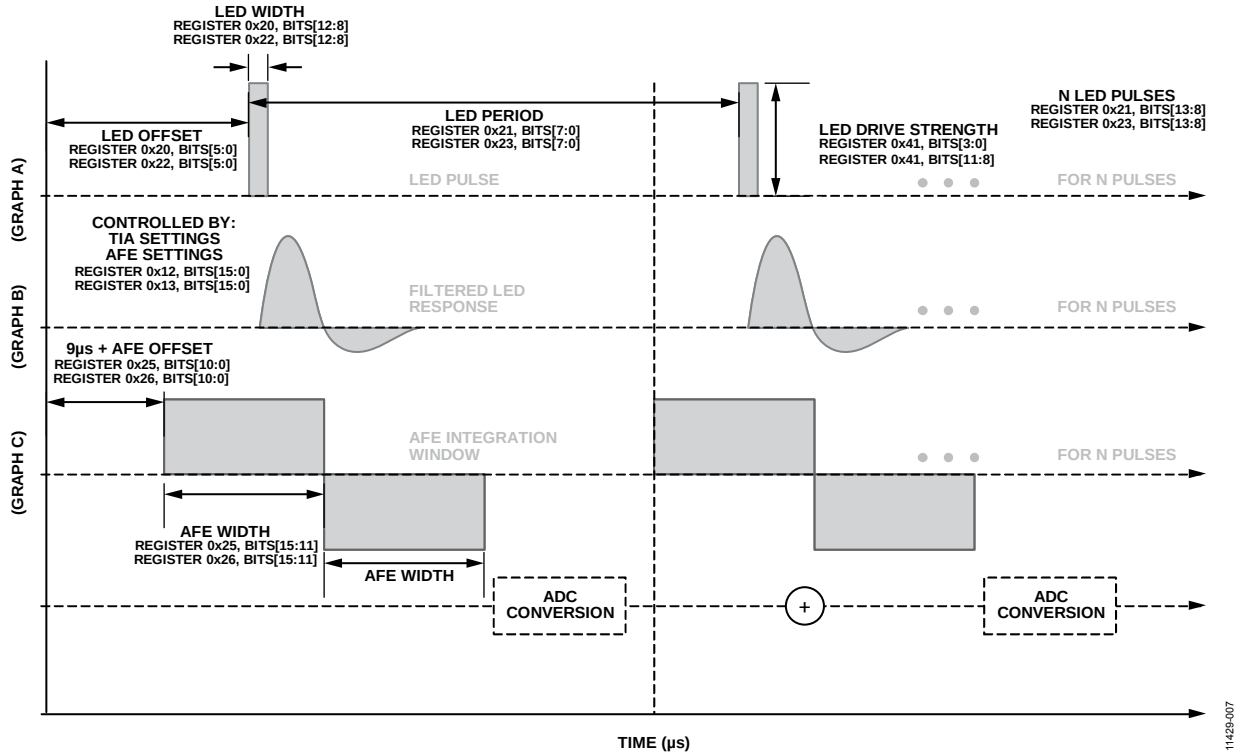

Figure 7. AFE Operation Diagram

I²C SERIAL INTERFACE

The ADUX1020 supports an I²C serial interface via the SDA (data) and the SCL (clock) pins. All internal registers are accessed through the I²C interface.

The ADUX1020 conforms to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 05—9 October 2012, available from NXP Semiconductors. It supports a fast mode (400 kbps) data transfer. Register read and write are supported, as shown in Figure 8. Figure 3 shows the timing diagram for the I²C interface.

Slave Address

The 7-bit I²C slave address for the device is 0x64, followed by the R/$\overline{W}$ bit; therefore, a write to the default I²C slave address is 0xC8 and a read to the default I²C slave address is 0xC9. The slave address is not configurable.

I²C Write and Read Operations

Figure 8 illustrates the ADUX1020 I²C write and read operations. Single-word read operations are supported. For a single register read, the host sends a no acknowledge (NACK) after the second data byte is read, and a new register address is needed for each access.

When reading from the FIFO (Register 0x60), the data is automatically advanced to the next word in the FIFO and the space is freed. All register writes are single-word only and require 16 bits (one word) of data.

The software reset (Register 0x0F, Bit 0) is the only command that does not return an ACK because the command is instantaneous.

Table 11. Definition of I²C Terminology

Term	Description
SCL	Serial clock.
SDA	Serial address and data.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by a master. The ADUX1020 operates as a slave device.
Start (S)	A high to low transition on the SDA line while SCL is high; all transactions begin with a start condition.
Start (Sr)	Repeated start condition.
Stop (P)	A low to high transition on the SDA line while SCL is high. A stop condition terminates all transactions.
ACK	During the ACK or NACK clock pulse, the SDA line is pulled low and remains low.
NACK	During the ACK or NACK clock pulse, the SDA line remains high.
Slave Address	After a start (S), a 7-bit slave address is sent, which is followed by a data direction bit (read or write).
Read (R)	A 1 indicates a request for data.
Write (W)	A 0 indicates a transmission.

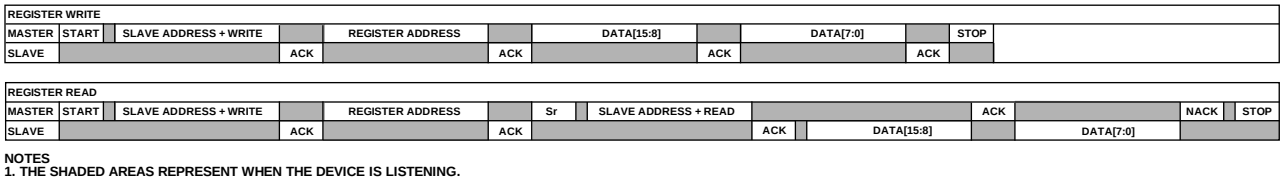

Figure 8. I²C Write and Read Operations

TYPICAL CONNECTION DIAGRAM

Figure 10 shows a typical circuit configuration using the ADUX1020. The 1.8 V I²C communication lines, SCL and SDA, along with the INT line, connect to a system microprocessor or sensor hub. The I²C signals can have pull-up resistors connected to a 1.8 V or a 3.3 V power supply. The INT signal is compatible only with a 1.8 V supply and may need a level translator.

Provide a 1.8 V supply to the VDD pin. Use the supply voltage for the LEDs (V_{LED}) for the LED supply using standard regulator circuits according to the peak current requirements specified in the Determining the Average Current section and calculated in the Calculating Current Consumption section.

For the best noise performance, connect AGND and DGND together at a large conductive surface such as a ground plane, a ground pour, or a large ground trace.

LED DRIVER PIN AND LED SUPPLY VOLTAGE

The LEDX pin has an absolute maximum voltage rating of 3.6 V. Any voltage exposure over this rating affects the reliability of the device operation and, in certain circumstances, causes the device to cease proper operation. Do not confuse the LEDX pin voltage with the supply voltage for the LEDs (V_{LED}). V_{LED} is the voltage applied to the anode of the external LED, whereas the LEDX pin is the input of the internal current driver, which must be connected to the cathode of the external LED.

LED DRIVER OPERATION

The LED driver for the ADUX1020 is a current sink requiring 0.2 V of compliance above ground to maintain the programmed current level. Figure 9 shows the basic schematic of how the ADUX1020 connects to an LED through the LED driver. The Determining the Average Current section defines the requirements for the bypass capacitor (C_{VLED}) and the supply voltages of the LEDs (V_{LED}).

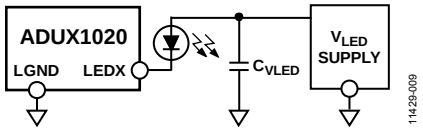

Figure 9. V_{LED} Supply Schematic

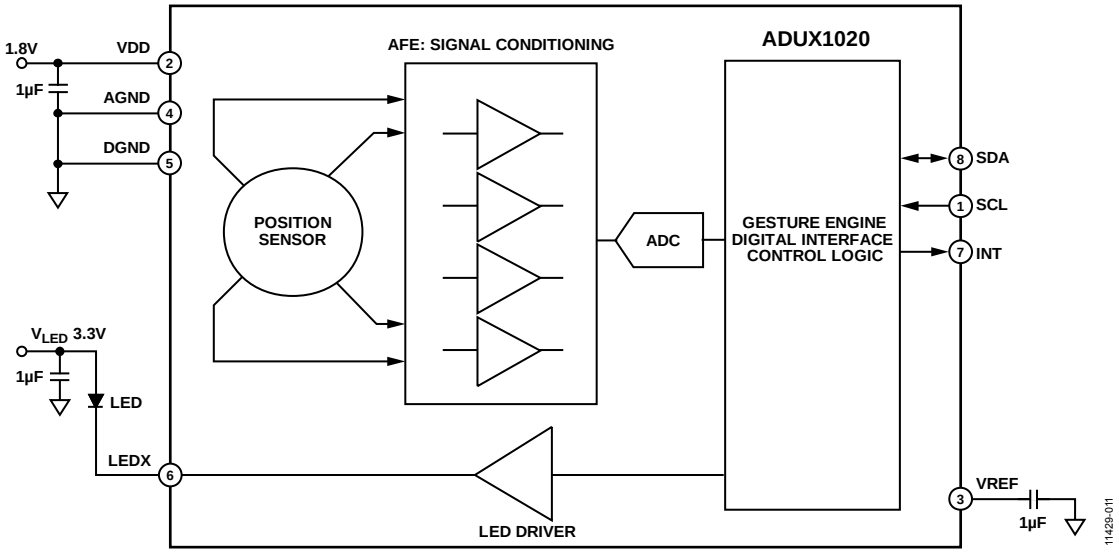

Figure 10. Typical Circuit Configuration

DETERMINING THE AVERAGE CURRENT

The ADUX1020 drives an LED in a series of short pulses. Figure 11 shows the typical ADUX1020 circuit configuration of a pulse burst sequence. In this example, the LED pulse width, t_{LED_PULSE}, is 3 µs, and the LED pulse period, t_{LED_PERIOD}, is 19 µs. The infrared LED may be driven to 250 mA peak current. The goal of C_{VLED} is to buffer the LED between individual pulses. In the worst case scenario, where the pulse train shown in Figure 11 is a continuous sequence of short pulses, the V_{LEDx} supply must supply the average current. Therefore, calculate $I_{LED\_AVERAGE}$ as follows:

$$I_{LED\_AVERAGE} = (t_{LED\_PULSE}/t_{LED\_PERIOD}) \times I_{LED\_MAX} \quad (6)$$

where:
$I_{LED\_AVERAGE}$ is the average current needed from the V_{LED} supply, and it is also the V_{LED} supply current rating.
t_{LED_PULSE} is the time the LED is pulsed on, nominally 3 µs.
t_{LED_PERIOD} is the period between LED pulses, nominally 19 µs.
I_{LED_MAX} is peak current setting of the LED.

For the numbers shown in Equation 6, $I_{LED\_AVERAGE} = 3/19 \times I_{LED\_MAX}$. For typical LED timing, the average V_{LED} supply current is 3/19 × 250 mA = 39.4 mA, indicating that the V_{LED} supply must support a dc current of 40 mA.

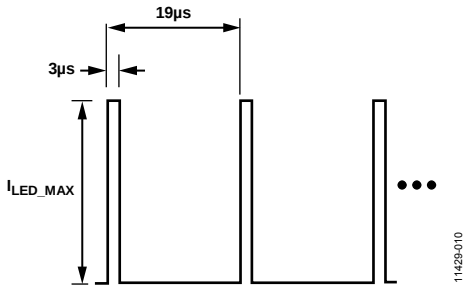

Figure 11. Typical LED Pulse Burst Sequence Configuration

LED INDUCTANCE CONSIDERATIONS

The LED driver (LEDX) on the ADUX1020 has a configurable slew rate settings (Register 0x41, Bits[6:4]) This slew rate is defined in Table 3. Even in the lowest setting, careful consideration must be taken in PCB design and layout. If a large series inductor, such as a long PCB trace, is placed between the LED cathode and the LEDX pin, voltage spikes from the switched inductor can cause violations of absolute maximum and minimum voltage on the LEDX pin during the slew portion of the LED pulse.

To verify that there are no voltage spikes on the LEDX pin due to parasitic inductance, use an oscilloscope on the LEDX pin to monitor the voltage during normal operation. Any positive spike >3.6 V may damage the device.

In addition, a negative spike ≤ −0.3 V may also damage the device.

RECOMMENDED START-UP SEQUENCE

The general power-up configuration sequence follows:

1. Check the device ID by reading the CHIP_ID value in Register 0x08, Bits[11:0], and the version value in Register 0x08, Bits[15:12].
2. Reset the device by writing 0x1 to Register 0x0F, Bit 0.
3. Load the default configuration.
4. Calibrate the clocks (see the Clocks and Timing Calibration section).

CLOCKS AND TIMING CALIBRATION

The ADUX1020 operates using two internal time bases: a 32 kHz clock sets the sample timing and internal power state machine, and a 32 MHz clock controls the timing of the internal functions such as LED pulsing and data capture. Both clocks are internally generated. Because the 32 kHz oscillator on the ADUX1020 may have up to 30% variation in frequency due to the variation of on-chip RC components, calibration is recommended to keep the error less than 2%.

Calibrating the 32 kHz Clock

The ADUX1020 provides a simple calibration procedure for both clocks. To calibrate the 32 kHz clock, take the following steps:

1. Set the projected output rate to 50 Hz by writing 0x8 to Register 0x40, Bits[3:0] and set the device to sample mode by writing 0x8 to Register 0x45, Bits[3:0].
2. Flush the I^2C FIFO by writing to Register 0x49, Bit 15.
3. Poll data from the I^2C FIFO for 3 sec.
4. Calculate the actual output rate equal to the sample set count divided by 3.
5. Adjust the 32 kHz oscillator trim value by writing to Register 0x18, Bits[5:0] with the appropriate value.
6. Repeat Step 1 through Step 5 until the actual measured output data rate is as close to 50 Hz as possible. If the output data rate is below 50 Hz, increment the trim value, and if it is above 50 Hz, decrement the trim value.

If a microprocessor is connected to the ADUX1020, the 32 kHz clock can reference to the microprocessor timer. In this case, the output rate can be set to 800 Hz, and the overall time for the clock calibrate is reduced. In general, one to three iterations can have the clock calibrated. It is equivalent to approximately 0.5 sec to 1.5 sec.

Use the following steps to calibrate the 32 kHz clock by referencing the timer of the controlling microprocessor. Do not set the I²C output rate to a speed that overloads the I²C FIFO. If the microprocessor is fully available for handling clock calibration operation at this time, and its I²C speed is set to 400 kHz, the I²C throughput will be more than 2 kHz.

1. Set the projected output rate to 820 Hz by writing 0x1C to Register 0x44.
2. Set up and run the device in sample mode by writing 0x8 to Register 0x45, Bits[3:0].
3. Flush the I²C FIFO by writing Register 0x49, Bit 15.
4. Poll data from I²C FIFO for 0.5 sec by repeatedly reading Register 0x60. Count the number of sample sets for 1 sec.
5. Calculate the actual output rate equal to the sample set count divided by 0.5.
6. Adjust the 32 kHz oscillator trim value by writing to Register 0x18, Bits[3:0] with the appropriate value.
7. Repeat Step 1 through Step 5 until the actual measured output data rate is as close to 820 Hz as possible. If the output data rate is below 820 Hz, increment the trim value, and if it is above 820 Hz, decrement the trim value.

Calibrating the 32 MHz Clock

The 32 MHz oscillator on the ADUX1020 may also have up to 30% variation in frequency due to the variation of on-chip RC components. Use the following steps to calibrate the 32 MHz clock by comparing it with the 32 kHz clock.

1. Enable the 32 kHz oscillator by writing Register 0x18, Bit 7.
2. Enable the 32 MHz oscillator by writing Register 0x32, Bit 3 and Bit 11.
3. Enable clock calibration by writing Register 0x30, Bit 5.
4. Read the calibration result from Register 0x0A, Bits[11:0].
5. Compare the calibration result. The calibration is complete when the result read is as close as possible to the optimal value of 2000. If it is not, increment the trim value if the result is below 2000, or decrement if it is above 2000. Write the new trim value and then write 1 to Register 0x30, Bit 5. Note that typically two trim values produce calibration results that straddle the optimal result. Choose the closest.
6. Write the new trim value in Register 0x1A, Bits[7:0].
7. Disable calibration by writing 0 to Register 0x30, Bit 5.

READING DATA

The ADUX1020 provides multiple methods for accessing the sample data. Interrupt signaling is available to simplify timely data access. The FIFO is available to loosen the system timing requirements for data accesses.

Reading Data Using the FIFO

The ADUX1020 includes a 64-byte FIFO memory buffer that can store data from either sample/gesture mode or proximity mode. Register 0x45, Bits[7:4] select the kind of data to be written to the FIFO. Data packets are written to the FIFO at the output data rate.

$$Output\ Data\ Rate = f_{SAMPLE}/N$$

where:

f_{SAMPLE} is the sampling frequency.

N is the averaging factor for sample/gesture mode or proximity mode. A data packet for the FIFO consists of a complete sample for either proximity mode or sample/gesture mode. In proximity mode, the device can store either only intensity i data as 2 bytes or x, y, and i data as 6 bytes. In sample/gesture mode, the device always sends 4 bytes to the FIFO.

To ensure that data packets are intact, new data is written only to the FIFO if there is sufficient space for a complete packet. Any new data that arrives when there is not enough space is lost. The FIFO continues to store data when sufficient space exists. Always read FIFO data in complete packets to ensure that data packets remain intact.

The number of bytes currently stored in the FIFO is available in Register 0x49, Bits[14:8]. A dedicated FIFO interrupt is also available and automatically generates when a specified amount of data is written to the FIFO.

To read data from the FIFO using an interrupt-based method, use the following procedure:

1. In standby mode, set the configuration of sample/gesture or proximity mode as desired for operation.
2. Write to Register 0x45, Bits[7:4] with the desired data format for each mode.
3. Set FIFO_TH in Register 0x1F, Bits[11:8] to the interrupt threshold. A good value for this is the number of 16-bit words in a data packet minus 1, which causes an interrupt to generate when at least one complete packet is in the FIFO.
4. Enable the FIFO interrupt by writing INT_MASK, Register 0x48, Bits[7:0]. Also, configure the interrupt pin (INT) by writing the appropriate value to Register 0x1C, Bit 2.
5. Enter sample/gesture or proximity mode by setting Register 0x45, Bits[3:0] to the desired value.
6. When an interrupt occurs, the following results:
    a. Note that there is no requirement to read the FIFO_STATUS register because the interrupt is generated only if there is one or more full packets. Optionally, the interrupt routine can check for the presence of more than one available packet by reading this register.
    b. Force the 32 MHz clock on by writing 0x0F4F to Register 0x32.
    c. Read a complete packet using one or more multiword accesses using Register 0x60. Reading the FIFO automatically frees the space for new samples.
    d. Set the 32 MHz clock to be controlled by the internal state machine by writing 0x40 to Register 0x32.

The interrupt automatically clears when enough data is read from the FIFO to bring the data level below the threshold.

To read data from the FIFO in a polling method, use the following procedure:

1. In standby mode, set the configuration of gesture/sample mode or proximity mode as desired for operation.
2. Write Register 0x45, Bits[7:4] with the desired data format.
3. Enter proximity or sample/gesture mode by setting Register 0x45, Bits[3:0] to the desired setting.

Next, begin the polling operations, by taking the following steps:

1. Wait for the polling interval to expire.
2. Read the FIFO_STATUS bits (Register 0x49, Bits[15:8]).
3. If FIFO_STATUS is greater than or equal to the packet size, read a packet using the following steps:
   a. Force the 32 MHz clock on by writing 0x0F4F to Register 0x32.
   b. Read a complete packet using one or more multiword accesses using Register 0x60. Reading the FIFO automatically frees the space for new samples.
   c. Set the 32 MHz clock to be controlled by the internal state machine by writing 0x0040 to Register 0x32.
4. When a mode change is required, or any other disruption to normal sampling is necessary, clear the FIFO. Use the following procedure to clear the state and empty the FIFO:
   a. Enter idle mode by setting Register 0x45, Bits[3:0] to 0xF.
   b. Force the 32 MHz clock on by writing 0x0F4F to Register 0x32.
   c. Write 1 to Register 0x49, Bit 15.
   d. Write 0x40 to Register 0x32 to set the 32 MHz clock to be controlled by the internal state machine.

Reading Data from Registers Using Interrupts

The latest sample data is always available in the data registers and is updated simultaneously at the end of each time slot. The data value for each photodiode channel is available as a 16-bit value in Register 0x00 through Register 0x03 (READX1, READX2, READY1, and READY2) for sample/gesture mode, and Register 0x04 through Register 0x06 (SAMPLEI, SAMPLEX, and SAMPLEY) for proximity mode. If allowed to reach their maximum value, Register 0x00 through Register 0x06 clip. Sample interrupts are available to indicate when the registers are updated and can be read. To use the interrupt for a given time slot, use the following procedure:

1. Enable the sample interrupt by writing a 0 to the appropriate bit in Register 0x48.
2. Configure the interrupt pin by writing the appropriate value to the bits in Register 0x1C.
3. An interrupt generates when the data registers are updated.
4. The interrupt handler must perform the following:
   a. Read Register 0x49 and observe Bits[7:0] to confirm which interrupt has occurred. This step is not required if only one interrupt is in use.
   b. Read the data registers before the next sample can be written. The system must have interrupt latency and service time short enough to respond before the next data update based on the output data rate.
   c. Write 0x0 to Bits[7:0] in Register 0x49 to clear the interrupt.

CALCULATING CURRENT CONSUMPTION

The current consumption of the ADUX1020 depends on the user selected operating configuration, as described in the Equation 7, Equation 8, and Equation 9.

Total Power Consumption

To calculate the total power consumption, use Equation 7.

$$Total\ Power = I_{VDD\_AVG} \times V_{DD} + I_{LED\_AVG} \times V_{LED} \quad (7)$$

where:
I_{VDD_AVG} is the V_{DD} average.
V_{DD} is the ADUX1020 supply voltage.
I_{LED_AVG} is the average LED current.
V_{LED} is the LED supply voltage.

Average V_{DD} Supply Current

To calculate the average V_{DD} supply current, use Equation 8.

$$I_{VDD\_AVG} = DR \times (I_{AFE} \times t_{MODE} + I_{PROC}) + I_{VDD\_STANDBY} \quad (8)$$

where:
DR is the data rate in Hz.
$I_{AFE} = 8.9 + (LED_{PEAK} - 25)/225$, where LED_{PEAK} is the peak LED current expressed in mA.
t_{MODE} = LED_OFFSET_x + LED_PERIOD_x × PULSE_COUNT_x. Note that LED_OFFSET_x is the pulse start time offset expressed, LED_PERIOD_x is the pulse period expressed in seconds, PULSE_COUNT_x is the number of pulses, and x is either PROX or GEST depending on the mode of operation.
I_{PROC} is an average current associated with the processing time. For sample/gesture mode, $I_{PROC} = 0.64 \times 10^{-3}$, and for proximity mode, $I_{PROC} = 0.51 \times 10^{-3}$.
$I_{VDD\_STANDBY} = 3.5 \times 10^{-3}$ mA.

Average V_{LEDA} Supply Current

To calculate the average V_{LED} supply current, use Equation 9.

$$I_{LED\_AVG} = (LED\_WIDTH/1 \times 10^6) \times LED_{PEAK} \times DR \times PULSE\_COUNT \quad (9)$$

where:
LED_WIDTH is the on time for the LED pulse, in µs.
PULSE_COUNT is the number of LED pulses per sample.

Tuning the Pulse Count

After the LED peak current and TIA gain are optimized, increasing the number of pulses per sample increases the SNR by the square root of the number of pulses. There are two ways to increase the pulse count. The pulse count registers (Register 0x21, Bits[13:8] for sample/gesture mode, and Register 0x23, Bits[13:8] for proximity mode) change the number of pulses per internal sample. Register 0x46, Bits[6:4] for sample/gesture mode and Bits[2:0] for proximity mode controls the number of internal samples that are averaged together before the data is sent to the output. Therefore, the number of pulses per sample is the pulse count register multiplied by the number of subsequent samples being averaged.

In general, the internal sampling rate increases as the number of internal sample averages increase to maintain the desired output data rate. The SNR/Watt is most optimal with pulse count values of 16 or less. Above pulse count values of 16, the square root relationship does not hold in the pulse count register. However, this relationship continues to hold when averaged between samples using Register 0x46.

Note that increasing LED peak current increases SNR almost directly proportional to LED power, whereas increasing the number of pulses by a factor of n results in only a nominal√(n) increase in SNR.

When using the sample sum/average function (Register 0x46), the output data rate decreases by the number of summed samples. To maintain a static output data rate, increase the sample frequency (Register 0x40, Bits[3:0] for sample/gesture mode, Bits[7:4] for proximity mode) by the same factor as that selected in Register 0x46. For example, for a 100 Hz output data rate and a sample sum/average of four samples, set the sample frequency to 400 Hz.

RECOMMENDED SOLDERING PROFILE

Figure 12 and Table 12 provide details about the recommended soldering profile.

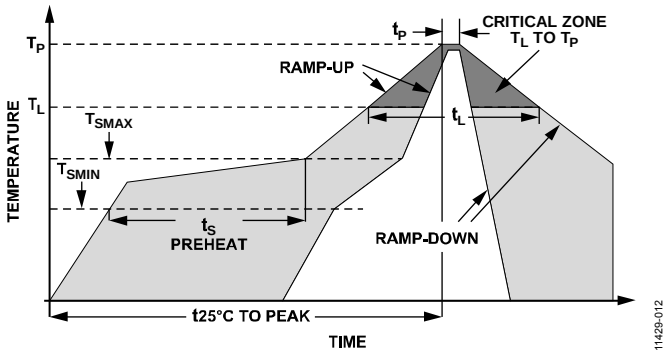

Figure 12. Recommended Soldering Profile

Table 12. Recommended Soldering Profile

Profile Feature	Condition (Pb-Free)
Average Ramp Rate (T_L to T_P)	3°C/sec maximum
Preheat	
Minimum Temperature (T_{SMIN})	150°C
Maximum Temperature (T_{SMAX})	200°C
Time (T_{SMIN} to T_{SMAX}) (t_S)	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec maximum
Time Maintained Above Liquidous Temperature	
Liquidous Temperature (T_L)	217°C
Time (t_L)	60 sec to 150 sec
Peak Temperature (T_P)	+260 (+0/−5)°C
Time Within 5°C of Actual Peak Temperature (t_P)	<30 sec
Ramp-Down Rate	6°C/sec maximum
Time from 25°C to Peak Temperature ($t_{25°C\ TO\ PEAK}$)	8 minutes maximum

COMPLETE REGISTER LISTING

Table 13. Data Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x00	[15:0]	0x0	SCK	Read only	READX1	X1 value
0x01	[15:0]	0x0	SCK	Read only	READX2	X2 value
0x02	[15:0]	0x0	SCK	Read only	READY1	Y1 value
0x03	[15:0]	0x0	SCK	Read only	READY2	Y2 value
0x04	[15:0]	0x0	SCK	Read only	SAMPLEI	I value
0x05	[15:0]	0x0	SCK	Read only	SAMPLEX	X value
0x06	[15:0]	0x0	SCK	Read only	SAMPLEY	Y value
0x07	[15:0]	0x20	SCK	Read only	Reserved	Write 0x20

Table 14. System Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x08	[11:0]	0x3FC	SCK	Read only	CHIP_ID	Reset by none
	[15:12]	0x0	SCK	Read only	Version	Reset by none
0x09	[6:0]	0xC8	SCK	Read only	SLAVE_ADDRESS	I^2C slave address; reset by none
	[15:7]	0x0	SCK	Read only	Reserved	Write 0x0

Table 15. Timer Test Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x0A	[11:0]	0x0	SCK	Read only	OSC_CAL_OUT	Counter value of 2 cycle, 32 kHz pulses with 32 MHz clock
	[15:12]	0x0	SCK	Read only	Reserved	Write 0x0
0x0C	[4:0]	0xF	SCK	Read/write	Reserved	Write 0xF
	[15:5]	0x0	SCK	Read/write	Reserved	Write 0x0

Table 16. Reset Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x0F	0	0x0	SCK	Read/write	SW_RESET	Software reset
	[15:1]	0x0	SCK	Read/write	Reserved	Write 0x0

Table 17. ADC Control Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x10	[15:0]	0x1010	SCK	Read/write	Reserved	Write 0x1010
0x11	[15:0]	0x004c	SCK	Read/write	Reserved	Write 0x004C

Table 18. AFE Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x12	[1:0]	0x0	SCK	Read/write	AFE_TRIM_TIA	Transimpedance amplifier gain (feedback resistor) select. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ.
	[3:2]	0x2	SCK	Read/write	AFE_TRIM_BPF	Sets the pole locations of the band-pass filter. 0: 50 kHz and 100 kHz. 1: 50 kHz and 300 kHz. 2: 100 kHz and 100 kHz. 3: 100 kHz and 300 kHz.
	[5:4]	0x0	SCK	Read/write	AFE_TRIM_VREF	Sets the reference voltage (V_{REF}) for the TIA. 0: (13/16) × V_{DD}. 1: (12/16) × V_{DD}. 2: (15/16) × V_{DD}. 3: (14/16) × V_{DD}.
	[6:7]	0x0	SCK	Read/write	Not applicable	Reserved.
	[12:8]	0x1C	SCK	Read/write	AFE_TRIM_INT	Integrator register and capacitor select bits. The upper three bits select the integrator capacitor, C_{FB}. C_{FB} = 3.62 pF × Bit 12 + 1.81 pF × Bit 11 + 0.9 pF × Bit 10. The lower two bits select the integrator resistor, R_{IN}. R_{IN} = 200 kΩ (Bits[9:8] = 0x00),100 kΩ (Bits[9:8] = 0x01), and 50 kΩ (Bits[9:8] = 0x10 or 0x11).
	[14:13]	0x0	SCK	Read/write	Reserved	Write 0x0.
	15	0x0	SCK	Read/write	Not applicable	Reserved.
0x13	[15:0]	0xADA5	SCK	Read/write	AFE_MUX_TEST	AFE internal connection bypass selection. 0xADA5: analog full path mode (TIA → BPF → INT → ADC). 0xB065: TIA ADC mode (TIA → ADC).

Table 19. Reference/Bias Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x14	[15:0]	0x80	SCK	Read/write	Reserved	Write 0x80
0x16	[6:0]	0x0	SCK	Read/write	Reserved	Write 0x0
	[11:7]	0xC	SCK	Read/write	LED_TRIM	Used to trim the amount of current being multiplied by the LED driver: ILED = (21.25 + 0.3125 × (Register Value))/25
	[15:12]	0x0	SCK	Read/write	Reserved	Write 0x0

Table 20. Oscillator Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x18	[5:0]	0x20	SCK	Read/write	OS32K_TRIM	32 kHz oscillator trim. 0x00: maximum frequency. 0x20: default frequency. 0x3F: minimum frequency.
	6	0x0	SCK	Read/write	Reserved	Write 0x0.
	7	0x0	SCK	Read/write	OS32K_PDB	32 kHz oscillator power down (low active). 0: power down. 1: normal operation.
	8	0x0	SCK	Read/write	OS32K_BYPASS	Bypass 32 kHz oscillator. 0: normal operation. 1: external clock (TCLI).
	[13:9]	0x1B	SCK	Read/write	Reserved	Write 0x1B.
	14	0x0	SCK	Read/write	OS32K_TEST4	32 kHz oscillator frequency range. 0: normal. 1: increased frequency range.
	15	0x0	SCK	Read/write	Reserved	Write 0x0.
0x19	[1:0]	0x0	SCK	Read/write	OS32M_BYPASS	Bypass 32 MHz oscillator. 0: normal operation. 1: external clock (TCLI).
	[4:2]	0x1	SCK	Read/write	Reserved	Write 0x1.
	[15:5]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x1A	[7:0]	0x5E	SCK	Read/write	OS32M_VTRIM	VCO trim. 0000 0000: minimum frequency. 0101 1110: default frequency (32 MHz). 1111 1111: maximum frequency.
	[14:8]	0x42	SCK	Read/write	OS32M_RTRIM	V_{REF} resistor temperature compensation proportional to absolute temperature (PTAT). 000 0000: minimum PTAT current. 100 0010: default PTAT current. 111 1111: maximum PTAT current.
	15	0x0	SCK	Read/write	Reserved	Write 0x0.

Table 21. ADC Post Processing Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x1B	[4:0]	0x0	SCK	Read/write	Reserved	Write 0x0
	5	0x0	SCK	Read/write	ADC_SPACING	Insert 1 cycle spacing between ADC samples
	[11:6]	0x0	SCK	Read/write	Reserved	Write 0x0
	[15:12]	0x0	SCK	Read/write	Reserved	Write 0x0

Table 22. Miscellaneous Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x1C	0	0x0	SCK	Read/write	Reserved	Write 0x0.
	1	0x0	SCK	Read/write	INT_IE	Interrupt (INT) pin input enable.
	2	0x0	SCK	Read/write	INT_OE	Interrupt (INT) pin output enable. 0: disable INT pin drive. 1: enable drive according to INT_POL polarity and open-drain (OD) value.
	4	0x1	SCK	Read/write	SDA_SLOPE_EN	SDA pad slope control. 0: SDA/SCL pad slew rate limiter disabled. 1: SDA/SCL pad slew rate limiter enabled (default).
	5	0x0	SCK	Read/write	TCLI_IE	Test mode only, reserved.
	6	0x0	SCK	Read/write	TCLI_OE	Test mode only, reserved.
	[14:7]	0x41	SCK	Read/write	Reserved	Write 0x41.
	15	0x0	SCK	Read/write	INT_PMOS_OEN	Interrupt (INT) pin PMOS output enable. 0: output driver enable controlled by INT_OE (default). 1: output driver disabled regardless of INT_OE.
0x1D	[4:0]	0x0	SCK	Read/write	Reserved	Write 0x0.
	5	0x0	SCK	Read/write	INT_POL	Interrupt (INT) pin polarity. 0: active high. 1: active low.
	[15:6]	0x0	SCK	Read/write	Reserved	Write 0x0.

Table 23. I²C Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x1E	[11:0]	0x1	SCK	Read/write	I2C_CTL	Configure I²C to proper operation mode. 0: reserved. 1: start condition followed by a matching address, an interrupt generates if this is asserted. 2: start condition followed by a matching address followed by a repeated start, an interrupt generates if this is asserted. 3: NACK. If set, the next communication is a NACK. 4: stop condition detected interrupt enable. 5: reserved. 6: transmit request interrupt enable. (If asserted and an I²C read transaction is in progress, and the transmit FIFO is not full, an interrupt generates.) 7: When set to 1, FIFO stores the higher byte first, and when set to 0, FIFO stores lower byte first. 8: set 0. 9: set 0. 10: when set to 1, I²C writes to the lower byte first, and when set to 0, I²C writes to higher byte first. 11: set 0.
	12	0x0	SCK	Read/write	SPEED_MODE	I²C speed mode. 0 = 400 kHz fast mode. 1 = 3.4 MHz high speed.
	[15:13]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x1F	[7:0]	0x0	SCK	Read/write	Reserved	Write 0x0.
	[11:8]	0x0	SCK	Read/write	FIFO_TH	Minimum FIFO words to trigger interrupt.

Table 24. LED Control Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x20	[5:0]	0x0	SCK	Read/write	LED_OFFSET_GEST	LED pulse offset (in 1 µs step) for sample/gesture mode.
	[7:6]	0x0	SCK	Read/write	Reserved	Write 0x0.
	[12:8]	0x1	SCK	Read/write	LED_WIDTH_GEST	LED pulse width (in 1 µs step) for sample/gesture mode.
	[15:9]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x21	[7:0]	0x8	SCK	Read/write	LED_PERIOD_GEST	LED pulse period (in 1 µs step) for sample/gesture mode.
	[13:8]	0x1	SCK	Read/write	LED_PULSES_GEST	LED pulse count for sample/gesture mode.
	[15:9]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x22	[5:0]	0x0	SCK	Read/write	LED_OFFSET_PROX	LED pulse offset (in 1 µs step) for proximity mode.
	[15:9]	0x0	SCK	Read/write	Reserved	Write 0x0.
	[12:8]	0x1	SCK	Read/write	LED_WIDTH_PROX	LED pulse width (in 1 µs step) for proximity mode.
	[15:9]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x23	[7:0]	0x8	SCK	Read/write	LED_PERIOD_PROX	LED pulse period (in 1 µs step) for proximity mode.
	[13:8]	0x1	SCK	Read/write	LED_PULSES_PROX	LED pulse count for proximity mode.
	[15:9]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x24	[7:0]	0x0	SCK	Read/write	Reserved	Write 0x0.
	8	0x0	SCK	Read/write	LED_MASK	LED masking signal. 0: disable. 1: enable.
	9	0x0	SCK	Read/write	Reserved	Write 0x0.
	[15:10]	0x0	SCK	Read/write	Reserved	Write 0x0.

Table 25. AFE Control Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x25	[4:0]	0x0	SCK	Read/write	AFE_FINE_OFFSET_GEST	AFE integration window, fine offset (in 31.25 ns step) for sample/gesture mode.
	[10:5]	0x0	SCK	Read/write	AFE_OFFSET_GEST	AFE integration window, coarse offset (in 1 µs step) for sample/gesture mode.
	[15:11]	0x1	SCK	Read/write	AFE_WIDTH_GEST	AFE integration window width (in 1 µs step) for sample/gesture mode.
0x26	[4:0]	0x0	SCK	Read/write	AFE_FINE_OFFSET_PROX	AFE integration window, fine offset (in 31.25 ns step) for proximity mode.
	[10:5]	0x0	SCK	Read/write	AFE_OFFSET_PROX	AFE integration window, coarse offset (in 1 µs step) for proximity mode.
	[15:11]	0x1	SCK	Read/write	AFE_WIDTH_PROX	AFE integration window width (in 1 µs step) for proximity mode.
0x27	0	0x0	SCK	Read/write	AFE_MASK	Mask bit for AFE clock. 0: disable masking. 1: enable masking.
	1	0x0	SCK	Read/write	AFE_MULTI_SAMPLE	Multisample mode enable bit. 0: single sample mode. 1: multiple sample mode.
	[6:2]	0x0	SCK	Read/write	Reserved	Write 0x0.
	[15:7]	0x0	SCK	Read/write	Reserved	Write 0x0.

Table 26. Sample/Gesture and Proximity Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x28	[15:0]	0x0	SCK	Read/write	GEST_DI_TH	di/dt threshold.
0x29	[2:0]	0x0	SCK	Read/write	ORIENTATION	Orientation control. 0: when set to 1, flip sign of x direction. 1: when set to 1, flip sign of y direction. 2: when set to 1, swap X0 and Y0, and X1 and Y1.
	[7:3]	0x0	SCK	Read/write	Reserved	Write 0x0.
	[15:8]	0x0	SCK	Read/write	GEST_N_PTS	Minimum length of valid gesture.
0x2A	[15:0]	0x0	SCK	Read/write	PROX_TH_ON1	Bits[15:0] of proximity ON1 threshold.
0x2B	[15:0]	0x0	SCK	Read/write	PROX_TH_OFF1	Bits[15:0] of proximity OFF1 threshold.
0x2C	[15:0]	0x0	SCK	Read/write	PROX_TH_ON2	Bits[15:0] of proximity ON2 threshold.
0x2D	[15:0]	0x0	SCK	Read/write	PROX_TH_OFF2	Bits[15:0] of proximity OFF2 threshold.
0x2E	[5:0]	0x0	SCK	Read/write	PROX_TH_ON1_HIGH	Bits[21:16] of proximity ON1 threshold.
	[12:6]	0x0	SCK	Read/write	Reserved	Write 0x0.
	[13:8]	0x0	SCK	Read/write	PROX_TH_OFF1_HIGH	Bits[21:16] of proximity OFF1 threshold.
	[15:14]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x2F	[5:0]	0x0	SCK	Read/write	PROX_TH_ON2_HIGH	Bits[21:16] of proximity ON2 threshold.
	[12:6]	0x0	SCK	Read/write	Reserved	Write 0x0.
	[13:8]	0x0	SCK	Read/write	PROX_TH_OFF2_HIGH	Bits[21:16] of proximity OFF2 threshold.
	14	0x0	SCK	Read/write	Reserved	Write 0x0.
	15	0x0	SCK	Read/write	PROX_TYPE	Proximity trigger type. 0: trigger when i crosses the threshold. 1: trigger when i is above or below the threshold.

Table 27. Test Modes Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x30	[3:0]	0x0	SCK	Read/write	TEST_MODE	Test mode setting. 0: normal INT pin function 1: observe 32 kHz oscillator (OS32K) on INT pin. 2: observe 32 MHz oscillator (OS32M) on INT pin. 3: observe OS32M/(2^{16}) on INT pin. 4: observe OS32K/(2^{11}) on INT pin. Others: normal function.
	4	0x0	SCK	Read/write	Reserved	Write 0x0.
	5	0x0	SCK	Read/write	OSC32M_CAL_EN	OS32M calibration enable.
	[14:6]	0x0	SCK	Read/write	Reserved	Write 0x0.
	15	0x0	SCK	Read/write	Reserved	Write 0x0.
0x32	[6:0]	0x40	SCK	Read/write	R_PD_FORCE	Power down control force mode. Each bit controls a component. 0: bias. 1: band gap (BG). 2: reference (REF). 3: OS32M oscillator. 4: LED. 5: ADC. 6: AFE. If set to 0, the power control comes from the state machine, and if set to 1, the power control comes from Register 0x32 (except for Bit 6, AFE). When Bit 6 (AFE) is set to 1, the power down control signals come from the internal AFE control logic.

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
	7	0x0	SCK	Read only	R_DEV_CONFIG_ENABLE	Device slave address configure enable. 0: slave address (I^2C) = 0x64, fixed. 1: not available.
	8	0x0	SCK	Read/write	R_BIAS_PDB	Power down of bias distribution (0 is power on).
	9	0x0	SCK	Read/write	R_BG_PDB	Power down of band gap (0 is power on).
	10	0x0	SCK	Read/write	R_REF_PDB	Power down of REF (0 is power on).
	11	0x0	SCK	Read/write	R_OS32M_PDB	Power down of OS32M (0 is power on).
	12	0x0	SCK	Read/write	R_LED_PDB	Power down of LED driver (0 is power on).
	13	0x0	SCK	Read/write	R_ADC_PDB	Power down of ADC (0 is power on).
	[15:14]	0x0	SCK	Read/write	Reserved	Write 0x0.

Table 28. AFE Channel Compensation Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x38	[7:0]	0x80	SCK	Read/write	GAIN1	AFE Channel 1 gain. Unsigned gain code x.xxx_xxxx, supports gain from 0/128 to 255/128.
	[15:8]	0x80	SCK	Read/write	GAIN2	AFE Channel 2 gain. Unsigned gain code x.xxx_xxxx, support gain from 0/128 to 255/128.
0x39	[7:0]	0x80	SCK	Read/write	GAIN3	AFE Channel 3 gain. Unsigned gain code x.xxx_xxxx, support gain from 0/128 to 255/128.
	[15:8]	0x80	SCK	Read/write	GAIN4	AFE Channel 4 gain. Unsigned gain code x.xxx_xxxx, support gain from 0/128 to 255/128.
0x3A	[13:0]	0x2000	SCK	Read/write	CH1_OFFSET	Default: 0x2000, which is the offset of ADC output.
	[15:14]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x3B	[13:0]	0x2000	SCK	Read/write	CH2_OFFSET	Default: 0x2000, which is the offset of ADC output.
	[15:14]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x3C	[13:0]	0x2000	SCK	Read/write	CH3_OFFSET	Default: 0x2000, which is the offset of ADC output.
	[15:14]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x3D	[13:0]	0x2000	SCK	Read/write	CH4_OFFSET	Default: 0x2000, which is the offset of ADC output.
	[15:14]	0x0	SCK	Read/write	Reserved	Write 0x0.

Table 29. Sample Rate Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x3E	[15:0]	0x0	SCK	Read/write	SLOPE_TH	Slope threshold used in x/y direction detection. If absolute value (dx) + absolute value (dy) < SLOPE_TH, gesture is z direction movement.
0x40	[3:0]	0xA	SCK	Read/write	GEST_FREQ	Sample rate in sample/gesture mode. 0: 0.1 Hz. 1: 0.2 Hz. 2: 0.5 Hz. 3: 1 Hz. 4: 2 Hz. 5: 5 Hz. 6:10 Hz. 7: 20 Hz. 8: 50 Hz. 9: 100 Hz. 10: 190 Hz. 11: 450 Hz. 12: 820 Hz. 13: 1400 Hz.

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
	[7:4]	0x6	SCK	Read/write	PROX_FREQ	Sample rate in proximity mode. 0: 0.1 Hz. 1: 0.2 Hz. 2: 0.5 Hz. 3: 1 Hz. 4: 2 Hz. 5: 5 Hz. 6: 10 Hz. 7: 20 Hz. 8: 50 Hz. 9: 100 Hz. 10: 190 Hz. 11: 450 Hz. 12: 820 Hz. 13: 1400 Hz.
	11	0x0	SCK	Read/write	IOUT_MODE	I output mode. 0: output lower 16 bits of internal i. 1: output higher 16 bits of internal i.
	[15:12]	0x0	SCK	Read/write	GEST_DIDT_M	M used for I(n) − I(n − m).

Table 30. LED Driver Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x41	[3:0]	0x0	SCK	Read/write	LED_IREF	LED driver current. 0: 25 mA. 1: 40 mA. 2: 55 mA. 3: 70 mA. 4: 85 mA. 5: 100 mA. 6: 115 mA. 7: 130 mA. 8: 145 mA. 9: 160 mA. 10: 175 mA. 11: 190 mA. 12: 205 mA. 13: 220 mA. 14: 235 mA. 15: 250 mA.
	[6:4]	0x0	SCK	Read/write	LED_ITAIL	Slew rate control.
	[7:5]	0x0	SCK	Read/write	Reserved	Write 0x0.
	[11:8]	0x0	SCK	Read/write	LED_PIREF	LED driver current for proximity mode.
	12	0x1	SCK	Read/write	LED_PIREF_EN	LED driver current for proximity enable. 0: use LED_IREF, Bits[3:0] for proximity mode. 1: use LED_PIREF, Bits[11:8] for proximity mode (default).
	[15:13]	0x0	SCK	Read/write	Reserved	Write 0x0.

Table 31. Operation Control Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x42	[7:0]	0x0	SCK	Read/write	REF_TIME	REF start-up time.
	[11:8]	0x0	SCK	Read/write	OS32M_TIME	Fast oscillator start-up time.
	[15:12]	0x4	SCK	Read/write	DIGITAL_TIME	Digital operation time.
0x43	[3:0]	0x0	SCK	Read/write	AFE_TIME	AFE operation time in 32 kHz period.
	[15:4]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x44	[15:0]	0x0	SCK	Read/write	DSAMPLE_TIME	System data sampling time ((100 + LED_PULSES_GEST × LED_PERIOD_GEST)/31.3 + 1).
0x45	[3:0]	0x0	SCK	Read/write	OP_MODE	Operation mode. 0: standby mode (every block is in power saving mode). 1: proximity mode. 2: gesture mode (unused). 3: sample mode. Set to 0xF, which is idle mode (BG/REF/bias are on, see Register 0x32, and other blocks are in power saving mode).
	[7:4]	0x0	SCK	Read/write	DATA_OUT_MODE	FIFO format in proximity mode (OP_MODE = 1). 1: store i in the FIFO, which takes 2 bytes. 3: store x, y, and i in the FIFO, which takes 6 bytes. Others: store none in the FIFO. However, in sample/gesture mode (OP_MODE = 2), store 4 bytes in the FIFO.
	8	0x0	SCK	Read/write	FIFO_PREVENT_EN	Prevent FIFO overrun enable. 0: write data into the FIFO. 1: write data into the FIFO when the FIFO has enough space, and drop the whole package if the FIFO does not have enough space for the whole package.
	9	0x0	SCK	Read/write	PACK_START_EN	Indicate package start in FIFO data. 0: normal operation. 1: replace the LSB of the first data of the package into the FIFO to 1, and replace the other data of the package into the FIFO with 0.
	10	0x0	SCK	Read/write	PROX_AUTO_GESTURE	Control of automatic switching from proximity mode to sample/gesture mode. 0: normal operation (no mode switching). 1: when OP_MODE = 1 (proximity mode), the ON2 interrupt triggers an OP_MODE switch from proximity mode to sample/gesture mode after the interrupt is asserted and FIFO storing is done.
	11	0x0	SCK	Read/write	Reserved	Write 0x0.
	12	0x0	SCK	Read/write	SAMP_OUT_MODE	Output mode for sample mode. 0: output every sample. 1: output sample between gesture start and gesture end.
	13	0x0	SCK	Read/write	RDOUT_MODE	Readback data mode. 0: with decimation. 1: no decimation.
	[15:14]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x46	[2:0]	0x0	SCK	Read/write	PROX_DEC_MODE	Decimation rate for proximity mode. 0: 1. 1: 2. 2: 4. 3: 8. 4: 16. 5: 32. Others: 32.

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
	[5:3]	0x0	SCK	Read/write	Reserved	Write 0x0.
	[6:4]	0x0	SCK	Read/write	GEST_DEC_MODE	Decimation rate for sample/gesture mode. 0: 1. 1: 2. 2: 4. 3: 8. 4: 16. 5: 32. Others: 32.
	[15:7]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x48	[7:0]	0xFF	SCK	Read/write	INT_MASK	Interrupt mask (active high) for the following: 0: proximity ON1 interrupt. 1: proximity OFF1 interrupt. 2: proximity ON2 interrupt. 3: proximity OFF2 interrupt. 4: gesture interrupt. 5: sample interrupt. 6: watchdog interrupt. 7: FIFO valid data more than threshold (FIFO_TH, Register 0x1F, Bits[11:8]).
	[15:8]	0x0	SCK	Read/write	Reserved	Write 0x0.
0x49	[7:0]	0x0	SCK	RW1C[1]	INT_STATUS	Status of interrupt. Each bit is cleared when 1 is written to that bit. 0: proximity ON1 interrupt. 1: proximity OFF1 interrupt. 2: proximity ON2 interrupt. 3: proximity OFF2 interrupt. 4: gesture interrupt. 5: sample interrupt. 6: watchdog interrupt. 7: FIFO valid data more than threshold (FIFO_TH, Register 0x1F, Bits[11:8]). This register self resets upon a read.
	[15:8]	0x0	SCK	RW1C[1]	FIFO_STATUS	FIFO status. Number of available data (in byte) to be read out. Note that Bits[6:0] are cleared when a write of 1 goes to Bit 15. This register self resets upon a read.
0x4A	[15:0]	0x0	SCK	Read only	I2C_STATUS	0: slave address match detection (can drive an interrupt). 1: repeated start (can drive an interrupt). 2: transmit request (can drive an interrupt). 3: return 0 when read. 4: transmit FIFO underflow. 5: transmit FIFO overflow. 6: slave responded with a no acknowledge (NACK). 7: slave busy. 8: general call reset interrupt (always drives an interrupt). 9: stop condition detected (can drive an interrupt). 10: high speed code detected. [15:11]: return 0s when read.

[1] RW1C is a read/write, cleared by writing a 1 to the register.

Table 32. Data Information Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x60	[15:0]	0x0	SCK	Read only	DATA_BUFFER_OUT	Data of next available word (16 bit) in FIFO

Table 33. Debug Registers

Address	Data Bits	Default Value	Update Type	Access Type	Name	Description
0x68	[15:0]	0x0	SCK	Read only	READ_X1L	Debug data register
0x69	[15:0]	0x0	SCK	Read only	READ_X2L	Debug data register
0x6A	[15:0]	0x0	SCK	Read only	READ_Y1L	Debug data register
0x6B	[15:0]	0x0	SCK	Read only	READ_Y2L	Debug data register
0x6C	[15:0]	0x0	SCK	Read only	READ_X1H	Debug data register
0x6D	[15:0]	0x0	SCK	Read only	READ_X2H	Debug data register
0x6E	[15:0]	0x0	SCK	Read only	READ_Y1H	Debug data register
0x6F	[15:0]	0x0	SCK	Read only	READ_Y2H	Debug data register

OUTLINE DIMENSIONS

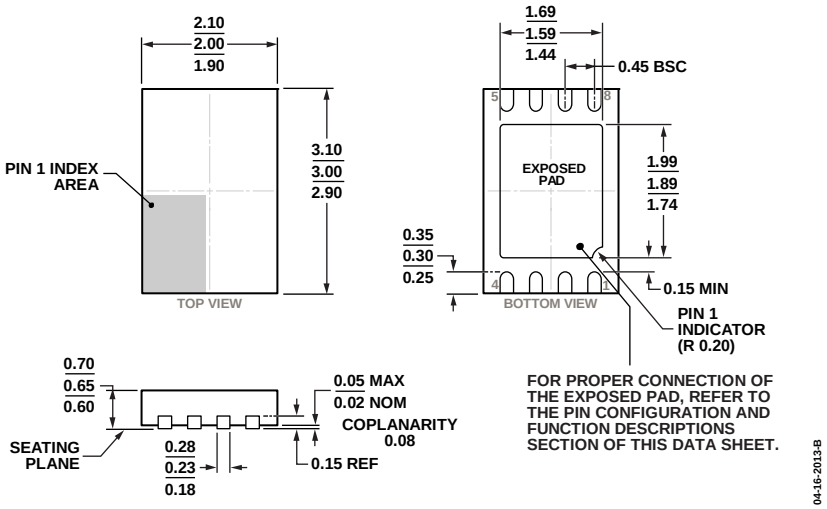

Figure 13. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 3 mm Body and 0.65 mm Package Height
(CP-8-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADUX1020BCPZRL7	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-17
ADUX1020-EVAL-SDP		ADUX1020 Evaluation Board	
ADUX1020-EVALZ-LED		High Power LED Daughterboard for ADUX1020 Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The ADUX1020-EVAL-SDP is a kit that includes the ADUX1020-EVAL-SMALL and the ADUX1020-EVAL-MCM.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).