AK8771

Shipped in packet-tape reel(5000pcs/Reel)

AK8771 is ultra-small Hall effect IC of a single silicon chip composed of Hall element and a signal processing IC.

| Bipolar Hall Effect Latch | Supply Voltage 1.6~5.5V | Power down Function | Ultra High Sensitivity Bop: 1.8mT | Output CMOS | SON | |
|------------------------------|----------------------------|------------------------|---|----------------|-----|--|
|------------------------------|----------------------------|------------------------|---|----------------|-----|--|

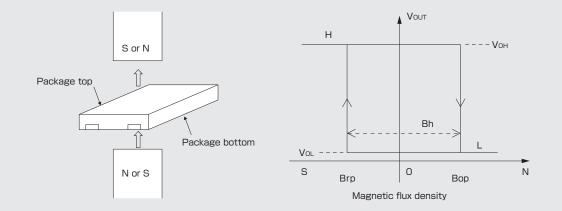
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Features

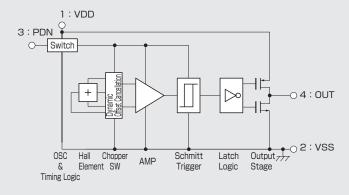
- Precision Bipolar Hall Effect Latch
- \cdot Power manageability through "PDN" pin Current consumption in Power down mode is less than 1 μA
- \cdot Ultra small SON package : 1.1 \times 1.4 \times t0.37mm, Halogen free



Operational Characteristics



Functional Block Diagram



| Item | Function | | | | |
|--|--|--|--|--|--|
| OSC | Generates operating clock | | | | |
| Timing Logic | Generates timing signal requires for Chopper SW, AMP and other circuits | | | | |
| Hall Element | Hall element fabricated by CMOS process | | | | |
| Chopper SW | Performs chopping in order to cancel the offset voltage of Hall sensor | | | | |
| AMP | Reduce offset voltage and amplifies Hall output voltage | | | | |
| Schmitt Trigger | hmitt Trigger Hysteresis comparator | | | | |
| Latch Logic Output Stage CMOS output, During the power down mode, out is latched in its previous state | | | | | |

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Absolute Maximum Ratings

| Item | symbol | Min. | Max. | Unit | Note |
|----------------------|--------|------|----------|------|------|
| Power supply voltage | Vdd | -0.3 | +6.5 | V | |
| Output current | Іоит | -0.5 | +0.5 | mA | OUT |
| Input voltage | VIN | -0.3 | VDD+0.3* | V | PDN |
| Input current | lin | -10 | +10 | mA | PDN |
| Storage temperature | Тѕтс | -55 | +125 | °C | |

*) Less than +6.5V.

Note) Stress beyond these listed values may cause permanent damage to the device.

Recommended Operating Conditions

| Item | symbol | Min. | Тур. | Max. | Unit |
|-----------------------|--------|------|------|------|------|
| Power supply voltage | VDD | 1.6 | 3.0 | 5.5 | V |
| Operating temperature | Та | -30 | | +85 | °C |

●Electrical Characteristics (Ta=25℃ VDD =3.0V)

| Item | symbol | Min. | Тур. | Max. | Unit | Note |
|----------------------------|--------|----------------------|------|------|------|--------------|
| Current consumption 1 | lod1 | | | 1 | μA | PDN=0V |
| Current consumption 2 | IDD2 | | 2.5 | 6 | mA | PDN=3V |
| PDN input current | lin | -1 | | 1 | μA | |
| PDN input H voltage | Vih | 0.7VDD | | | V | |
| PDN input L voltage | VIL | | | 0.3 | V | |
| High level output voltage | Vон | V _{DD} -0.4 | | | V | IOUT =-0.5mA |
| Low level output voltage | Vol | | | 0.4 | V | IOUT=+0.5mA |
| PDN mode transition time 1 | TPD1 | | | 100 | μs | Active→PDN |
| PDN mode transition time 2 | TPD2 | | | 100 | μs | PDN→Active |

●Magnetic Characteristics① (Ta=25℃ VDD=3.0V)

| Item | symbol | Min. | Тур. | Max. | Unit |
|-----------------|--------|------|------|------|------|
| Operating point | Вор | | 1.8 | 4.0 | mT |
| Releasing point | Brp | -4.0 | -1.8 | | mT |
| Hysteresis | Bh | | 3.6 | | mT |

●Magnetic Characteristics② (Ta=-30~+85℃ VDD = 1.6~5.5V)

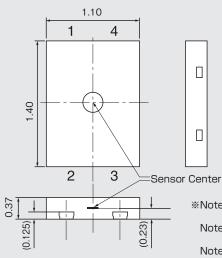
| Item | symbol | Min. | Тур. | Max. | Unit |
|-----------------|--------|------|------|------|------|
| Operating point | Вор | | 1.8 | 4.2 | mT |
| Releasing point | Brp | -4.2 | -1.8 | | mT |
| Hysteresis | Bh | | 3.6 | | mT |

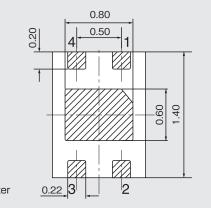
Note) The specifications in Magnetic Characteristics 2 are design targets.

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Package (Unit:mm)





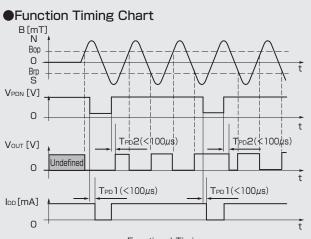
«Note 1) Sensitive area position referenced to the center of package within ϕ 0.3mm circle. Note 2) Tolerances of dimension otherwise noted is

±0.05mm.

Note 3) Hatched area is plated.

Note 4) Center pad area (TAB) should be tied to the VSS or floating

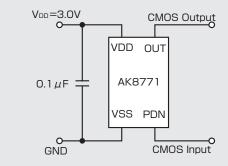
| No. | Pin name | Function | Note |
|-----|----------|---------------------|---------------------------------|
| 1 | VDD | Power supply | |
| 2 | VSS | Ground | |
| 3 | PDN | Power down. | CMOS Input. This pin has to be |
| | | H:Device active | tied to "H" level when external |
| | | L:Device power down | power control is not used. |
| 4 | OUT | Output | CMOS Output |



Functional Timing

- Note1) During power down mode, output is latched in its previous state.
- Note2) When VDD is supplied, the time from reaching V_{DD} =1.6V to the update of the output state is equal to TPD2.

Application Circuit



•Footprint (for reference)

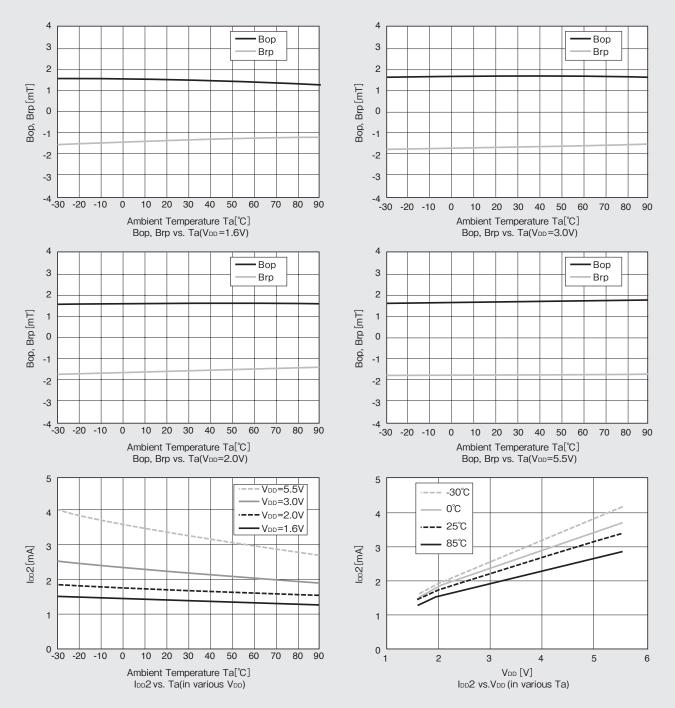
0.35

0.22

0.80

0.50

0.60 1.00 .70



•Typical Characteristic Data (for reference)

AK8771

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