

### FEATURES

- Fully differential**
- Low noise**
  - 2.25 nV/ $\sqrt{\text{Hz}}$
  - 2.1 pA/ $\sqrt{\text{Hz}}$
- Low harmonic distortion**
  - 98 dBc SFDR @ 1 MHz
  - 85 dBc SFDR @ 5 MHz
  - 72 dBc SFDR @ 20 MHz
- High speed**
  - 410 MHz, 3 dB BW (G = 1)
  - 800 V/ $\mu\text{s}$  slew rate
  - 45 ns settling time to 0.01%
- 69 dB output balance @ 1 MHz**
- 80 dB dc CMRR**
- Low offset:  $\pm 0.5$  mV maximum**
- Low input offset current: 0.5  $\mu\text{A}$  maximum**
- Differential input and output**
- Differential-to-differential or single-ended-to-differential operation**
- Rail-to-rail output**
- Adjustable output common-mode voltage**
- Wide supply voltage range: 5 V to 12 V**
- Available in a small SOIC package and an 8-lead LFCSP**

### GENERAL DESCRIPTION

The AD8139 is an ultralow noise, high performance differential amplifier with rail-to-rail output. With its low noise, high SFDR, and wide bandwidth, it is an ideal choice for driving ADCs with resolutions to 18 bits. The AD8139 is easy to apply, and its internal common-mode feedback architecture allows its output common-mode voltage to be controlled by the voltage applied to one pin. The internal feedback loop also provides outstanding output balance as well as suppression of even-order harmonic distortion products. Fully differential and single-ended-to-differential gain configurations are easily realized by the AD8139. Simple external feedback networks consisting of four resistors determine the closed-loop gain of the amplifier.

The AD8139 is manufactured on the Analog Devices, Inc. proprietary, second-generation XFCB process, enabling it to achieve low levels of distortion with input voltage noise of only 2.25 nV/ $\sqrt{\text{Hz}}$ .

### APPLICATIONS

- ADC drivers to 18 bits
- Single-ended-to-differential converters
- Differential filters
- Level shifters
- Differential PCB drivers
- Differential cable drivers

### FUNCTIONAL BLOCK DIAGRAMS

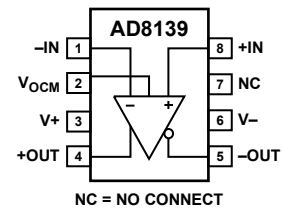


Figure 1. 8-Lead SOIC

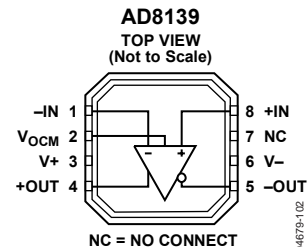


Figure 2. 8-Lead LFCSP

The AD8139 is available in an 8-lead SOIC package with an exposed paddle (EP) on the underside of its body and a 3 mm  $\times$  3 mm LFCSP. It is rated to operate over the temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

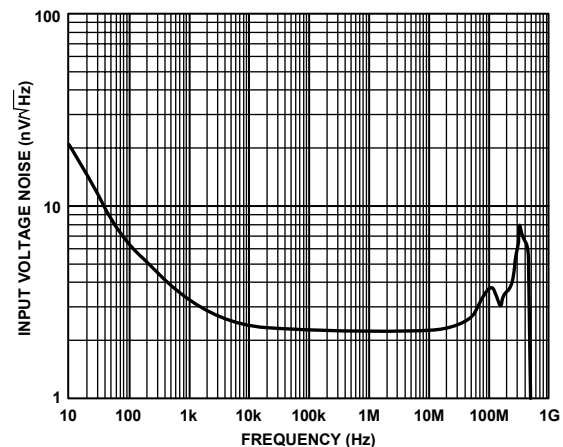


Figure 3. Input Voltage Noise vs. Frequency

#### Rev. B

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## TABLE OF CONTENTS

Features .....	1
Applications .....	1
Functional Block Diagrams .....	1
General Description .....	1
Revision History .....	2
Specifications .....	3
$V_S = \pm 5\text{ V}$ , $V_{OCM} = 0\text{ V}$ .....	3
$V_S = 5\text{ V}$ , $V_{OCM} = 2.5\text{ V}$ .....	5
Absolute Maximum Ratings .....	7
Thermal Resistance .....	7
ESD Caution .....	7

## REVISION HISTORY

### 10/07—Rev. A to Rev. B.

Changes to General Description .....	1
Inserted Figure 2; Renumbered Sequentially .....	1
Changes to Table 1 .....	3
Changes to Table 2 .....	5
Changes to Table 6 and Layout .....	8
Inserted Figure 6; Renumbered Sequentially .....	8
Changes to Figure 30 .....	12
Changes to Layout .....	17
Changes to Figure 63 .....	22
Changes to Exposed Paddle (EP) Section .....	23
Updated Outline Dimensions .....	24

Pin Configurations and Function Descriptions .....	8
Typical Performance Characteristics .....	9
Test Circuits .....	17
Theory of Operation .....	18
Typical Connection and Definition of Terms .....	18
Applications .....	19
Estimating Noise, Gain, and Bandwidth with Matched Feedback Networks .....	19
Outline Dimensions .....	24
Ordering Guide .....	24

### 8/04—Rev. 0 to Rev. A.

Added 8-Lead LFCSP .....	Universal
Changes to General Description .....	1
Changes to Figure 2 .....	1
Changes to $V_S = \pm 5\text{ V}$ , $V_{OCM} = 0\text{ V}$ Specifications .....	3
Changes to $V_S = 5\text{ V}$ , $V_{OCM} = 2.5\text{ V}$ Specifications .....	5
Changes to Table 4 .....	7
Changes to Maximum Power Dissipation Section .....	7
Changes to Figure 26 and Figure 29 .....	12
Inserted Figure 39 and Figure 42 .....	14
Changes to Figure 45 to Figure 47 .....	15
Inserted Figure 48 .....	15
Changes to Figure 52 and Figure 53 .....	16
Changes to Figure 55 and Figure 56 .....	17
Changes to Table 6 .....	19
Changes to Voltage Gain Section .....	19
Changes to Driving a Capacitive Load Section .....	22
Changes to Ordering Guide .....	24
Updated Outline Dimensions .....	24

### 5/04—Revision 0: Initial Version

## SPECIFICATIONS

$V_S = \pm 5\text{ V}$ ,  $V_{OCM} = 0\text{ V}$

$T_A = 25^\circ\text{C}$ , differential gain = 1,  $R_{L, dm} = 1\text{ k}\Omega$ ,  $R_F = R_G = 200\ \Omega$ , unless otherwise noted.  $T_{MIN}$  to  $T_{MAX} = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
<b>DIFFERENTIAL INPUT PERFORMANCE</b>					
Dynamic Performance					
–3 dB Small Signal Bandwidth	$V_{O, dm} = 0.1\text{ V p-p}$	340	410		MHz
–3 dB Large Signal Bandwidth	$V_{O, dm} = 2\text{ V p-p}$	210	240		MHz
Bandwidth for 0.1 dB Flatness	$V_{O, dm} = 0.1\text{ V p-p}$		45		MHz
Slew Rate	$V_{O, dm} = 2\text{ V step}$		800		V/ $\mu\text{s}$
Settling Time to 0.01%	$V_{O, dm} = 2\text{ V step}$ , $C_F = 2\text{ pF}$		45		ns
Overdrive Recovery Time	$G = 2$ , $V_{IN, dm} = 12\text{ V p-p}$ triangle wave		30		ns
Noise/Harmonic Performance					
SFDR					
	$V_{O, dm} = 2\text{ V p-p}$ , $f_c = 1\text{ MHz}$		98		dBc
	$V_{O, dm} = 2\text{ V p-p}$ , $f_c = 5\text{ MHz}$		85		dBc
	$V_{O, dm} = 2\text{ V p-p}$ , $f_c = 20\text{ MHz}$		72		dBc
Third-Order IMD	$V_{O, dm} = 2\text{ V p-p}$ , $f_c = 10.05\text{ MHz} \pm 0.05\text{ MHz}$		–90		dBc
Input Voltage Noise	$f = 100\text{ kHz}$		2.25		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		2.1		pA/ $\sqrt{\text{Hz}}$
DC Performance					
Input Offset Voltage	$V_{IP} = V_{IN} = V_{OCM} = 0\text{ V}$	–500	$\pm 150$	+500	$\mu\text{V}$
Input Offset Voltage Drift	$T_{MIN}$ to $T_{MAX}$		1.25		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$T_{MIN}$ to $T_{MAX}$		2.25	8.0	$\mu\text{A}$
Input Offset Current			0.12	0.5	$\mu\text{A}$
Open-Loop Gain			114		dB
Input Characteristics					
Input Common-Mode Voltage Range		–4		+4	V
Input Resistance	Differential		600		k $\Omega$
	Common mode		1.5		M $\Omega$
Input Capacitance	Common mode		1.2		pF
CMRR	$\Delta V_{ICM} = \pm 1\text{ V dc}$ , $R_F = R_G = 10\text{ k}\Omega$	80	84		dB
Output Characteristics					
Output Voltage Swing	Each single-ended output, $R_F = R_G = 10\text{ k}\Omega$	$-V_S + 0.20$		$+V_S - 0.20$	V
	Each single-ended output, $R_{L, dm} = \text{open circuit}$ , $R_F = R_G = 10\text{ k}\Omega$	$-V_S + 0.15$		$+V_S - 0.15$	V
Output Current	Each single-ended output		100		mA
Output Balance Error	$f = 1\text{ MHz}$		–69		dB
<b><math>V_{OCM}</math> TO <math>V_{O, cm}</math> PERFORMANCE</b>					
$V_{OCM}$ Dynamic Performance					
–3 dB Bandwidth	$V_{O, cm} = 0.1\text{ V p-p}$		515		MHz
Slew Rate	$V_{O, cm} = 2\text{ V p-p}$		250		V/ $\mu\text{s}$
Gain		0.999	1.000	1.001	V/V
$V_{OCM}$ Input Characteristics					
Input Voltage Range		–3.8		+3.8	V
Input Resistance			3.5		M $\Omega$
Input Offset Voltage	$V_{OS, cm} = V_{O, cm} - V_{OCM}$ ; $V_{IP} = V_{IN} = V_{OCM} = 0\text{ V}$	–900	$\pm 300$	+900	$\mu\text{V}$
Input Voltage Noise	$f = 100\text{ kHz}$		3.5		nV/ $\sqrt{\text{Hz}}$
Input Bias Current			1.3	4.5	$\mu\text{A}$
CMRR	$\Delta V_{OCM}/\Delta V_{O, dm}$ , $\Delta V_{OCM} = \pm 1\text{ V}$	74	88		dB

# AD8139

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		+4.5		±6	V
Quiescent Current			24.5	25.5	mA
+PSRR	Change in $+V_s = \pm 1$ V	95	112		dB
-PSRR	Change in $-V_s = \pm 1$ V	95	109		dB
OPERATING TEMPERATURE RANGE		-40		+125	°C

**$V_S = 5\text{ V}$ ,  $V_{OCM} = 2.5\text{ V}$**  $T_A = 25^\circ\text{C}$ , differential gain = 1,  $R_{L, dm} = 1\text{ k}\Omega$ ,  $R_F = R_G = 200\ \Omega$ , unless otherwise noted.  $T_{MIN}$  to  $T_{MAX} = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .**Table 2.**

Parameter	Conditions	Min	Typ	Max	Unit
<b>DIFFERENTIAL INPUT PERFORMANCE</b>					
Dynamic Performance					
–3 dB Small Signal Bandwidth	$V_{O, dm} = 0.1\text{ V p-p}$	330	385		MHz
–3 dB Large Signal Bandwidth	$V_{O, dm} = 2\text{ V p-p}$	135	165		MHz
Bandwidth for 0.1 dB Flatness	$V_{O, dm} = 0.1\text{ V p-p}$		34		MHz
Slew Rate	$V_{O, dm} = 2\text{ V step}$		540		V/ $\mu\text{s}$
Settling Time to 0.01%	$V_{O, dm} = 2\text{ V step}$		55		ns
Overdrive Recovery Time	$G = 2$ , $V_{IN, dm} = 7\text{ V p-p triangle wave}$		35		ns
Noise/Harmonic Performance					
SFDR	$V_{O, dm} = 2\text{ V p-p}$ , $f_c = 1\text{ MHz}$		99		dBc
	$V_{O, dm} = 2\text{ V p-p}$ , $f_c = 5\text{ MHz}$ , $R_L = 800\ \Omega$		87		dBc
	$V_{O, dm} = 2\text{ V p-p}$ , $f_c = 20\text{ MHz}$ , $R_L = 800\ \Omega$		75		dBc
Third-Order IMD	$V_{O, dm} = 2\text{ V p-p}$ , $f_c = 10.05\text{ MHz} \pm 0.05\text{ MHz}$		–87		dBc
Input Voltage Noise	$f = 100\text{ kHz}$		2.25		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		2.1		pA/ $\sqrt{\text{Hz}}$
DC Performance					
Input Offset Voltage	$V_{IP} = V_{IN} = V_{OCM} = 2.5\text{ V}$	–500	$\pm 150$	+500	$\mu\text{V}$
Input Offset Voltage Drift	$T_{MIN}$ to $T_{MAX}$		1.25		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$T_{MIN}$ to $T_{MAX}$		2.2	7.5	$\mu\text{A}$
Input Offset Current			0.13	0.5	$\mu\text{A}$
Open-Loop Gain			112		dB
Input Characteristics					
Input Common-Mode Voltage Range		1		4	V
Input Resistance	Differential		600		k $\Omega$
	Common mode		1.5		M $\Omega$
Input Capacitance	Common mode		1.2		pF
CMRR	$\Delta V_{ICM} = \pm 1\text{ V dc}$ , $R_F = R_G = 10\text{ k}\Omega$	75	79		dB
Output Characteristics					
Output Voltage Swing	Each single-ended output, $R_F = R_G = 10\text{ k}\Omega$	$-V_S + 0.15$		$+V_S - 0.15$	V
	Each single-ended output, $R_{L, dm} = \text{open circuit}$ , $R_F = R_G = 10\text{ k}\Omega$	$-V_S + 0.10$		$+V_S - 0.10$	V
Output Current	Each single-ended output		80		mA
Output Balance Error	$f = 1\text{ MHz}$		–70		dB
<b><math>V_{OCM}</math> TO <math>V_{O, cm}</math> PERFORMANCE</b>					
$V_{OCM}$ Dynamic Performance					
–3 dB Bandwidth	$V_{O, cm} = 0.1\text{ V p-p}$		440		MHz
Slew Rate	$V_{O, cm} = 2\text{ V p-p}$		150		V/ $\mu\text{s}$
Gain		0.999	1.000	1.001	V/V
$V_{OCM}$ Input Characteristics					
Input Voltage Range		1.0		3.8	V
Input Resistance			3.5		M $\Omega$
Input Offset Voltage	$V_{OS, cm} = V_{O, cm} - V_{OCM}$ ; $V_{IP} = V_{IN} = V_{OCM} = 2.5\text{ V}$	–1.0	$\pm 0.45$	+1.0	mV
Input Voltage Noise	$f = 100\text{ kHz}$		3.5		nV/ $\sqrt{\text{Hz}}$
Input Bias Current			1.3	4.2	$\mu\text{A}$
CMRR	$\Delta V_{OCM}/\Delta V_{O, dm}$ , $\Delta V_{OCM} = \pm 1\text{ V}$	67	79		dB

# AD8139

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		+4.5		±6	V
Quiescent Current			21.5	22.5	mA
+PSRR	Change in $+V_S = \pm 1$ V	86	97		dB
-PSRR	Change in $-V_S = \pm 1$ V	92	105		dB
OPERATING TEMPERATURE RANGE		-40		+125	°C

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12 V
$V_{OCM}$	$\pm V_S$
Power Dissipation	See Figure 4
Input Common-Mode Voltage	$\pm V_S$
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Operating Temperature Range	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Lead Temperature (Soldering 10 sec)	$300^{\circ}\text{C}$
Junction Temperature	$150^{\circ}\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is,  $\theta_{JA}$  is specified for device soldered in circuit board for surface-mount packages.

Table 4.

Package Type	$\theta_{JA}$	Unit
8-Lead SOIC with EP/4-Layer	70	$^{\circ}\text{C}/\text{W}$
8-Lead LFCSP/4-Layer	70	$^{\circ}\text{C}/\text{W}$

### Maximum Power Dissipation

The maximum safe power dissipation in the AD8139 package is limited by the associated rise in junction temperature ( $T_J$ ) on the die. At approximately  $150^{\circ}\text{C}$ , which is the glass transition temperature, the plastic will change its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8139. Exceeding a junction temperature of  $175^{\circ}\text{C}$  for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package ( $P_D$ ) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins ( $V_S$ ) times the quiescent current ( $I_S$ ). The load current consists of differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and the internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a  $1\text{ k}\Omega$  differential load on the output. RMS output voltages should be considered when dealing with ac signals.

Airflow reduces  $\theta_{JA}$ . In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduce the  $\theta_{JA}$ .

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the exposed paddle (EP) 8-lead SOIC ( $\theta_{JA} = 70^{\circ}\text{C}/\text{W}$ ) and the 8-lead LFCSP ( $\theta_{JA} = 70^{\circ}\text{C}/\text{W}$ ) on a JEDEC standard 4-layer board.  $\theta_{JA}$  values are approximations.

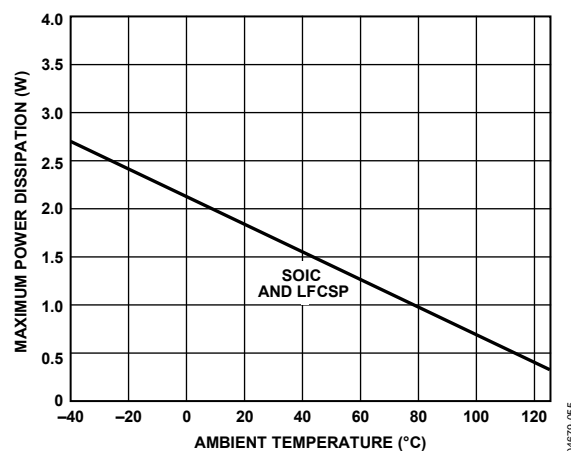


Figure 4. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# AD8139

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

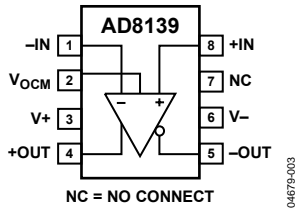


Figure 5. 8-Lead SOIC Pin Configuration

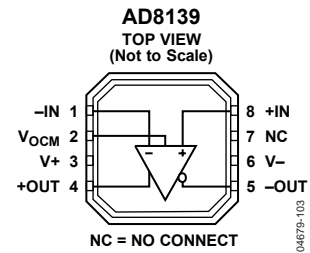


Figure 6. 8-Lead LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	-IN	Inverting Input.
2	$V_{OCM}$	An internal feedback loop drives the output common-mode voltage to be equal to the voltage applied to the $V_{OCM}$ pin, provided the operation of the amplifier remains linear.
3	V+	Positive Power Supply Voltage.
4	+OUT	Positive Side of the Differential Output.
5	-OUT	Negative Side of the Differential Output.
6	V-	Negative Power Supply Voltage.
7	NC	No Internal Connection.
8	+IN	Noninverting Input.
9	Exposed Paddle	Solder exposed paddle on back of package to ground plane or to a power plane.



# TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, differential gain = +1,  $R_G = R_F = 200 \Omega$ ,  $R_{L, dm} = 1 \text{ k}\Omega$ ,  $V_S = \pm 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OCM} = 0 \text{ V}$ . Refer to the basic test circuit in Figure 57 for the definition of terms.

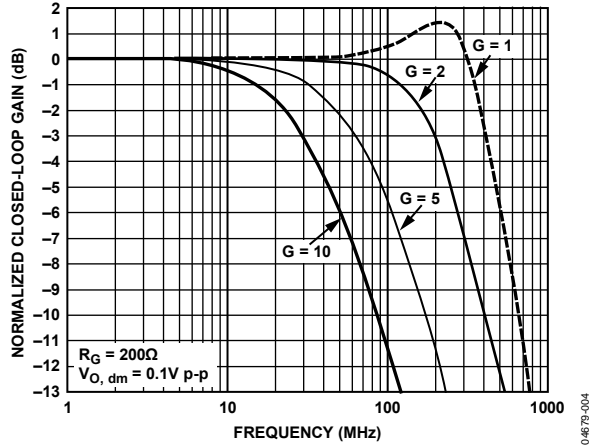


Figure 7. Small Signal Frequency Response for Various Gains

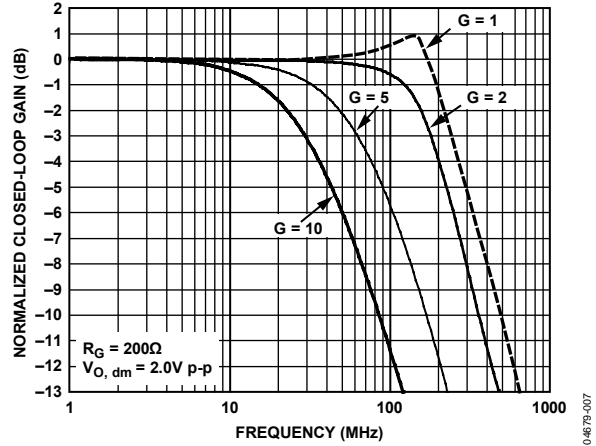


Figure 10. Large Signal Frequency Response for Various Gains

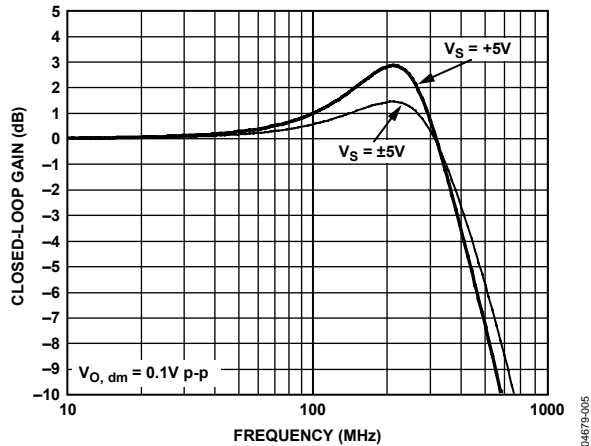


Figure 8. Small Signal Frequency Response for Various Power Supplies

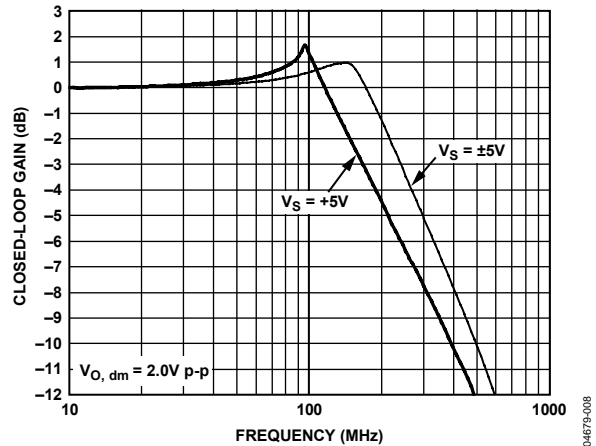


Figure 11. Large Signal Frequency Response for Various Power Supplies

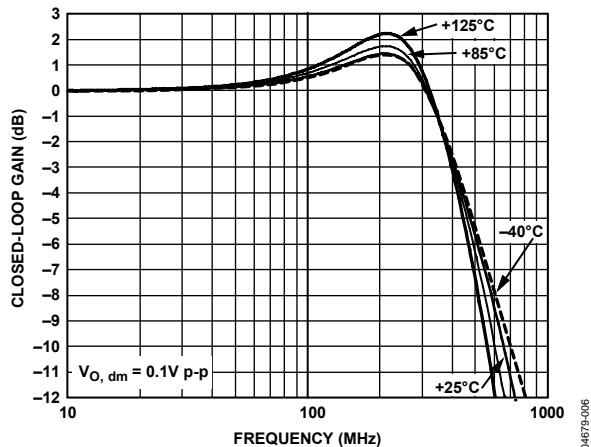


Figure 9. Small Signal Frequency Response at Various Temperatures

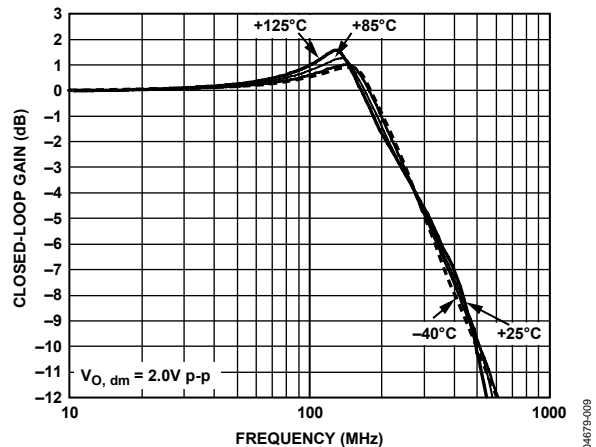


Figure 12. Large Signal Frequency Response at Various Temperatures

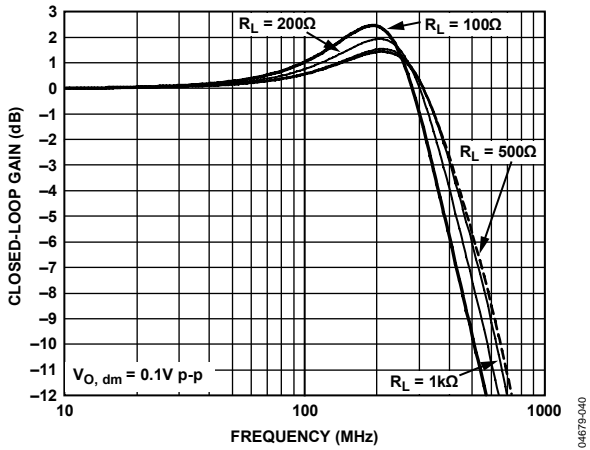


Figure 13. Small Signal Frequency Response for Various Loads

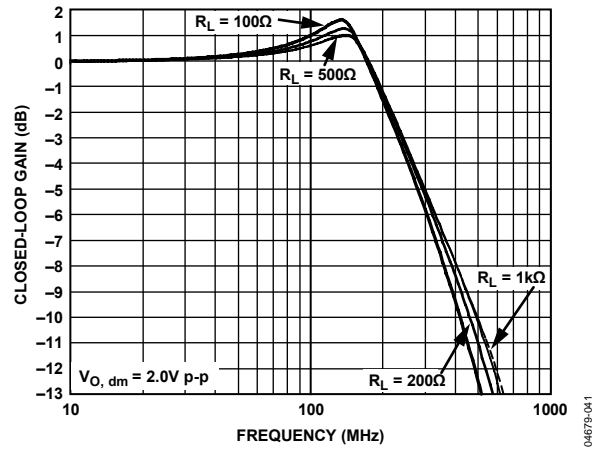


Figure 16. Large Signal Frequency Response for Various Loads

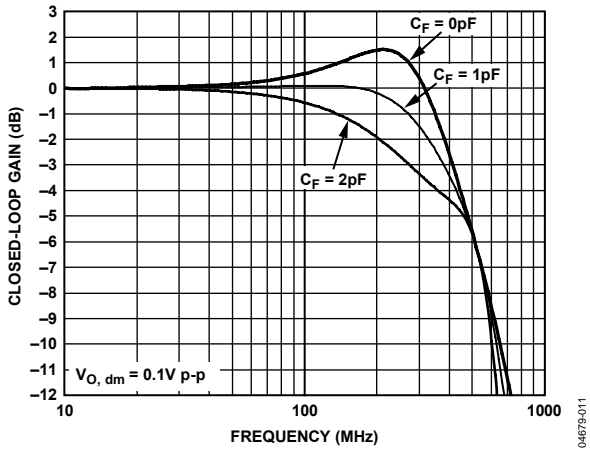


Figure 14. Small Signal Frequency Response for Various  $C_F$

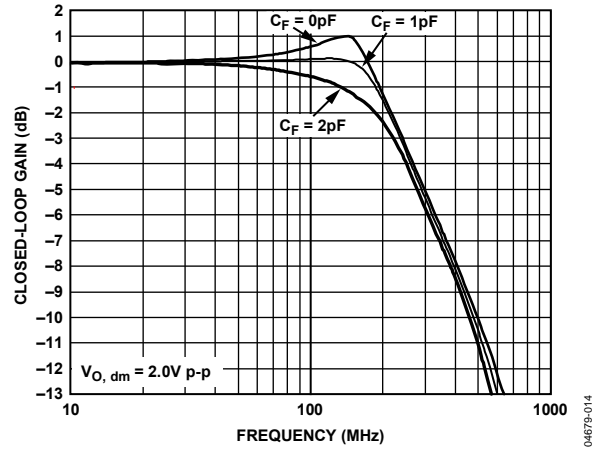


Figure 17. Large Signal Frequency Response for Various  $C_F$

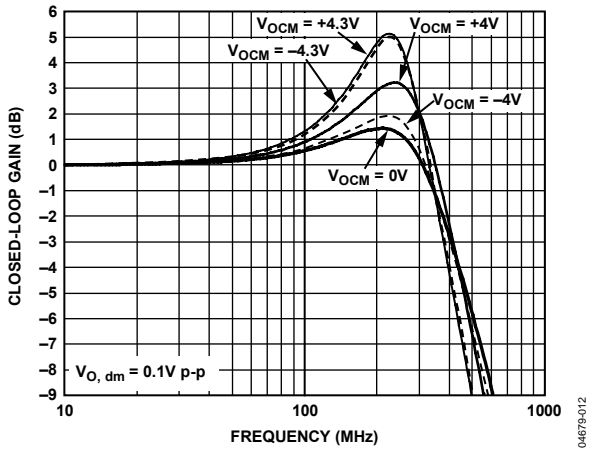


Figure 15. Small Signal Frequency Response at Various  $V_{OCM}$

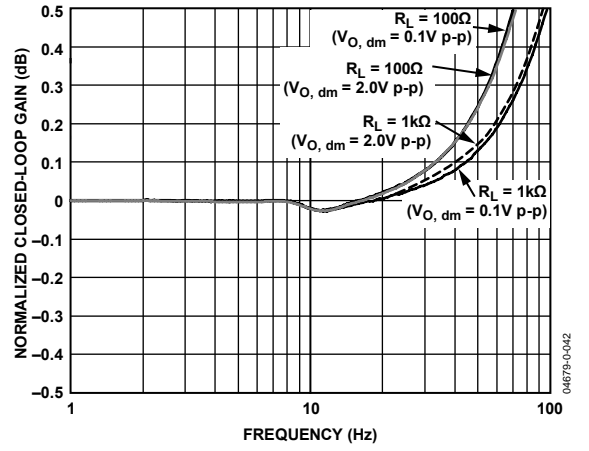


Figure 18. 0.1 dB Flatness for Various Loads and Output Amplitudes

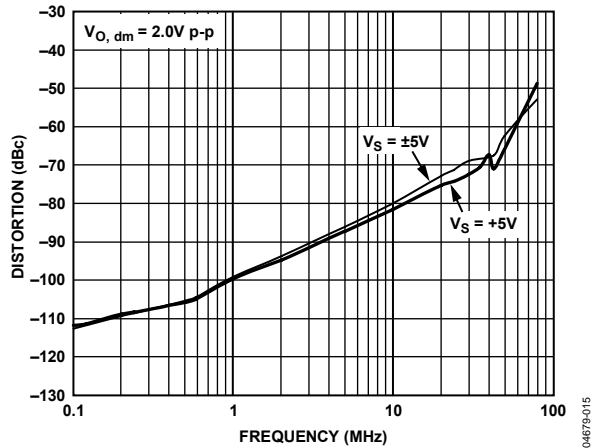


Figure 19. Second Harmonic Distortion vs. Frequency and Supply Voltage

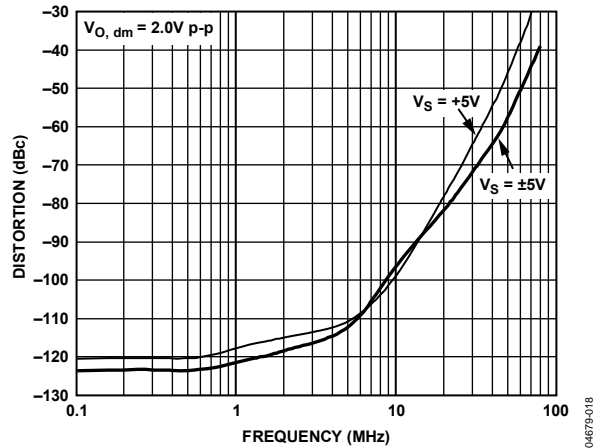


Figure 22. Third Harmonic Distortion vs. Frequency and Supply Voltage

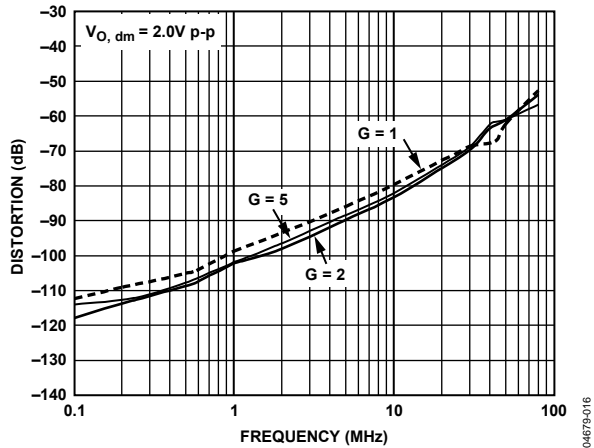


Figure 20. Second Harmonic Distortion vs. Frequency and Gain

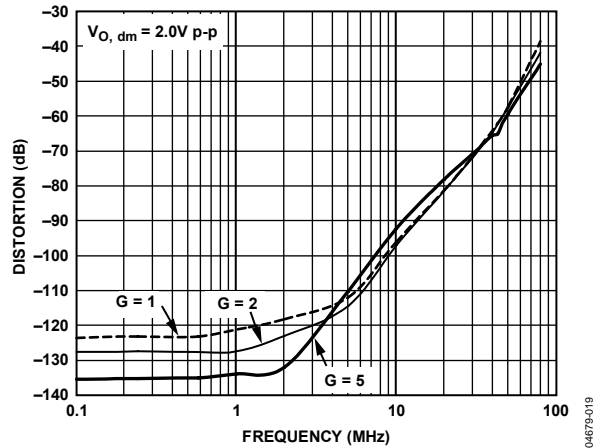


Figure 23. Third Harmonic Distortion vs. Frequency and Gain

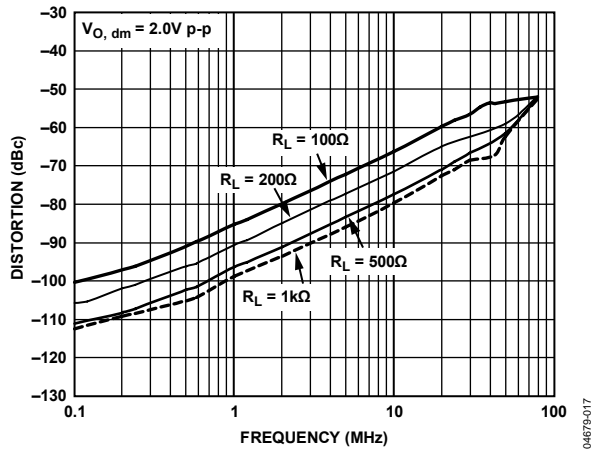


Figure 21. Second Harmonic Distortion vs. Frequency and Load

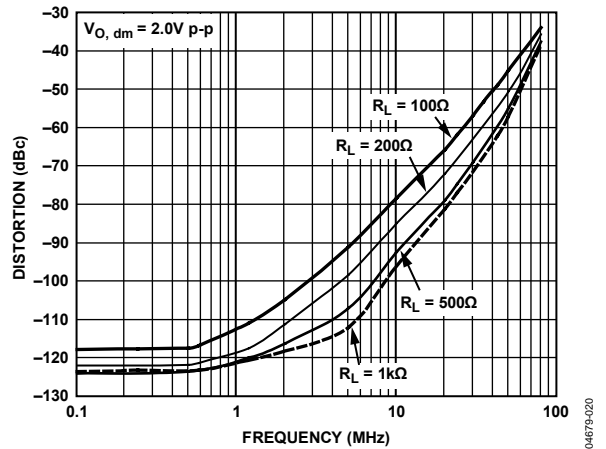


Figure 24. Third Harmonic Distortion vs. Frequency and Load

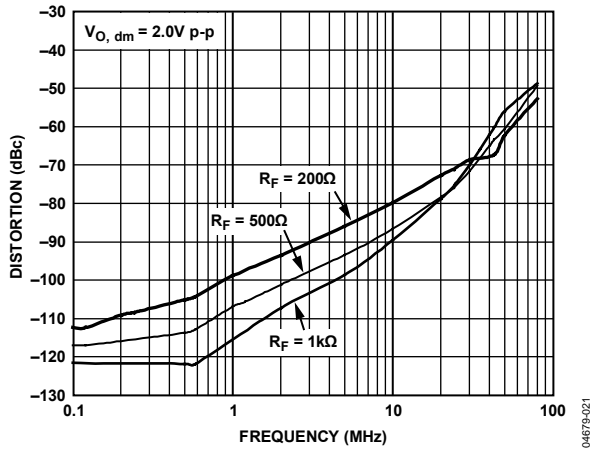


Figure 25. Second Harmonic Distortion vs. Frequency and  $R_F$

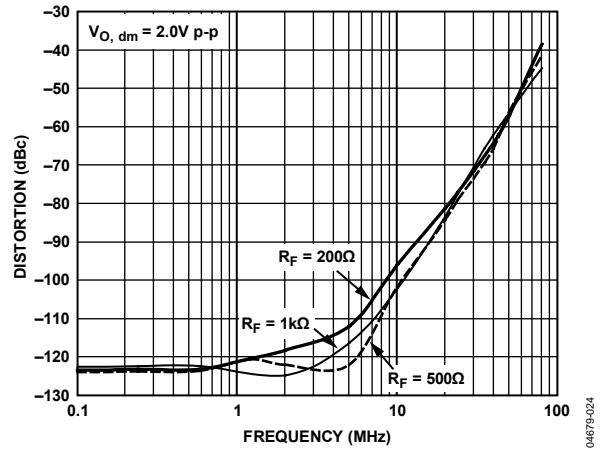


Figure 28. Third Harmonic Distortion vs. Frequency and  $R_F$

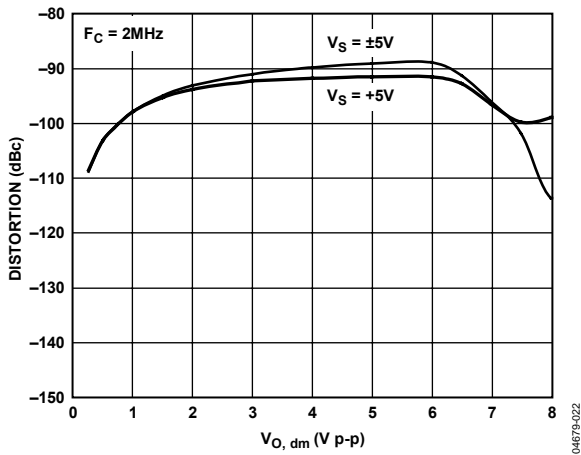


Figure 26. Second Harmonic Distortion vs. Output Amplitude

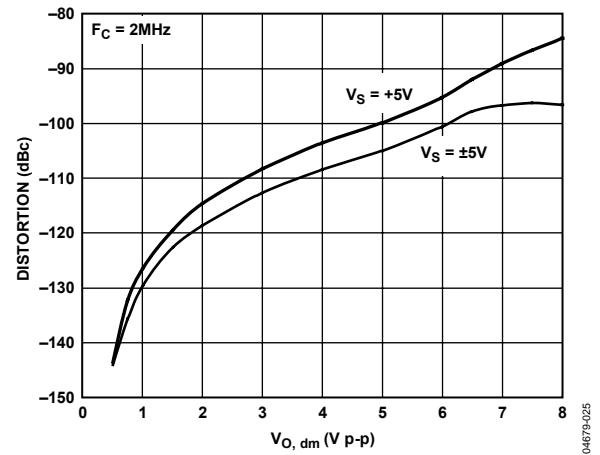


Figure 29. Third Harmonic Distortion vs. Output Amplitude

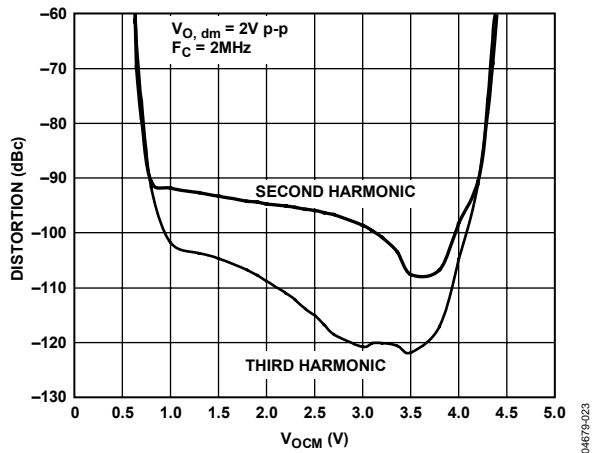


Figure 27. Harmonic Distortion vs.  $V_{OCM}$ ,  $V_S = +5V$

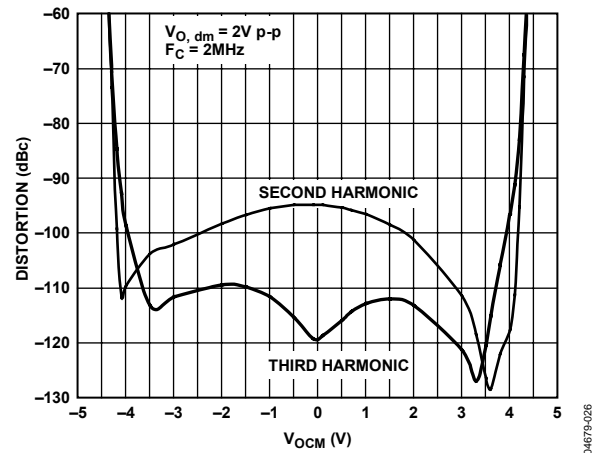


Figure 30. Harmonic Distortion vs.  $V_{OCM}$ ,  $V_S = \pm 5V$

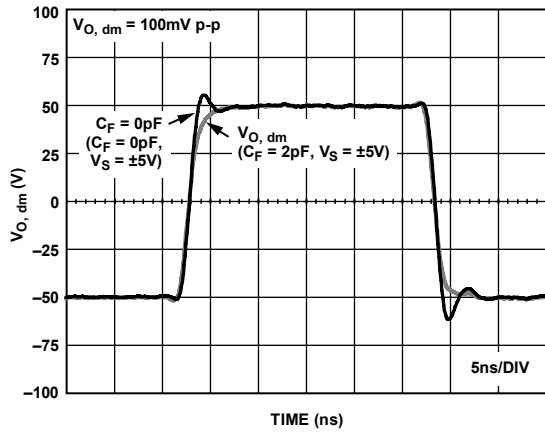


Figure 31. Small Signal Transient Response for Various  $C_f$

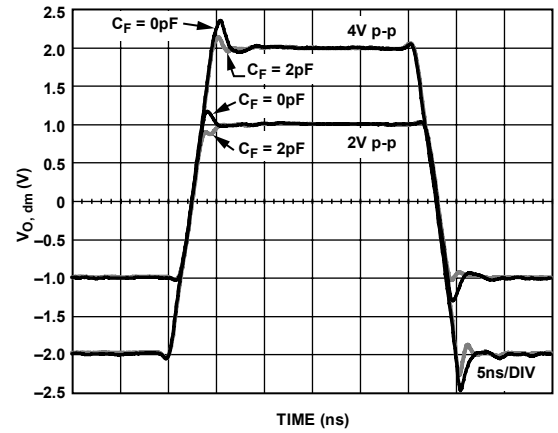


Figure 34. Large Signal Transient Response for Various  $C_f$

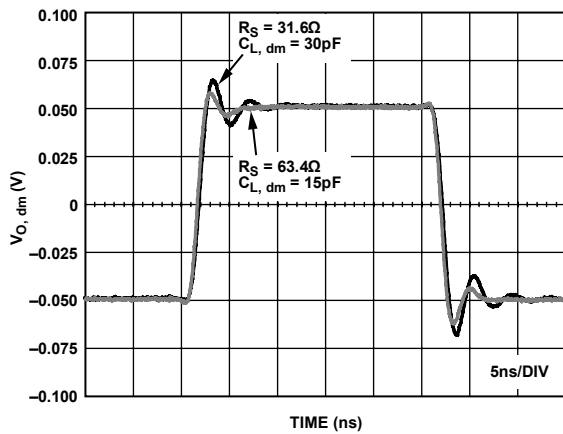


Figure 32. Small Signal Transient Response for Capacitive Loads

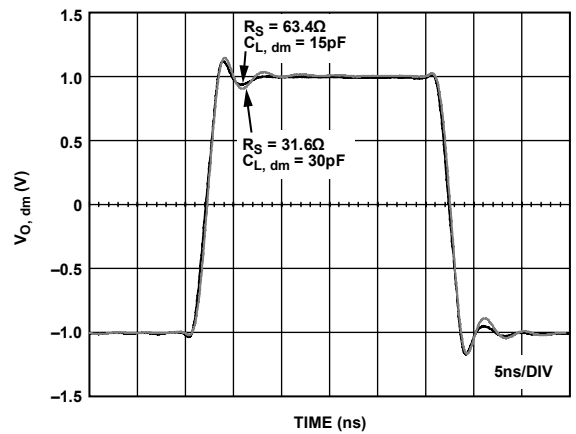


Figure 35. Large Signal Transient Response for Capacitive Loads

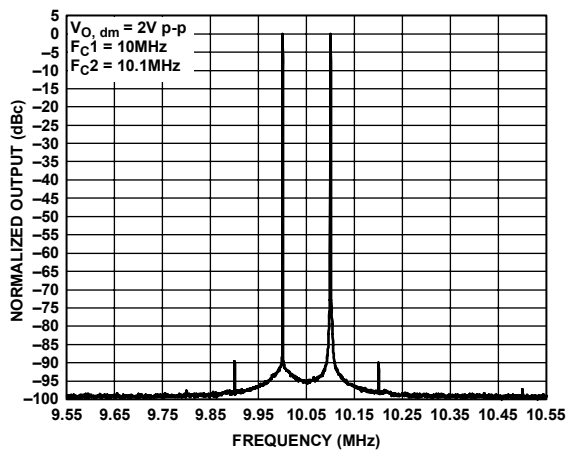


Figure 33. Intermodulation Distortion

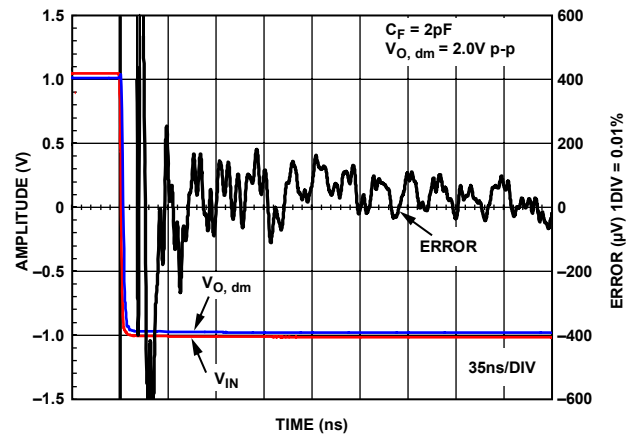


Figure 36. Settling Time (0.01%)

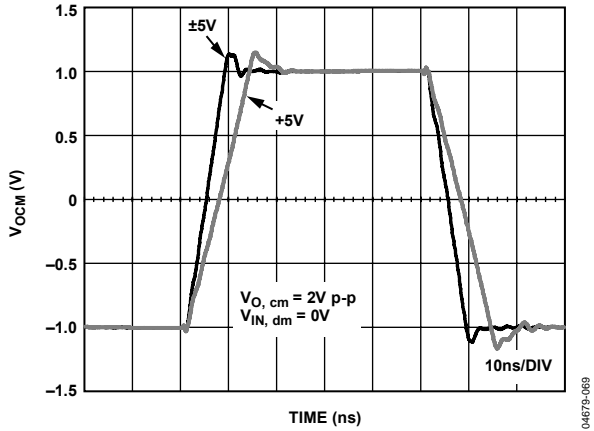


Figure 37.  $V_{OCM}$  Large Signal Transient Response

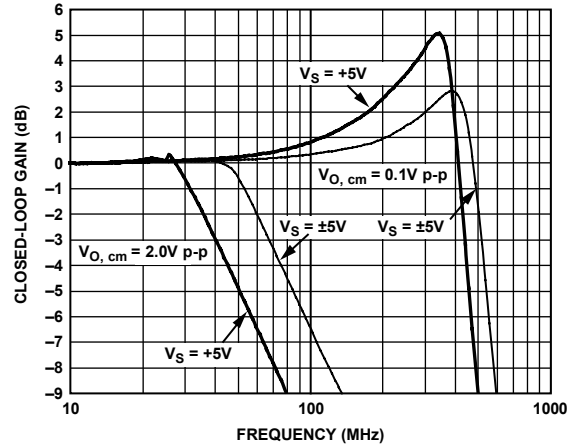


Figure 40.  $V_{OCM}$  Frequency Response for Various Supplies

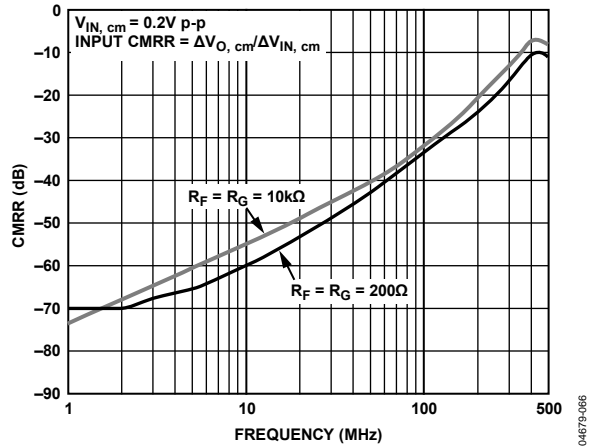


Figure 38. CMRR vs. Frequency

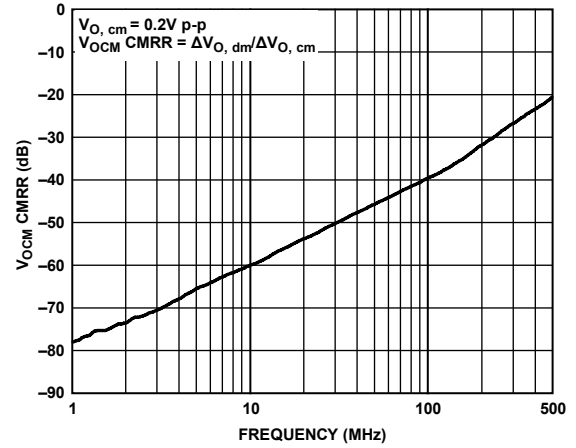


Figure 41.  $V_{OCM}$  CMRR vs. Frequency

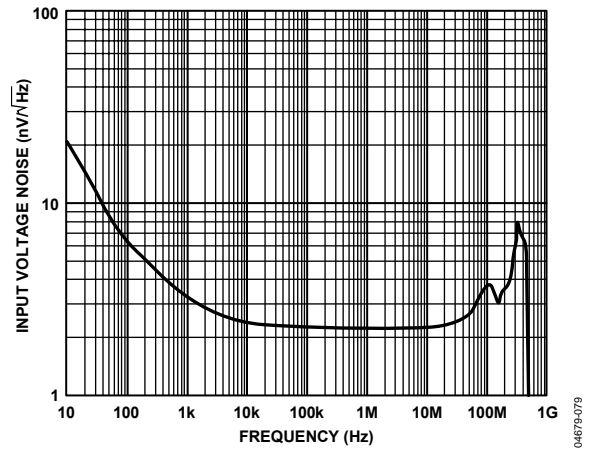


Figure 39. Input Voltage Noise vs. Frequency

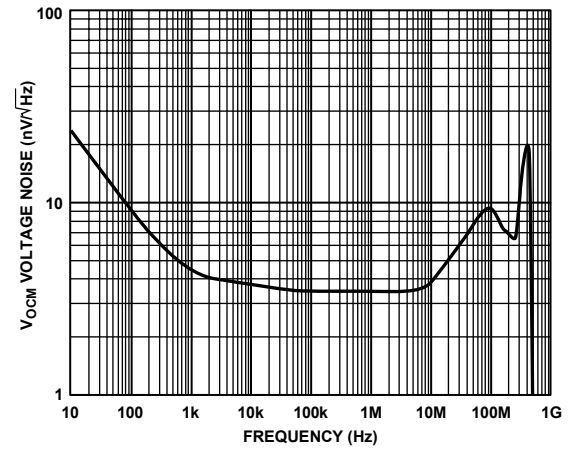


Figure 42.  $V_{OCM}$  Voltage Noise vs. Frequency

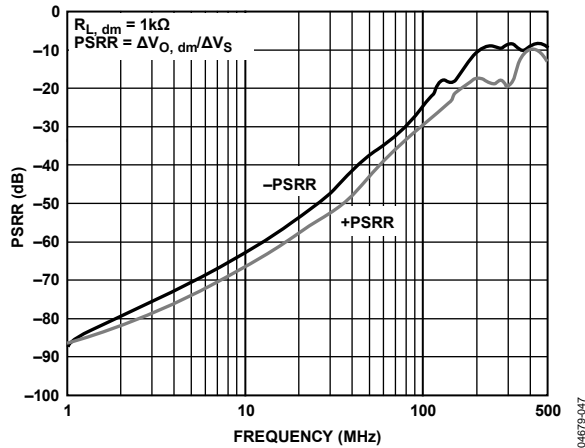


Figure 43. PSRR vs. Frequency

04679-047

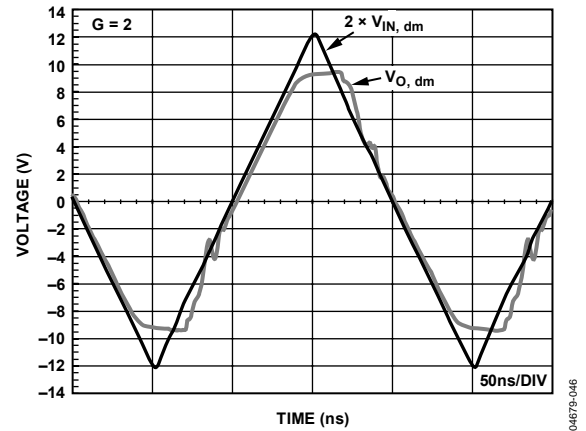


Figure 46. Overdrive Recovery

04679-046

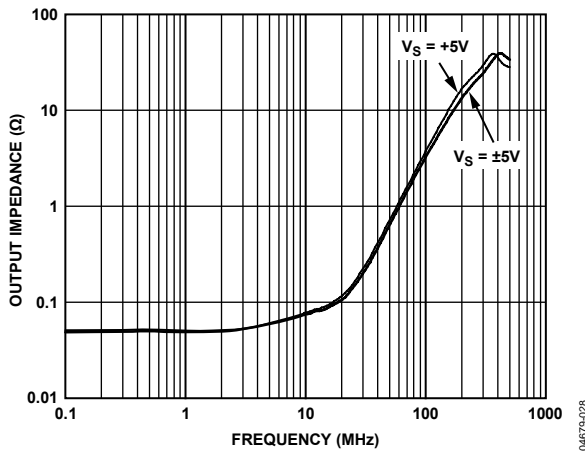


Figure 44. Single-Ended Output Impedance vs. Frequency

04679-028

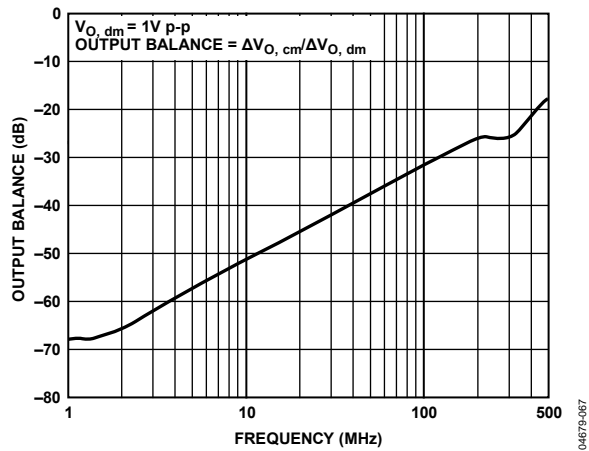


Figure 47. Output Balance vs. Frequency

04679-067

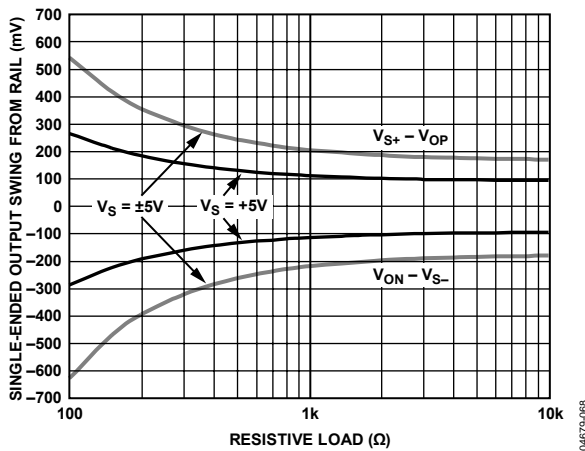


Figure 45. Output Saturation Voltage vs. Output Load

04679-068

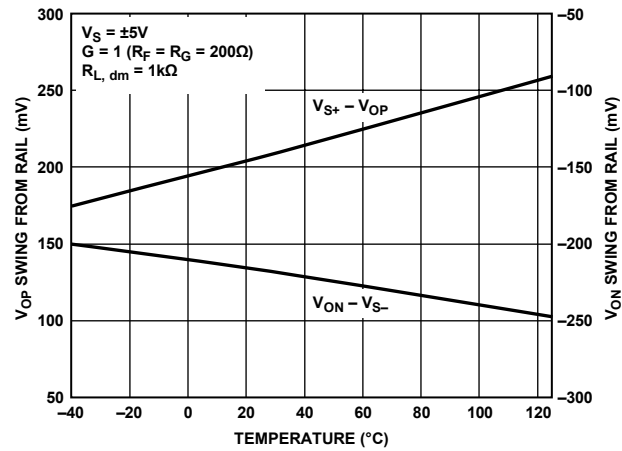


Figure 48. Output Saturation Voltage vs. Temperature

04679-077

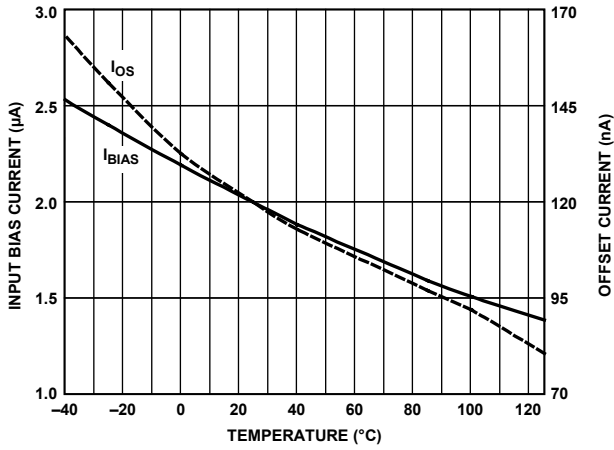


Figure 49. Input Bias and Offset Current vs. Temperature

04679-062

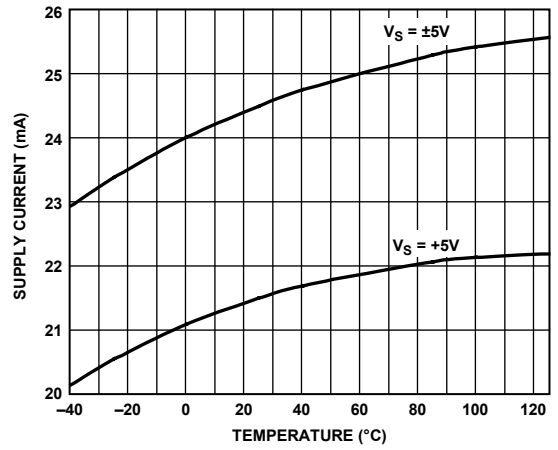


Figure 52. Supply Current vs. Temperature

04679-060

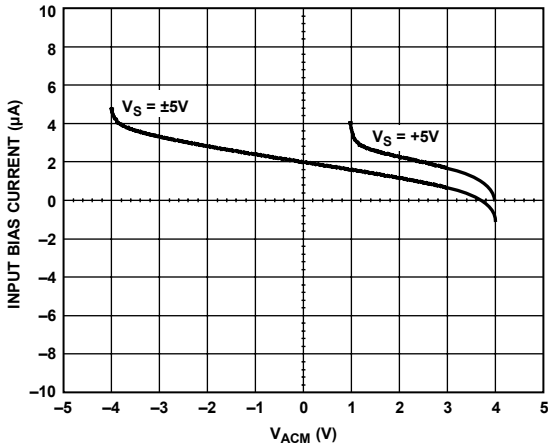


Figure 50. Input Bias Current vs. Input Common-Mode Voltage

04679-073

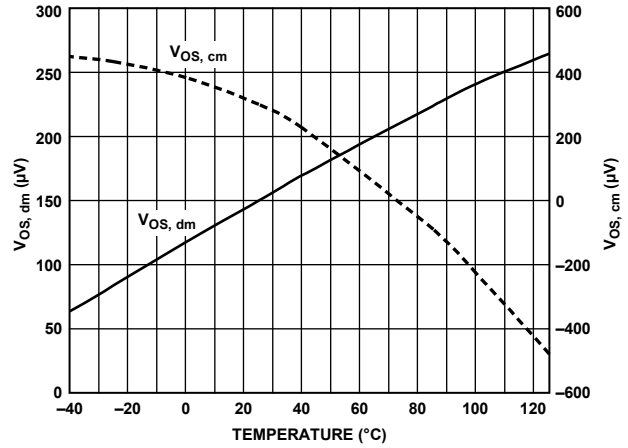


Figure 53. Offset Voltage vs. Temperature

04679-061

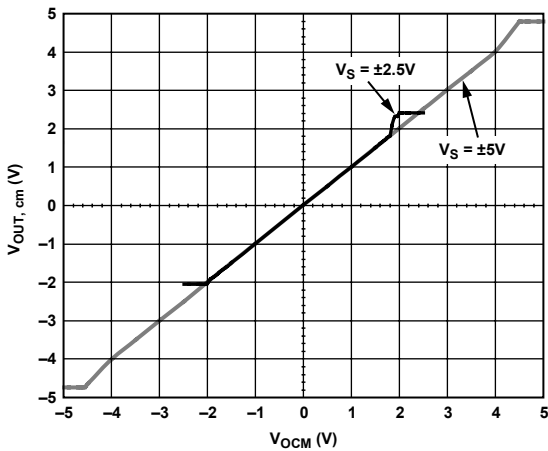


Figure 51.  $V_{OUT, cm}$  vs.  $V_{OCM}$  Input Voltage

04679-048

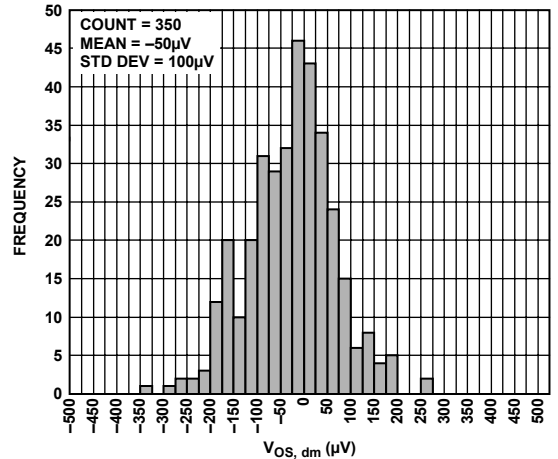


Figure 54.  $V_{OS, dm}$  Distribution

04679-071



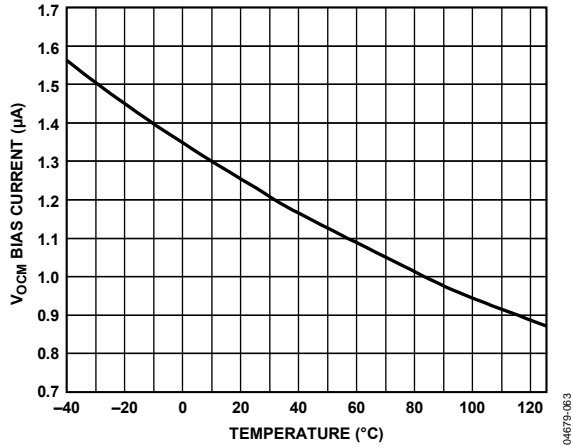


Figure 55. Vocm Bias Current vs. Temperature

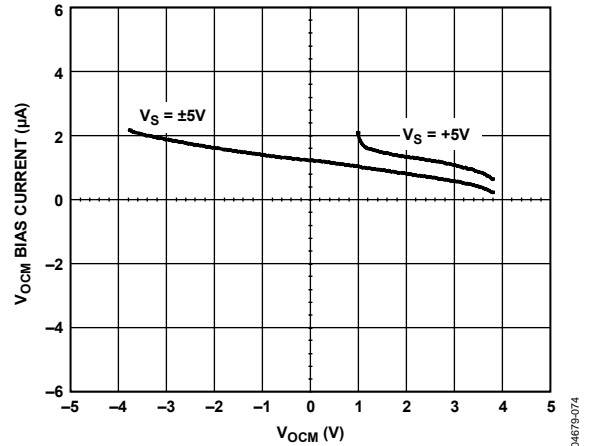


Figure 56. Vocm Bias Current vs. Vocm Input Voltage

TEST CIRCUITS

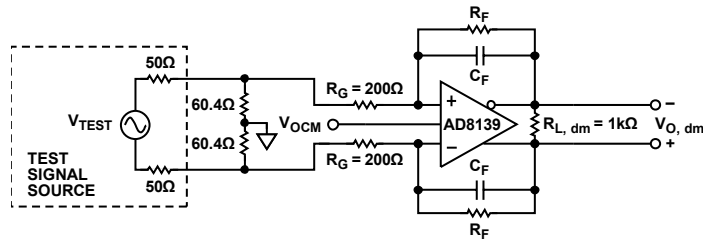


Figure 57. Basic Test Circuit

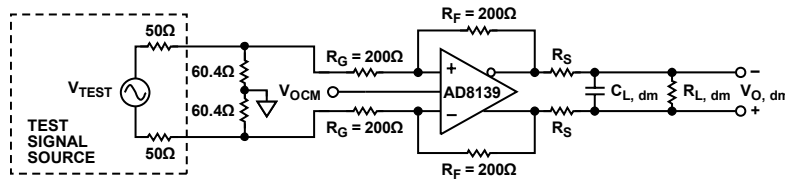


Figure 58. Capacitive Load Test Circuit, G = +1

## THEORY OF OPERATION

The AD8139 is a high speed, low noise differential amplifier fabricated on the Analog Devices second-generation eXtra Fast Complementary Bipolar (XFCB) process. It is designed to provide two closely balanced differential outputs in response to either differential or single-ended input signals. Differential gain is set by external resistors, similar to traditional voltage-feedback operational amplifiers. The common-mode level of the output voltage is set by a voltage at the  $V_{OCM}$  pin and is independent of the input common-mode voltage. The AD8139 has an H-bridge input stage for high slew rate, low noise, and low distortion operation and rail-to-rail output stages that provide maximum dynamic output range. This set of features allows for convenient single-ended-to-differential conversion, a common need to take advantage of modern high resolution ADCs with differential inputs.

### TYPICAL CONNECTION AND DEFINITION OF TERMS

Figure 59 shows a typical connection for the AD8139, using matched external  $R_F/R_G$  networks. The differential input terminals of the AD8139,  $V_{AP}$  and  $V_{AN}$ , are used as summing junctions. An external reference voltage applied to the  $V_{OCM}$  terminal sets the output common-mode voltage. The two output terminals,  $V_{OP}$  and  $V_{ON}$ , move in opposite directions in a balanced fashion in response to an input signal.

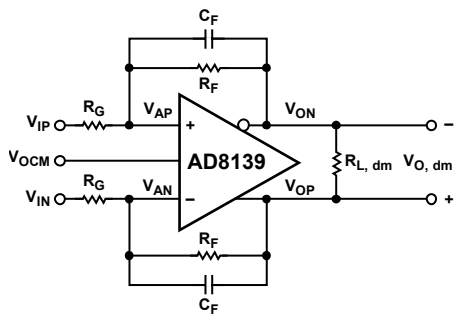


Figure 59. Typical Connection

The differential output voltage is defined as

$$V_{O, dm} = V_{OP} - V_{ON} \quad (1)$$

Common-mode voltage is the average of two voltages. The output common-mode voltage is defined as

$$V_{O, cm} = \frac{V_{OP} + V_{ON}}{2} \quad (2)$$

### Output Balance

Output balance is a measure of how well  $V_{OP}$  and  $V_{ON}$  are matched in amplitude and how precisely they are  $180^\circ$  out of phase with each other. It is the internal common-mode feedback loop that forces the signal component of the output common-mode towards zero, resulting in the near perfectly balanced differential

outputs of identical amplitude and exactly  $180^\circ$  out of phase. The output balance performance does not require tightly matched external components, nor does it require that the feedback factors of each loop be equal to each other. Low frequency output balance is limited ultimately by the mismatch of an on-chip voltage divider, which is trimmed for optimum performance.

Output balance is measured by placing a well-matched resistor divider across the differential voltage outputs and comparing the signal at the midpoint of the divider with the magnitude of the differential output. By this definition, output balance is equal to the magnitude of the change in output common-mode voltage divided by the magnitude of the change in output differential-mode voltage:

$$\text{Output Balance} = \frac{\Delta V_{O, cm}}{\Delta V_{O, dm}} \quad (3)$$

The block diagram of the AD8139 in Figure 60 shows the external differential feedback loop ( $R_F/R_G$  networks and the differential input transconductance amplifier,  $G_{DIFF}$ ) and the internal common-mode feedback loop (voltage divider across  $V_{OP}$  and  $V_{ON}$  and the common-mode input transconductance amplifier,  $G_{CM}$ ). The differential negative feedback drives the voltages at the summing junctions  $V_{AN}$  and  $V_{AP}$  to be essentially equal to each other.

$$V_{AN} = V_{AP} \quad (4)$$

The common-mode feedback loop drives the output common-mode voltage, sampled at the midpoint of the two  $500\ \Omega$  resistors, to equal the voltage set at the  $V_{OCM}$  terminal. This ensures that

$$V_{OP} = V_{OCM} + \frac{V_{O, dm}}{2} \quad (5)$$

and

$$V_{ON} = V_{OCM} - \frac{V_{O, dm}}{2} \quad (6)$$

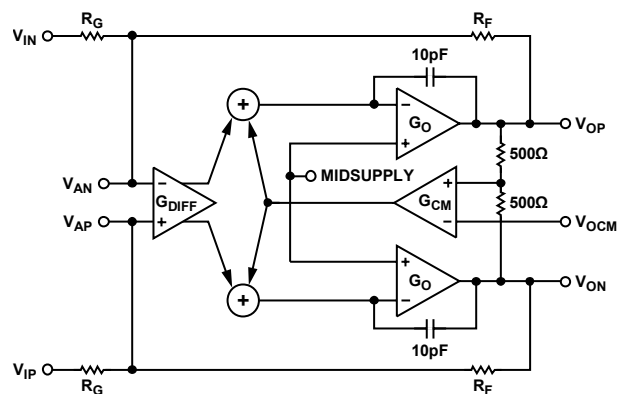


Figure 60. Block Diagram

## APPLICATIONS

### ESTIMATING NOISE, GAIN, AND BANDWIDTH WITH MATCHED FEEDBACK NETWORKS

#### Estimating Output Noise Voltage

The total output noise is calculated as the root-sum-squared total of several statistically independent sources. Because the sources are statistically independent, the contributions of each must be individually included in the root-sum-square calculation. Table 6 lists recommended resistor values and estimates of bandwidth and output differential voltage noise for various closed-loop gains. For most applications, 1% resistors are sufficient.

**Table 6. Recommended Values of Gain-Setting Resistors and Voltage Noise for Various Closed-Loop Gains**

Gain	R <sub>G</sub> (Ω)	R <sub>F</sub> (Ω)	3 dB Bandwidth (MHz)	Total Output Noise (nV/√Hz)
1	200	200	400	5.8
2	200	400	160	9.3
5	200	1 k	53	19.7
10	200	2 k	26	37

The differential output voltage noise contains contributions from the input voltage noise and input current noise of the AD8139 as well as those from the external feedback networks.

The contribution from the input voltage noise spectral density is computed as

$$V_{o\_n1} = v_n \left( 1 + \frac{R_F}{R_G} \right), \text{ or equivalently, } v_n / \beta \quad (7)$$

where  $v_n$  is defined as the input-referred differential voltage noise. This equation is the same as that of traditional op amps.

The contribution from the input current noise of each input is computed as

$$V_{o\_n2} = i_n (R_F) \quad (8)$$

where  $i_n$  is defined as the input noise current of one input. Each input needs to be treated separately because the two input currents are statistically independent processes.

The contribution from each  $R_G$  is computed as

$$V_{o\_n3} = \sqrt{4kTR_G} \left( \frac{R_F}{R_G} \right) \quad (9)$$

This result can be intuitively viewed as the thermal noise of each  $R_G$  multiplied by the magnitude of the differential gain.

The contribution from each  $R_F$  is computed as

$$V_{o\_n4} = \sqrt{4kTR_F} \quad (10)$$

#### Voltage Gain

The behavior of the node voltages of the single-ended-to-differential output topology can be deduced from the previous definitions. Referring to Figure 59, ( $C_F = 0$ ) and setting  $V_{IN} = 0$ , one can write

$$\frac{V_{IP} - V_{AP}}{R_G} = \frac{V_{AP} - V_{ON}}{R_F} \quad (11)$$

$$V_{AN} = V_{AP} = V_{OP} \left[ \frac{R_G}{R_F + R_G} \right] \quad (12)$$

Solving the above two equations and setting  $V_{IP}$  to  $V_i$  gives the gain relationship for  $V_{O, dm}/V_i$ .

$$V_{OP} - V_{ON} = V_{O, dm} = \frac{R_F}{R_G} V_i \quad (13)$$

An inverting configuration with the same gain magnitude can be implemented by simply applying the input signal to  $V_{IN}$  and setting  $V_{IP} = 0$ . For a balanced differential input, the gain from  $V_{IN, dm}$  to  $V_{O, dm}$  is also equal to  $R_F/R_G$ , where  $V_{IN, dm} = V_{IP} - V_{IN}$ .

#### Feedback Factor Notation

When working with differential amplifiers, it is convenient to introduce the feedback factor  $\beta$ , which is defined as

$$\beta = \frac{R_G}{R_F + R_G} \quad (14)$$

This notation is consistent with conventional feedback analysis and is very useful, particularly when the two feedback loops are not matched.

#### Input Common-Mode Voltage

The linear range of the  $V_{AN}$  and  $V_{AP}$  terminals extends to within approximately 1 V of either supply rail. Because  $V_{AN}$  and  $V_{AP}$  are essentially equal to each other, they are both equal to the input common-mode voltage of the amplifier. Their range is indicated in the Specifications tables as input common-mode range. The voltage at  $V_{AN}$  and  $V_{AP}$  for the connection diagram in Figure 59 can be expressed as

$$V_{AN} = V_{AP} = V_{ACM} = \left( \frac{R_F}{R_F + R_G} \times \frac{(V_{IP} + V_{IN})}{2} \right) + \left( \frac{R_G}{R_F + R_G} \times V_{OCM} \right) \quad (15)$$

where  $V_{ACM}$  is the common-mode voltage present at the amplifier input terminals.

Using the  $\beta$  notation, Equation 15 can be written as follows:

$$V_{ACM} = \beta V_{OCM} + (1 - \beta) V_{ICM} \quad (16)$$

or equivalently,

$$V_{ACM} = V_{ICM} + \beta(V_{OCM} - V_{ICM}) \quad (17)$$

where  $V_{ICM}$  is the common-mode voltage of the input signal, that is,  $V_{ICM} = V_{IP} + V_{IN}/2$ .





### Driving a Capacitive Load

A purely capacitive load reacts with the bondwire and pin inductance of the AD8139, resulting in high frequency ringing in the transient response and loss of phase margin. One way to minimize this effect is to place a small resistor in series with each output to buffer the load capacitance (see Figure 58 and Figure 63). The resistor and load capacitance form a first-order, low-pass filter; therefore, the resistor value should be as small as possible. In some cases, the ADCs require small series resistors to be added on their inputs.

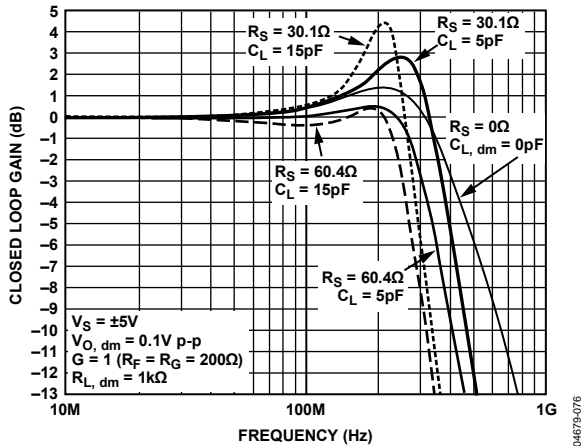


Figure 63. Frequency Response for Various Capacitive Load and Series Resistance

The Typical Performance Characteristics that illustrate transient response vs. the capacitive load were generated using series resistors in each output and a differential capacitive load.

### Layout Considerations

Standard high speed PCB layout practices should be adhered to when designing with the AD8139. A solid ground plane is recommended, and good wideband power supply decoupling networks should be placed as close as possible to the supply pins.

To minimize stray capacitance at the summing nodes, the copper in all layers under all traces and pads that connect to the summing nodes should be removed. Small amounts of stray summing-node capacitance cause peaking in the frequency response, and large amounts can cause instability. If some stray summing-node capacitance is unavoidable, its effects can be compensated for by placing small capacitors across the feedback resistors.

### Terminating a Single-Ended Input

Controlled impedance interconnections are used in most high speed signal applications, and they require at least one line termination. In analog applications, a matched resistive termination is generally placed at the load end of the line. This section deals with how to properly terminate a single-ended input to the AD8139.

The input resistance presented by the AD8139 input circuitry is seen in parallel with the termination resistor, and its loading effect must be taken into account. The Thevenin equivalent circuit of the driver, its source resistance, and the termination resistance must all be included in the calculation as well. An exact solution to the problem requires the solution of several simultaneous algebraic equations and is beyond the scope of this data sheet. An iterative solution is also possible and simpler, especially considering the fact that standard 1% resistor values are generally used.

Figure 64 shows the AD8139 in a unity-gain configuration driving the AD6645, which is a 14-bit, high speed ADC, and with the following discussion, provides a good example of how to provide a proper termination in a 50  $\Omega$  environment.

The termination resistor,  $R_T$ , in parallel with the 268  $\Omega$  input resistance of the AD8139 circuit (calculated using Equation 19), yields an overall input resistance of 50  $\Omega$  that is seen by the signal source. To have matched feedback loops, each loop must have the same  $R_G$  if they have the same  $R_F$ . In the input (upper) loop,  $R_G$  is equal to the 200  $\Omega$  resistor in series with the (+) input plus the parallel combination of  $R_T$  and the source resistance of 50  $\Omega$ . In the upper loop,  $R_G$  is therefore equal to 228  $\Omega$ . The closest standard 1% value to 228  $\Omega$  is 226  $\Omega$  and is used for  $R_G$  in the lower loop. Greater accuracy could be achieved by using two resistors in series to obtain a resistance closer to 228  $\Omega$ .

Things get more complicated when it comes to determining the feedback resistor values. The amplitude of the signal source generator  $V_s$  is two times the amplitude of its output signal when terminated in 50  $\Omega$ . Therefore, a 2 V p-p terminated amplitude is produced by a 4 V p-p amplitude from  $V_s$ . The Thevenin equivalent circuit of the signal source and  $R_T$  must be used when calculating the closed-loop gain, because in the upper loop,  $R_G$  is split between the 200  $\Omega$  resistor and the Thevenin resistance looking back toward the source. The Thevenin voltage of the signal source is greater than the signal source output voltage when terminated in 50  $\Omega$  because  $R_T$  must always be greater than 50  $\Omega$ . In this case,  $R_T$  is 61.9  $\Omega$  and the Thevenin voltage and resistance are 2.2 V p-p and 28  $\Omega$ , respectively. Now the upper input branch can be viewed as a 2.2 V p-p source in series with 228  $\Omega$ . Because this is a unity-gain application, a 2 V p-p differential output is required, and  $R_F$  must therefore be  $228 \times (2/2.2) = 206 \Omega$ . The closest standard value to this is 205  $\Omega$ .

When generating the Typical Performance Characteristics data, the measurements were calibrated to take the effects of the terminations on the closed-loop gain into account.

Because this is a single-ended-to-differential application on a single supply, the input common-mode voltage swing must be checked. From Figure 64,  $\beta = 0.52$ ,  $V_{OCM} = 2.4\text{ V}$ , and  $V_{ICM}$  is 1.1 V p-p swinging about ground. Using Equation 16,  $V_{ACM}$  is calculated to be 0.53 V p-p swinging about a baseline of 1.25 V, and the minimum negative excursion is approximately 1 V.

**Exposed Paddle (EP)**

The 8-lead SOIC and the 8-lead LFCSP have an exposed paddle on the bottom of the package. To achieve the specified thermal resistance, the exposed paddle must be soldered to one of the PCB planes. The exposed paddle mounting pad should contain several thermal vias within it to ensure a low thermal path to the plane.

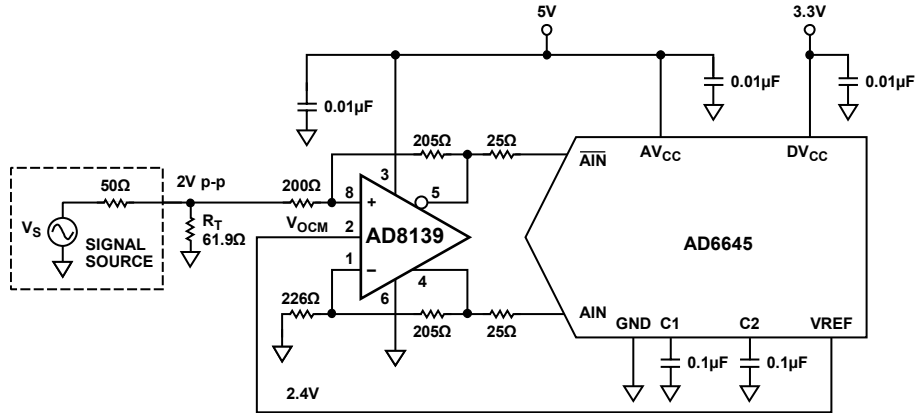
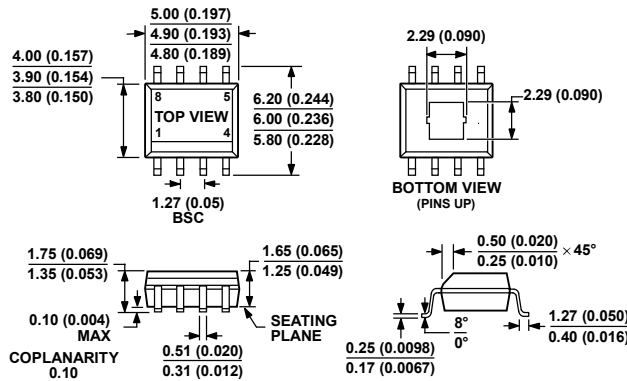


Figure 64. AD8139 Driving AD6645, 14-Bit, 80 MSPS/105 MSPS ADC

04679-054

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETER; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 65. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC\_N\_EP] Narrow Body (RD-8-1)—Dimensions shown in millimeters and (inches)

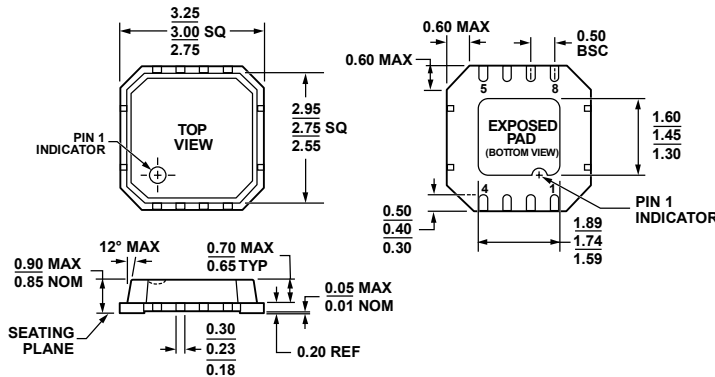


Figure 66. 8-Lead Lead Frame Chip Scale Package [LFCSP\_VD] 3 mm x 3 mm Body, Very Thin, Dual Lead (CP-8-2)—Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8139ARD	-40°C to +125°C	8-Lead Small Outline Package with Exposed Pad (SOIC_N_EP)	RD-8-1	
AD8139ARD-REEL	-40°C to +125°C	8-Lead Small Outline Package with Exposed Pad (SOIC_N_EP)	RD-8-1	
AD8139ARD-REEL7	-40°C to +125°C	8-Lead Small Outline Package with Exposed Pad (SOIC_N_EP)	RD-8-1	
AD8139ARDZ <sup>1</sup>	-40°C to +125°C	8-Lead Small Outline Package with Exposed Pad (SOIC_N_EP)	RD-8-1	
AD8139ARDZ-REEL <sup>1</sup>	-40°C to +125°C	8-Lead Small Outline Package with Exposed Pad (SOIC_N_EP)	RD-8-1	
AD8139ARDZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead Small Outline Package with Exposed Pad (SOIC_N_EP)	RD-8-1	
AD8139ACP-R2	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HEB
AD8139ACP-REEL	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HEB
AD8139ACP-REEL7	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HEB
AD8139ACPZ-R2 <sup>1</sup>	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HEB#
AD8139ACPZ-REEL <sup>1</sup>	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HEB#
AD8139ACPZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HEB#

<sup>1</sup> Z = RoHS Compliant Part, # denotes RoHS product may be top or bottom marked.