Ultralow Noise VGAs with Preamplifier and Programmable R_{IN}

AD8331/AD8332/AD8334

FEATURES

Ultralow noise preamplifier
- **Voltage noise = 0.74 nV/√Hz**
- **Current noise = 2.5 pA/√Hz**

3 dB bandwidth
- **AD8331: 120 MHz**
- **AD8332, AD8334: 100 MHz**

Low power
- **AD8331: 125 mW/channel**
- **AD8332, AD8334: 145 mW/channel**

Wide gain range with programmable postamp
- **–4.5 dB to +43.5 dB**
- **+7.5 dB to +55.5 dB**

Low output-referred noise: 48 nV/√Hz typical
Active input impedance matching
Optimized for 10-bit/12-bit ADCs
Selectable output clamping level
Single 5 V supply operation
AD8332 and AD8334 available in lead frame chip scale package

APPLICATIONS

Ultrasound and sonar time-gain controls
High performance AGC systems
I/Q signal processing
High speed, dual ADC drivers

GENERAL DESCRIPTION

The AD8331/AD8332/AD8334 are single-, dual-, and quad-channel ultralow noise, linear-in-dB, variable gain amplifiers (VGAs). Optimized for ultrasound systems, they are usable as a low noise variable gain element at frequencies up to 120 MHz.

Included in each channel are an ultralow noise preamplifier (LNA), an X-AMP® VGA with 48 dB of gain range, and a selectable gain postamplifier with adjustable output limiting. The LNA gain is 19 dB with a single-ended input and differential outputs. Using a single resistor, the LNA input impedance can be adjusted to match a signal source without compromising noise performance.

The 48 dB gain range of the VGA makes these devices suitable for a variety of applications. Excellent bandwidth uniformity is maintained across the entire range. The gain control interface provides precise linear-in-dB scaling of 50 dB/V for control voltages between 40 mV and 1 V. Factory trim ensures excellent part-to-part and channel-to-channel gain matching.

FUNCTIONAL BLOCK DIAGRAM

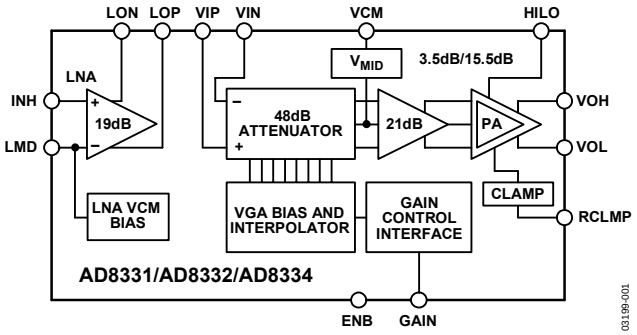


Figure 1. Signal Path Block Diagram

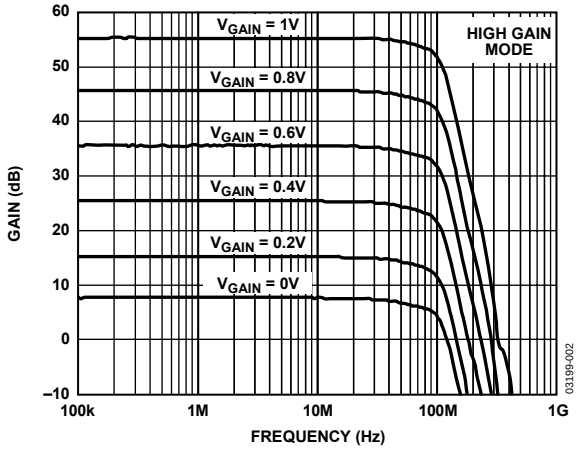


Figure 2. Frequency Response vs. Gain

Differential signal paths result in superb second- and third-order distortion performance and low crosstalk.

The VGA's low output-referred noise is advantageous in driving high speed differential ADCs. The gain of the postamplifier can be pin selected to 3.5 dB or 15.5 dB to optimize gain range and output noise for 12-bit or 10-bit converter applications. The output can be limited to a user-selected clamping level, preventing input overload to a subsequent ADC. An external resistor adjusts the clamping level.

The operating temperature range is –40°C to +85°C. The AD8331 is available in a 20-lead QSOP package, the AD8332 is available in 28-lead TSSOP and 32-lead LFCSP packages, and the AD8334 is available in a 64-lead LFCSP package.

Rev. E
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2006 Analog Devices, Inc. All rights reserved.**

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 3
Specifications ... 4
Absolute Maximum Ratings ... 7
ESD Caution ... 7
Pin Configurations and Function Descriptions ... 8
Typical Performance Characteristics ... 12
Test Circuits ... 20
Measurement Considerations ... 20
Theory of Operation ... 24
Overview ... 24
Low Noise Amplifier (LNA) ... 25
Variable Gain Amplifier ... 27
Postamplifier ... 28
Applications ... 30
LNA—External Components ... 30
Driving ADCs ... 32
Overload ... 32
Optional Input Overload Protection. ... 33
Layout, Grounding, and Bypassing ... 33
Multiple Input Matching ... 33
Disabling the LNA ... 33
Ultrasound TGC Application ... 34
High Density Quad Layout ... 34
Outline Dimensions ... 39
Ordering Guide ... 40

REVISION HISTORY

4/06—Rev. D to Rev. E

Added AD8334 ..... Universal
Changes to Figure 1 and Figure 2 1
Changes to Table 1 4
Changes to Table 2 7
Changes to Figure 7 through Figure 9 and Figure 12 12
Changes to Figure 13, Figure 14, Figure 16, and Figure 18 13
Changes to Figure 23 and Figure 24 14
Changes to Figure 25 through Figure 27 15
Changes to Figure 31 and Figure 33 through Figure 36 16
Changes to Figure 37 through Figure 42 17
Changes to Figure 43, Figure 44, and Figure 48 18
Changes to Figure 49, Figure 50, and Figure 54 19
Inserted Figure 56 and Figure 57 20
Inserted Figure 58, Figure 59, and Figure 61 21
Changes to Figure 60 21
Inserted Figure 63 and Figure 65 22
Changes to Figure 64 22
Moved Measurement Considerations Section 20
Inserted Figure 67 and Figure 68 23
Inserted Figure 70 and Figure 71 24
Change to Figure 72 24
Changes to Figure 73 and Low Noise Amplifier Section 25
Changes to Postamplifier Section 28
Changes to Figure 80 29
Changes to LNA—External Components Section 30
Changes to Logic Inputs—ENB, MODE, and HILO Section 31
Changes to Output Decoupling and Overload Sections 32
Changes to Layout, Grounding, and Bypassing Section 33
Changes to Ultrasound TGC Application Section 34
Added High Density Quad Layout Section 34
Inserted Figure 94 38
Updated Outline Dimensions 39
Changes to Ordering Guide 40

3/06—Rev. C to Rev. D

Updated Format ..... Universal
Changes to Features and General Description 1
Changes to Table 1 3
Changes to Table 2 6
Changes to Ordering Guide 34

11/03—Rev. B to Rev. C

Addition of New Part ..... Universal
Changes to Figures ..... Universal
Updated Outline Dimensions 32

5/03—Rev. A to Rev. B

Edits to Ordering Guide 32
Edits to Ultrasound TGC Application Section 25
Added Figure 71, Figure 72, and Figure 73 26
Updated Outline Dimensions 31

2/03—Rev. 0 to Rev. A

Edits to Ordering Guide 32

SPECIFICATIONS

T_A = 25°C, V_S = 5 V, R_L = 500 Ω, R_S = R_{IN} = 50 Ω, R_{FB} = 280 Ω, C_{SH} = 22 pF, f = 10 MHz, R_{CLMP} = ∞, C_L = 1 pF, VCM pin floating, −4.5 dB to +43.5 dB gain (HILO = LO), and differential output voltage, unless otherwise specified.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
LNA CHARACTERISTICS					
Gain	Single-ended input to differential output		19		dB
	Input to output (single ended)		13		dB
Input Voltage Range	AC-coupled		±275		mV
Input Resistance	R_{FB} = 280 Ω		50		Ω
	R_{FB} = 412 Ω		75		Ω
	R_{FB} = 562 Ω		100		Ω
	R_{FB} = 1.13 kΩ		200		Ω
	R_{FB} = ∞		6		kΩ
Input Capacitance			13		pF
Output Impedance	Single-ended, either output		5		Ω
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		130		MHz
Slew Rate			650		V/µs
Input Voltage Noise	R_S = 0 Ω, HI or LO gain, R_{FB} = ∞, f = 5 MHz		0.74		nV/√Hz
Input Current Noise	R_{FB} = ∞, HI or LO gain, f = 5 MHz		2.5		pA/√Hz
Noise Figure	f = 10 MHz, LOP output				
Active Termination Match	R_S = R_{IN} = 50 Ω		3.7		dB
Unterminated	R_S = 50 Ω, R_{FB} = ∞		2.5		dB
Harmonic Distortion @ LOP1 or LOP2	V_{OUT} = 0.5 V p-p, single-ended, f = 10 MHz				
HD2			−56		dBc
HD3			−70		dBc
Output Short-Circuit Current	Pin LON, Pin LOP		165		mA
LNA + VGA CHARACTERISTICS					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p				
AD8331			120		MHz
AD8332, AD8334			100		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p				
AD8331			110		MHz
AD8332, AD8334			90		MHz
Slew Rate					
AD8331	LO gain		300		V/µs
	HI gain		1200		V/µs
AD8332, AD8334	LO gain		275		V/µs
	HI gain		1100		V/µs
Input Voltage Noise	R_S = 0 Ω, HI or LO gain, R_{FB} = ∞, f = 5 MHz		0.82		nV/√Hz
Noise Figure	V_{GAIN} = 1.0 V				
Active Termination Match	R_S = R_{IN} = 50 Ω, f = 10 MHz, measured		4.15		dB
	R_S = R_{IN} = 200 Ω, f = 5 MHz, simulated		2.0		dB
Unterminated	R_S = 50 Ω, R_{FB} = ∞, f = 10 MHz, measured		2.5		dB
	R_S = 200 Ω, R_{FB} = ∞, f = 5 MHz, simulated		1.0		dB
Output-Referred Noise					
AD8331	V_{GAIN} = 0.5 V, LO gain		48		nV/√Hz
	V_{GAIN} = 0.5 V, HI gain		178		nV/√Hz
AD8332, AD8334	V_{GAIN} = 0.5 V, LO gain		40		nV/√Hz
	V_{GAIN} = 0.5 V, HI gain		150		nV/√Hz
Output Impedance, Postamplifier	DC to 1 MHz		1		Ω

Parameter	Conditions	Min	Typ	Max	Unit
Output Signal Range, Postamplifier	$R_L \geq 500\ \Omega$, unclamped, either pin		$V_{CM} \pm 1.125$		V
Differential			4.5		V p-p
Output Offset Voltage	$V_{GAIN} = 0.5$ V				
AD8331	Differential	−50	±5	+50	mV
	Common mode	−125	−25	+100	mV
AD8332, AD8334	Differential	−20	±5	+20	mV
	Common mode	−125	−25	+100	mV
Output Short-Circuit Current			45		mA
Harmonic Distortion	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p, HI gain				
AD8331					
HD2	f = 1 MHz		−88		dBc
HD3			−85		dBc
HD2	f = 10 MHz		−68		dBc
HD3			−65		dBc
AD8332, AD8334					
HD2	f = 1 MHz		−82		dBc
HD3			−85		dBc
HD2	f = 10 MHz		−62		dBc
HD3			−66		dBc
Input 1 dB Compression Point	$V_{GAIN} = 0.25$ V, $V_{OUT} = 1$ V p-p, f = 1 MHz to 10 MHz		1		dBm[1]
Two-Tone Intermodulation Distortion (IMD3)					
AD8331	$V_{GAIN} = 0.72$ V, $V_{OUT} = 1$ V p-p, f = 1 MHz		−80		dBc
	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p, f = 10 MHz		−72		dBc
AD8332, AD8334	$V_{GAIN} = 0.72$ V, $V_{OUT} = 1$ V p-p, f = 1 MHz		−78		dBc
	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p, f = 10 MHz		−74		dBc
Output Third-Order Intercept					
AD8331	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p, f = 1 MHz		38		dBm
	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p, f = 10 MHz		33		dBm
AD8332, AD8334	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p, f = 1 MHz		35		dBm
	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p, f = 10 MHz		32		dBm
Channel-to-Channel Crosstalk (AD8332, AD8334)	$V_{GAIN} = 0.5$ V, $V_{OUT} = 1$ V p-p, f = 1 MHz		−98		dB
Overload Recovery	$V_{GAIN} = 1.0$ V, $V_{IN} = 50$ mV p-p/1 V p-p, f = 10 MHz		5		ns
Group Delay Variation	5 MHz < f < 50 MHz, full gain range		±2		ns
ACCURACY					
Absolute Gain Error[2]	$0.05\text{ V} < V_{GAIN} < 0.10$ V	−1	+0.5	+2	dB
	$0.10\text{ V} < V_{GAIN} < 0.95$ V	−1	±0.3	+1	dB
	$0.95\text{ V} < V_{GAIN} < 1.0$ V	−2	−1	+1	dB
Gain Law Conformance[3]	$0.1\text{ V} < V_{GAIN} < 0.95$ V		±0.2		dB
Channel-to-Channel Gain Matching	$0.1\text{ V} < V_{GAIN} < 0.95$ V		±0.1		dB
GAIN CONTROL INTERFACE (Pin GAIN)					
Gain Scaling Factor	$0.10\text{ V} < V_{GAIN} < 0.95$ V	48.5	50	51.5	dB/V
Gain Range	LO gain		−4.5 to +43.5		dB
	HI gain		7.5 to 55.5		dB
Input Voltage (V_{GAIN}) Range			0 to 1.0		V
Input Impedance			10		MΩ
Response Time	48 dB gain change to 90% full scale		500		ns
COMMON-MODE INTERFACE (PIN VCMn)					
Input Resistance[4]	Current limited to ±1 mA		30		Ω
Output CM Offset Voltage	$V_{CM} = 2.5$ V	−125	−25	+100	mV
Voltage Range	$V_{OUT} = 2.0$ V p-p		1.5 to 3.5		V

Parameter	Conditions	Min	Typ	Max	Unit
ENABLE INTERFACE (PIN ENB, PIN ENBL, PIN ENBV)					
Logic Level to Enable Power		2.25		5	V
Logic Level to Disable Power		0		1.0	V
Input Resistance	Pin ENB		25		kΩ
	Pin ENBL		40		kΩ
	Pin ENBV		70		kΩ
Power-Up Response Time	V_{INH} = 30 mV p-p		300		µs
	V_{INH} = 150 mV p-p		4		ms
HILO GAIN RANGE INTERFACE (PIN HILO)					
Logic Level to Select HI Gain Range		2.25		5	V
Logic Level to Select LO Gain Range		0		1.0	V
Input Resistance			50		kΩ
OUTPUT CLAMP INTERFACE (PIN RCLMP; HI OR LO GAIN)					
Accuracy					
HILO = LO	R_{CLMP} = 2.74 kΩ, V_{OUT} = 1 V p-p (clamped)		±50		mV
HILO = HI	R_{CLMP} = 2.21 kΩ, V_{OUT} = 1 V p-p (clamped)		±75		mV
MODE INTERFACE (PIN MODE)					
Logic Level for Positive Gain Slope		0		1.0	V
Logic Level for Negative Gain Slope		2.25		5	V
Input Resistance			200		kΩ
POWER SUPPLY (PIN VPS1, PIN VPS2, PIN VPSV, PIN VPSL, PIN VPOS)					
Supply Voltage		4.5	5.0	5.5	V
Quiescent Current per Channel					
AD8331		20	25		mA
AD8332, AD8334		20	29		mA
Power Dissipation per channel	No signal				
AD8331			125		mW
AD8332, AD8334			145		mW
Power-Down Current					
AD8332 (VGA and LNA Disabled)		50	300	600	µA
AD8331 (VGA and LNA Disabled)		50	240	400	µA
LNA Current					
AD8331 (ENBL)	Each channel	7.5	11	15	mA
AD8332, AD8334 (ENBL)	Each channel	7.5	12	15	mA
VGA Current					
AD8331 (ENBV)		7.5	14	20	mA
AD8332, AD8334 (ENBV)		7.5	17	20	mA
PSRR	V_{GAIN} = 0 V, f = 100 kHz		−68		dB

[1] All dBm values are referred to 50 Ω.
[2] The absolute gain refers to the theoretical gain expression in Equation 1.
[3] Best-fit to linear-in-dB curve.
[4] The current is limited to ±1 mA typical.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage (VPSn, VPSV, VPSL, VPOS)	5.5 V
Input Voltage (INHn)	V_S + 200 mV
ENB, ENBL, ENBV, HILO Voltage	V_S + 200 mV
GAIN Voltage	2.5 V
Power Dissipation	
AR Package[1]	0.96 W
CP-20 Package (AD8331)	1.63 W
CP-32 Package (AD8332)	1.97 W
RQ Package[1]	0.78 W
CP-64 Package (AD8334)	0.91 W
Temperature	
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C
θ_{JA}	
AR Package[1]	68°C/W
CP-20 Package[2]	40°C/W
CP-32 Package[2]	33°C/W
RQ Package[1]	83°C/W
CP-64 Package[3]	24.2°C/W

[1] Four-layer JEDEC board (2S2P).
[2] Exposed pad soldered to board, nine thermal vias in pad—JEDEC, 4-layer board J-STD-51-9.
[3] Exposed pad soldered to board, 25 thermal vias in pad—JEDEC, 4-layer board J-STD-51-9.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

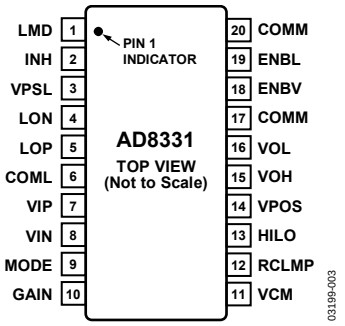


Figure 3. 20-Lead QSOP Pin Configuration (AD8331)

Table 3. 20-Lead QSOP Pin Function Description (AD8331)

Pin No.	Mnemonic	Description
1	LMD	LNA Signal Ground
2	INH	LNA Input
3	VPSL	LNA 5 V Supply
4	LON	LNA Inverting Output
5	LOP	LNA Noninverting Output
6	COML	LNA Ground
7	VIP	VGA Noninverting Input
8	VIN	VGA Inverting Input
9	MODE	Gain Slope Logic Input
10	GAIN	Gain Control Voltage
11	VCM	Common Mode Voltage
12	RCLMP	Output Clamping Level
13	HILO	Gain Range Select (HI or LO)
14	VPOS	VGA 5 V Supply
15	VOH	Noninverting VGA Output
16	VOL	Inverting VGA Output
17	COMM	VGA Ground
18	ENBV	VGA Enable
19	ENBL	LNA Enable
20	COMM	VGA Ground

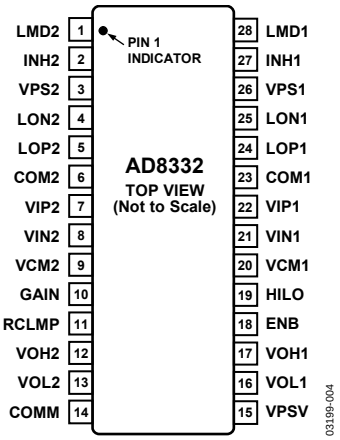


Figure 4. 28-Lead TSSOP Pin Configuration (AD8332)

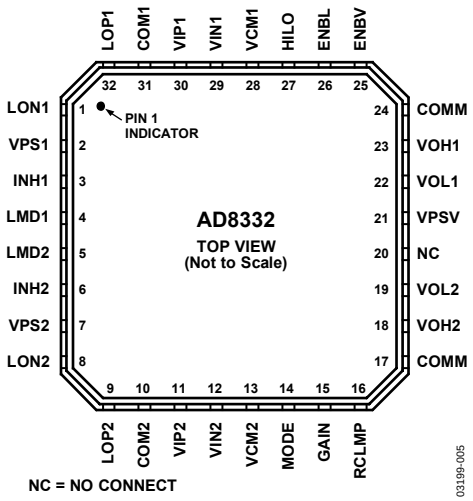


Figure 5. 32-Lead LFCSP Pin Configuration (AD8332)

Table 4. 28-Lead TSSOP Pin Function Description (AD8332)

Pin No.	Mnemonic	Description
1	LMD2	CH2 LNA Signal Ground
2	INH2	CH2 LNA Input
3	VPS2	CH2 Supply LNA 5 V
4	LON2	CH2 LNA Inverting Output
5	LOP2	CH2 LNA Noninverting Output
6	COM2	CH2 LNA Ground
7	VIP2	CH2 VGA Noninverting Input
8	VIN2	CH2 VGA Inverting Input
9	VCM2	CH2 Common-Mode Voltage
10	GAIN	Gain Control Voltage
11	RCLMP	Output Clamping Resistor
12	VOH2	CH2 Noninverting VGA Output
13	VOL2	CH2 Inverting VGA Output
14	COMM	VGA Ground (Both Channels)
15	VPSV	VGA Supply 5 V (Both Channels)
16	VOL1	CH1 Inverting VGA Output
17	VOH1	CH1 Noninverting VGA Output
18	ENB	Enable—VGA/LNA
19	HILO	VGA Gain Range Select (HI or LO)
20	VCM1	CH1 Common-Mode Voltage
21	VIN1	CH1 VGA Inverting Input
22	VIP1	CH1 VGA Noninverting Input
23	COM1	CH1 LNA Ground
24	LOP1	CH1 LNA Noninverting Output
25	LON1	CH1 LNA Inverting Output
26	VPS1	CH1 LNA Supply 5 V
27	INH1	CH1 LNA Input
28	LMD1	CH1 LNA Signal Ground

Table 5. 32-Lead LFCSP Pin Function Description (AD8332)

Pin No.	Mnemonic	Description
1	LON1	CH1 LNA Inverting Output
2	VPS1	CH1 LNA Supply 5 V
3	INH1	CH1 LNA Input
4	LMD1	CH1 LNA Signal Ground
5	LMD2	CH2 LNA Signal Ground
6	INH2	CH2 LNA Input
7	VPS2	CH2 LNA Supply 5 V
8	LON2	CH2 LNA Inverting Output
9	LOP2	CH2 LNA Noninverting Output
10	COM2	CH2 LNA Ground
11	VIP2	CH2 VGA Noninverting Input
12	VIN2	CH2 VGA Inverting Input
13	VCM2	CH2 Common-Mode Voltage
14	MODE	Gain Slope Logic Input
15	GAIN	Gain Control Voltage
16	RCLMP	Output Clamping Level Input
17	COMM	VGA Ground
18	VOH2	CH2 Noninverting VGA Output
19	VOL2	CH2 Inverting VGA Output
20	NC	No Connect
21	VPSV	VGA Supply 5 V
22	VOL1	CH1 Inverting VGA Output
23	VOH1	CH1 Noninverting VGA Output
24	COMM	VGA Ground
25	ENBV	VGA Enable
26	ENBL	LNA Enable
27	HILO	VGA Gain Range Select (HI or LO)
28	VCM1	CH1 Common-Mode Voltage
29	VIN1	CH1 VGA Inverting Input
30	VIP1	CH1 VGA Noninverting Input
31	COM1	CH1 LNA Ground
32	LOP1	CH1 LNA Noninverting Output

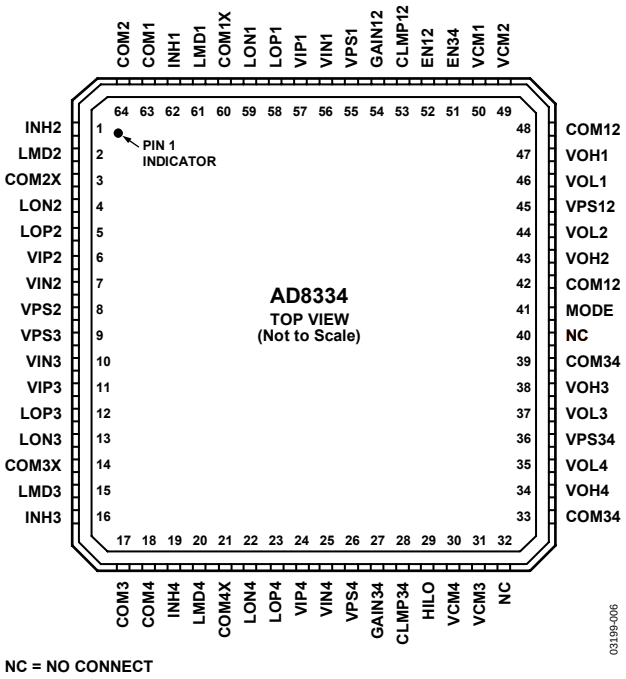


Figure 6. 64-Lead LFCSP Pin Configuration (AD8334)

Table 6. 64-Lead LFCSP Pin Function Description (AD8334)

Pin No.	Mnemonic	Description
1	INH2	CH2 LNA Input
2	LMD2	CH2 LNA V_{MID} Bypass (AC-Coupled to GND)
3	COM2X	CH2 LNA Ground Shield
4	LON2	CH2 LNA Feedback Output (for R_{FBK})
5	LOP2	CH2 LNA Output
6	VIP2	CH2 VGA Positive Input
7	VIN2	CH2VGA Negative Input
8	VPS2	CH2 LNA Supply 5 V
9	VPS3	CH3 LNA Supply 5 V
10	VIN3	CH3VGA Negative Input
11	VIP3	CH3 VGA Positive Input
12	LOP3	CH3 LNA Positive Output
13	LON3	CH3 LNA Feedback Output (for R_{FBK})
14	COM3X	CH3 LNA Ground Shield
15	LMD3	CH3 LNA V_{MID} Bypass (AC-Coupled to GND)
16	INH3	CH3 LNA Input
17	COM3	CH3 LNA Ground
18	COM4	CH4 LNA Ground
19	INH4	CH4 LNA Input
20	LMD4	CH4 LNA V_{MID} Bypass (AC-Coupled to GND)
21	COM4X	CH4 LNA Ground Shield
22	LON4	CH4 LNA Feedback Output (for R_{FBK})
23	LOP4	CH4 LNA Positive Output
24	VIP4	CH4 VGA Positive Input
25	VIN4	CH4VGA Negative Input
26	VPS4	CH4 LNA Supply 5 V
27	GAIN34	Gain Control Voltage for CH3 and CH4
28	CLMP34	Output Clamping Level Input for CH3 and CH4

Pin No.	Mnemonic	Description
29	HILO	Gain Select for Postamp 0 dB or 12 dB
30	VCM4	CH4 Common-Mode Voltage—AC Bypass
31	VCM3	CH3 Common-Mode Voltage—AC Bypass
32	NC	No Connect
33	COM34	VGA Ground, CH3 and CH4
34	VOH4	CH4 Positive VGA Output
35	VOL4	CH4 Negative VGA Output
36	VPS34	VGA Supply 5V CH3 and CH4
37	VOL3	CH3 Negative VGA Output
38	VOH3	CH3 Positive VGA Output
39	COM34	VGA ground CH3 and CH4
40	NC	No Connect
41	MODE	Gain Control SLOPE, Logic Input, 0 = Positive
42	COM12	VGA Ground CH1 and CH2
43	VOH2	CH2 Positive VGA Output
44	VOL2	CH2 Negative VGA Output
45	VPS12	CH2 VGA Supply 5 V CH1 and CH2
46	VOL1	CH1 Negative VGA Output
47	VOH1	CH1 Positive VGA Output
48	COM12	VGA Ground CH1 and CH2
49	VCM2	CH2 Common-Mode Voltage—AC Bypass
50	VCM1	CH1 Common-Mode Voltage—AC Bypass
51	EN34	Shared LNA/VGA Enable, CH3 and CH4
52	EN12	Shared LNA/VGA Enable, CH1 and CH2
53	CLMP12	Output Clamping Level Input, CH1 and CH2
54	GAIN12	Gain Control Voltage CH1 and CH2
55	VPS1	CH1 LNA Supply 5 V
56	VIN1	CH1 VGA Negative Input
57	VIP1	CH1 VGA Positive Input
58	LOP1	CH1 LNA Positive Output
59	LON1	CH1 LNA Feedback Output (for R_{FBK})
60	COM1X	CH1 LNA Ground Shield
61	LMD1	CH1 LNA V_{MID} Bypass (AC-Coupled to GND)
62	INH1	CH1 LNA Input
63	COM1	CH1 LNA Ground
64	COM2	CH2 LNA Ground

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5 V, R_L = 500 Ω, R_S = R_{IN} = 50 Ω, R_{FB} = 280 Ω, C_{SH} = 22 pF, f = 10 MHz, R_{CLMP} = ∞, C_L = 1 pF, VCM pin floating, −4.5 dB to +43.5 dB gain (HILO = LO), and differential output voltage, unless otherwise specified.

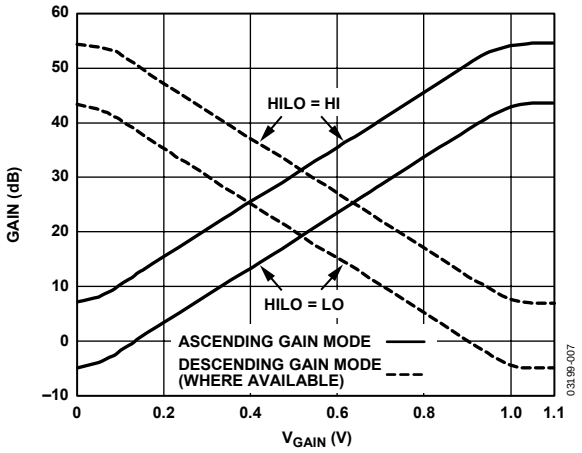


Figure 7. Gain vs. V_{GAIN} and MODE (MODE Available on AC Package)

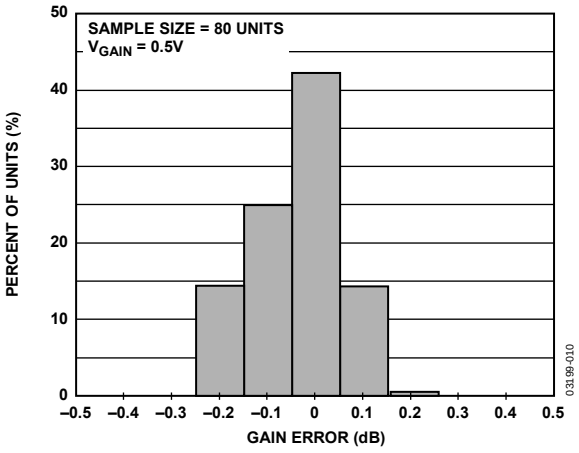


Figure 10. Gain Error Histogram

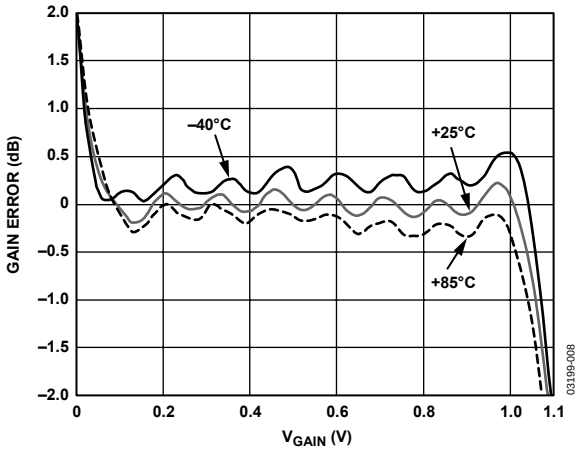


Figure 8. Absolute Gain Error vs. V_{GAIN} at Three Temperatures

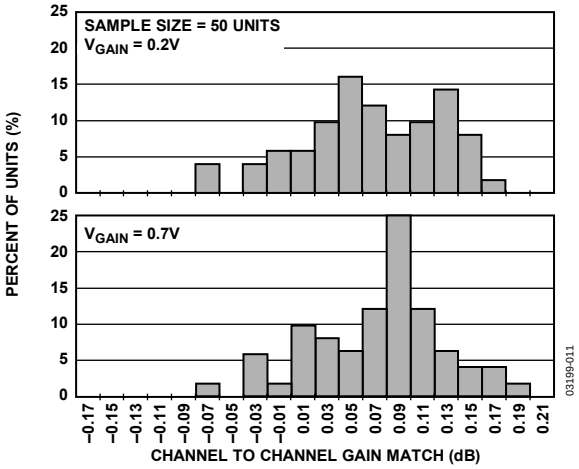


Figure 11. Gain Match Histogram for V_{GAIN} = 0.2 V and 0.7 V

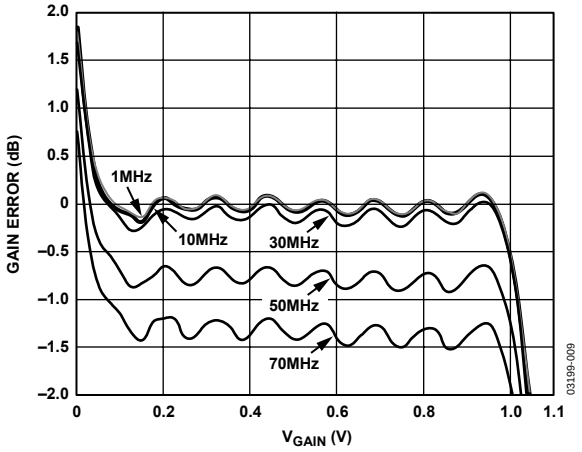


Figure 9. Absolute Gain Error vs. V_{GAIN} at Various Frequencies

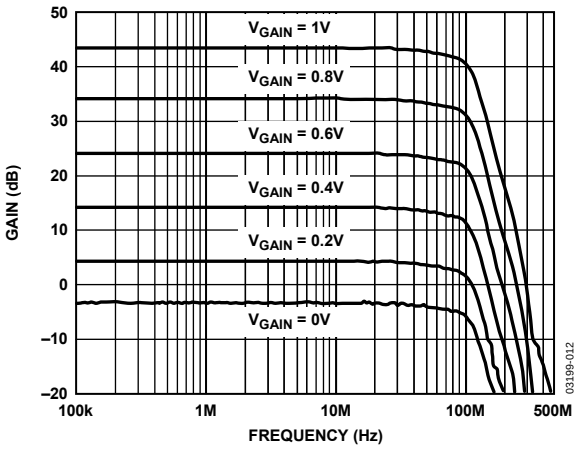


Figure 12. Frequency Response for Various Values of V_{GAIN}

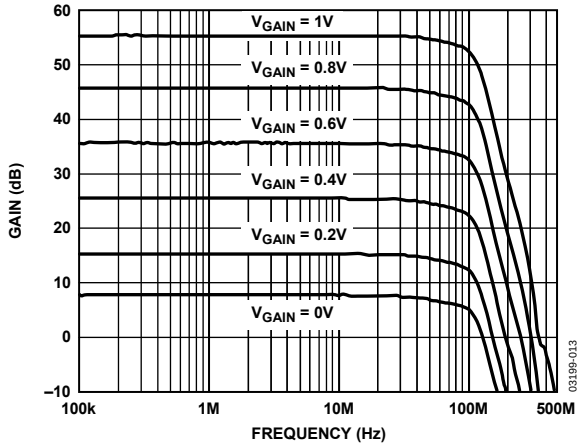


Figure 13. Frequency Response for Various Values of V_{GAIN}, HILO = HI

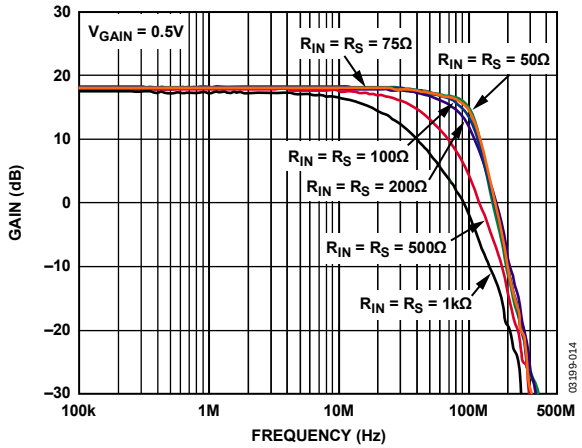


Figure 14. Frequency Response for Various Matched Source Impedances

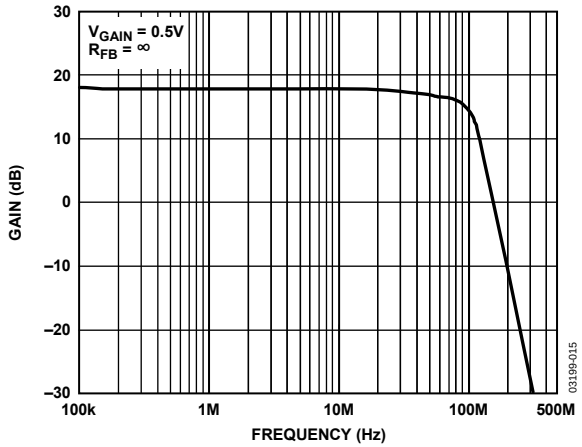


Figure 15. Frequency Response, Unterminated LNA, R_S = 50 Ω

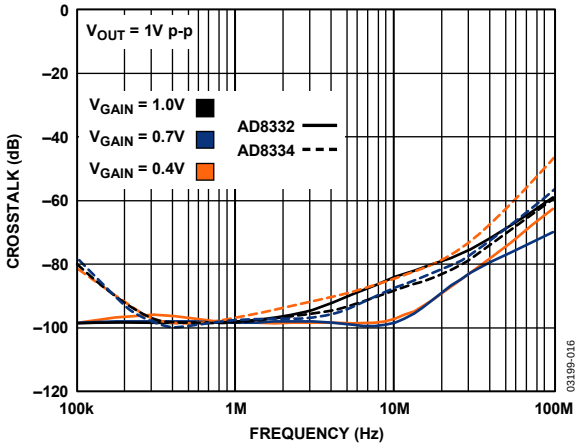


Figure 16. Channel-to-Channel Crosstalk vs. Frequency for Various Values of V_{GAIN}

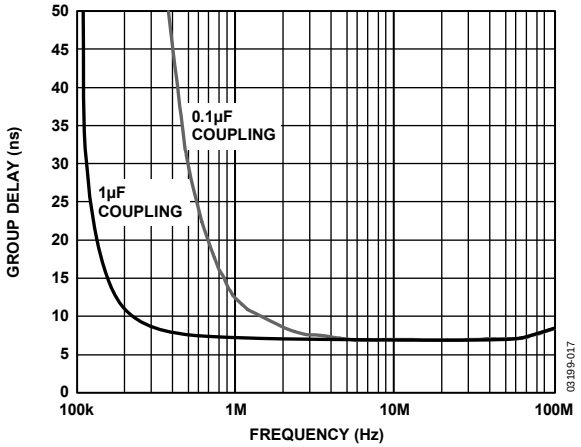


Figure 17. Group Delay vs. Frequency for Two Values of AC Coupling

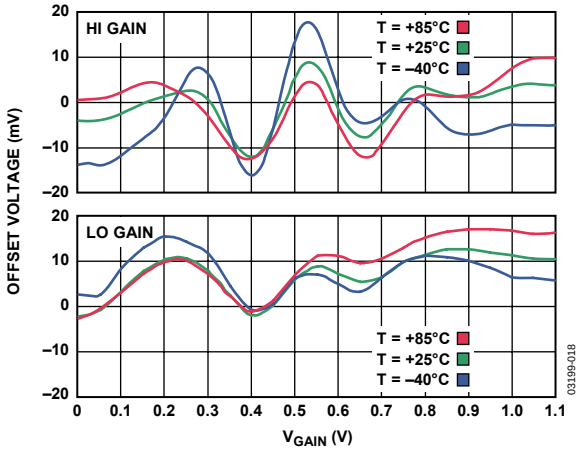


Figure 18. Representative Differential Output Offset Voltage vs. V_{GAIN} at Three Temperatures

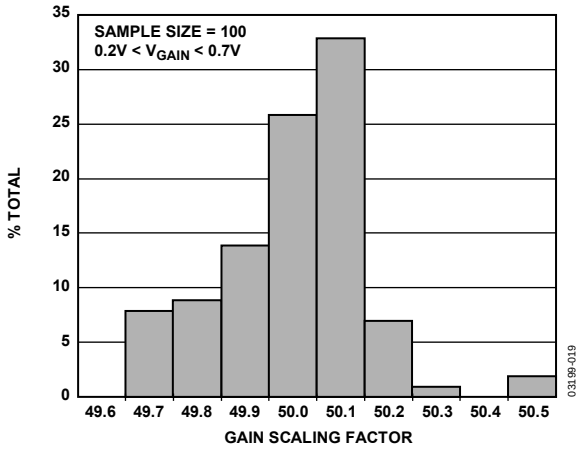


Figure 19. Gain Scaling Factor Histogram

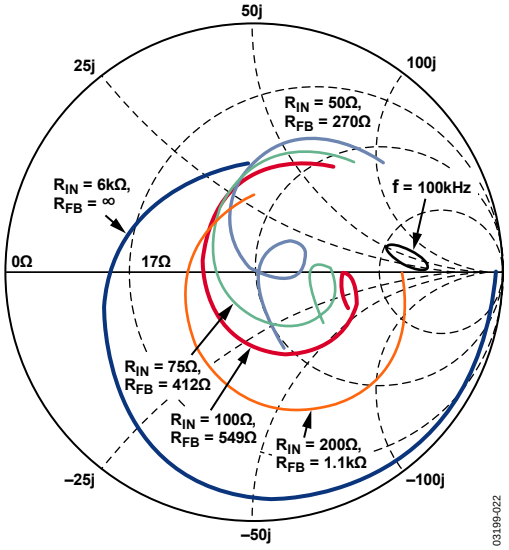


Figure 22. Smith Chart, S11 vs. Frequency, 0.1 MHz to 200 MHz for Various Values of R_{FB}

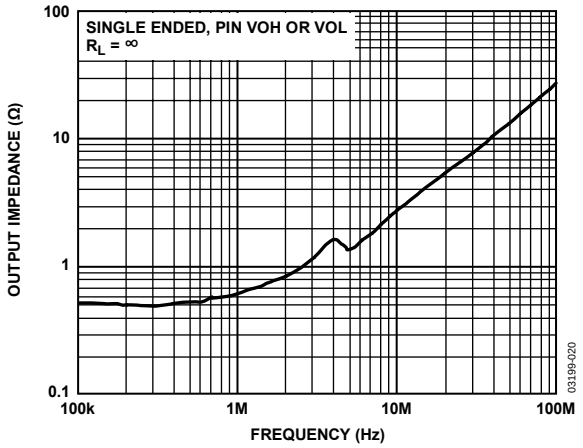


Figure 20. Output Impedance vs. Frequency

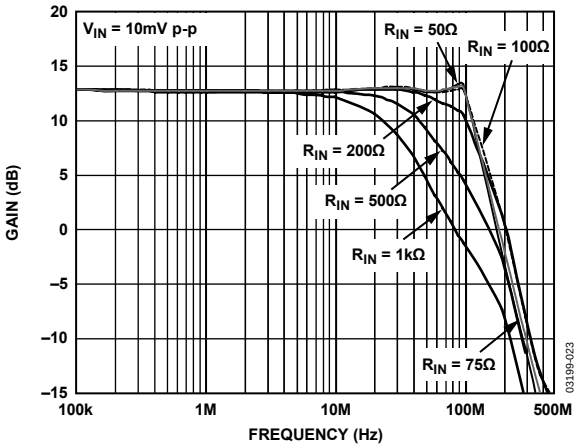


Figure 23. LNA Frequency Response, Single Ended, for Various Values of R_{IN}

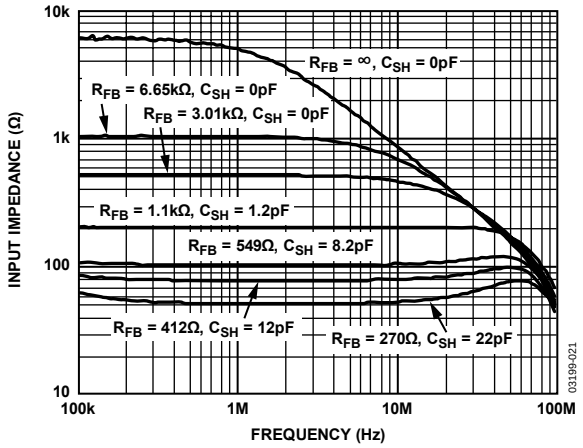


Figure 21. LNA Input Impedance vs. Frequency for Various Values of R_{FB} and C_{SH}

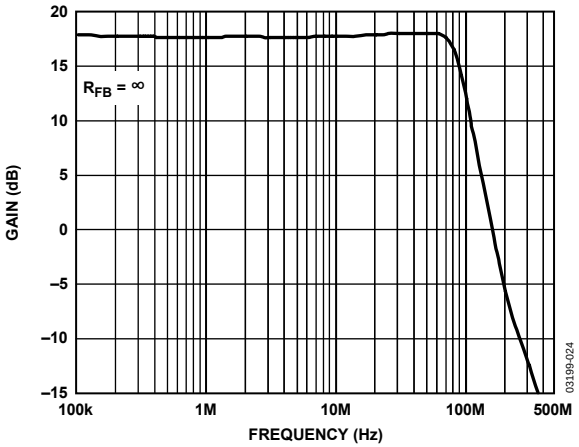


Figure 24. Frequency Response for Unterminated LNA, Single Ended

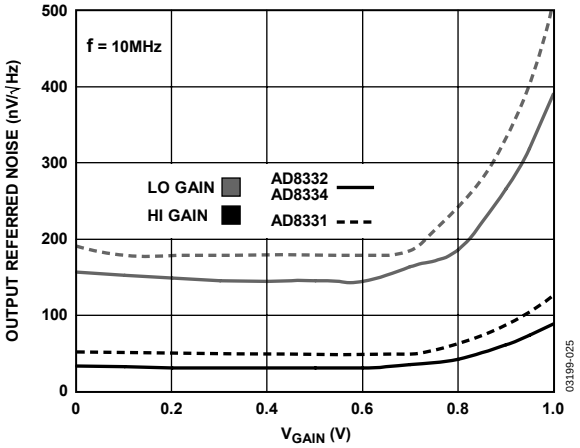


Figure 25. Output-Referred Noise vs. V_{GAIN}

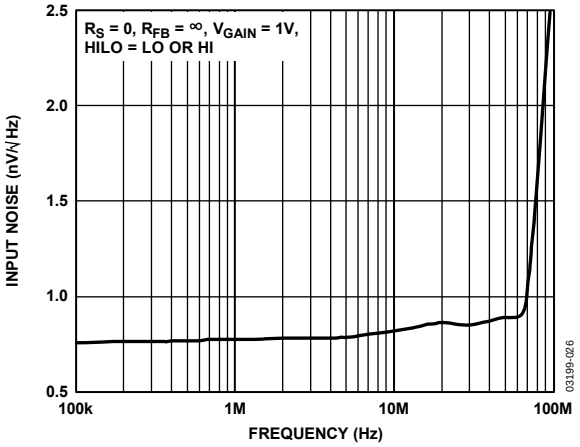


Figure 26. Short-Circuit, Input-Referred Noise vs. Frequency

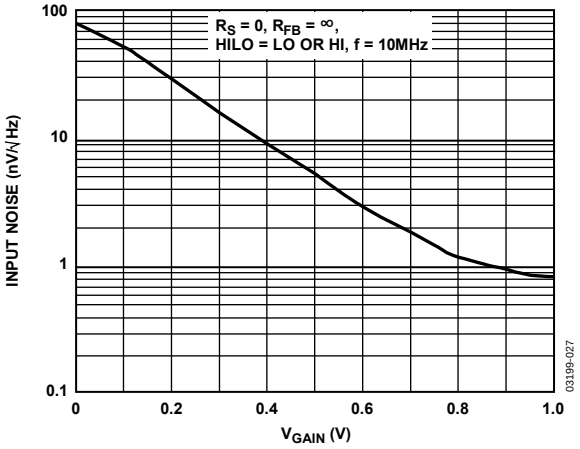


Figure 27. Short-Circuit, Input-Referred Noise vs. V_{GAIN}

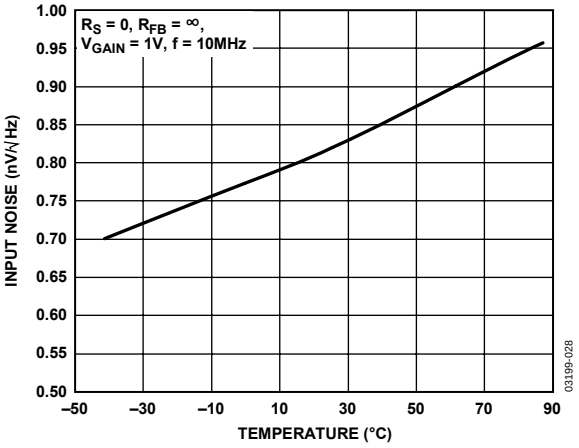


Figure 28. Short-Circuit, Input-Referred Noise vs. Temperature

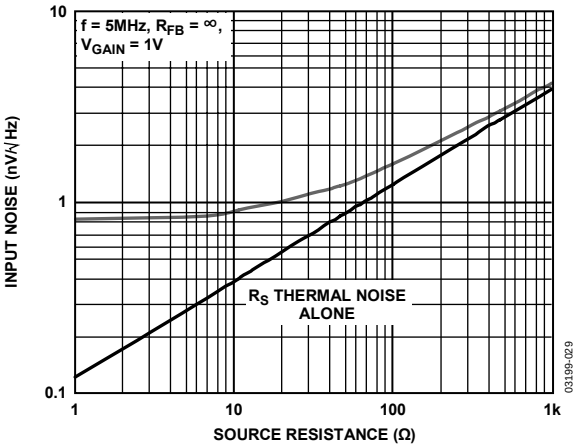


Figure 29. Input-Referred Noise vs. R_S

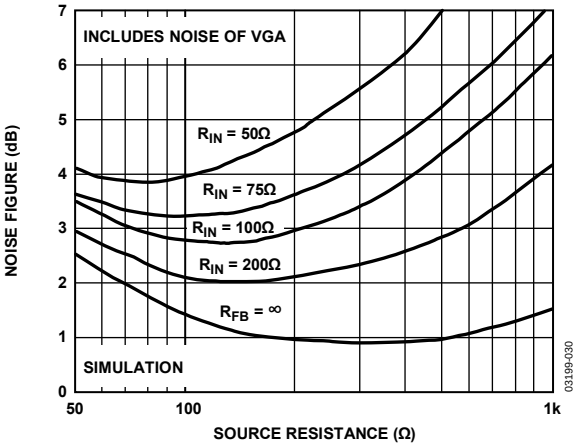


Figure 30. Noise Figure vs. R_S for Various Values of R_{IN}

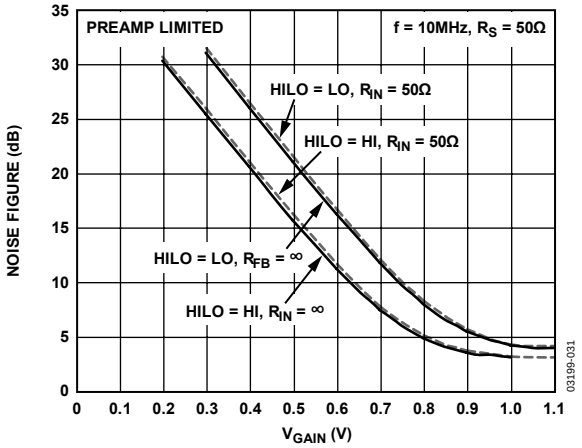


Figure 31. Noise Figure vs. V_{GAIN}

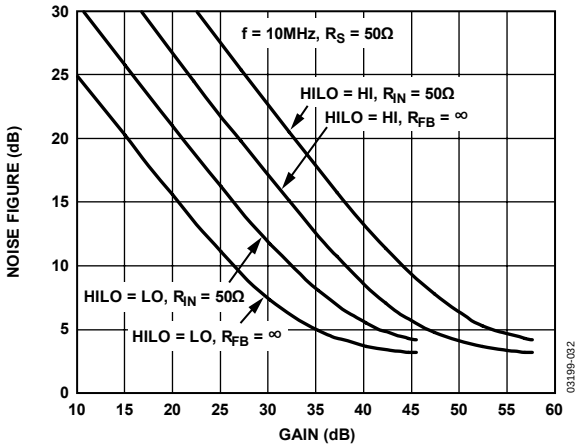


Figure 32. Noise Figure vs. Gain

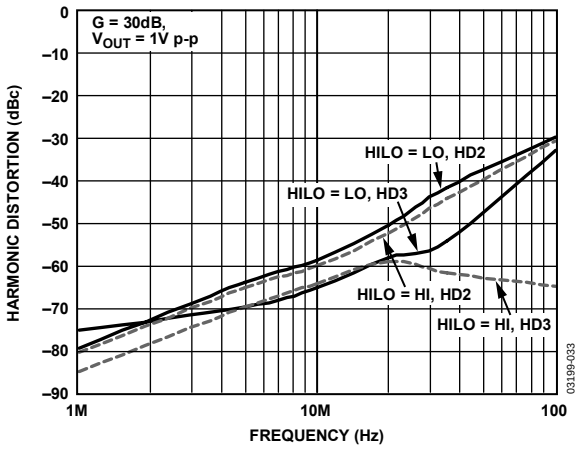


Figure 33. Harmonic Distortion vs. Frequency

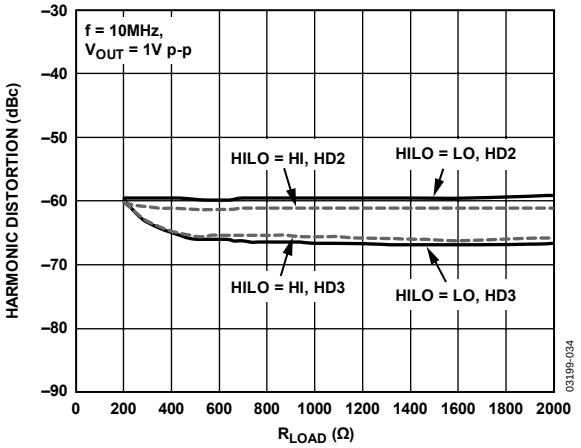


Figure 34. Harmonic Distortion vs. R_{LOAD}

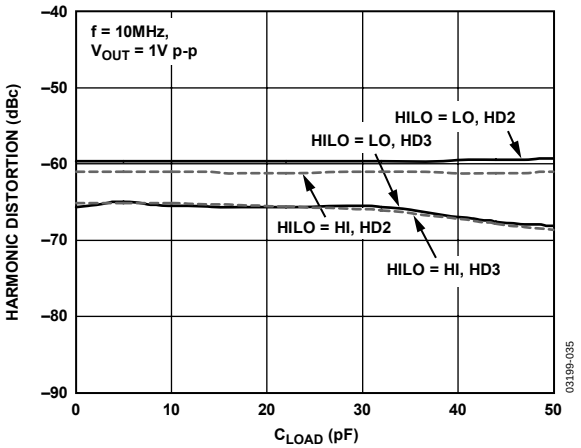


Figure 35. Harmonic Distortion vs. C_{LOAD}

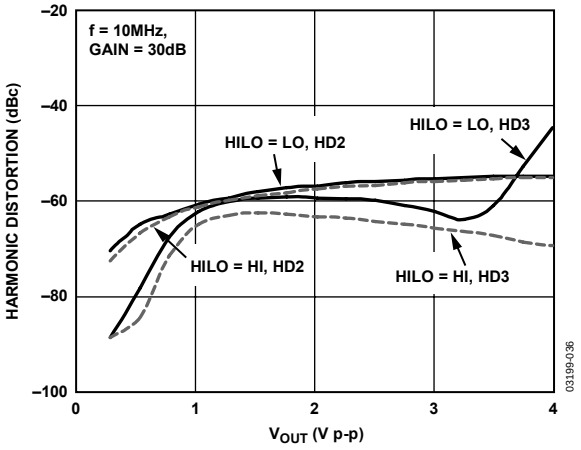


Figure 36. Harmonic Distortion vs. Differential Output Voltage

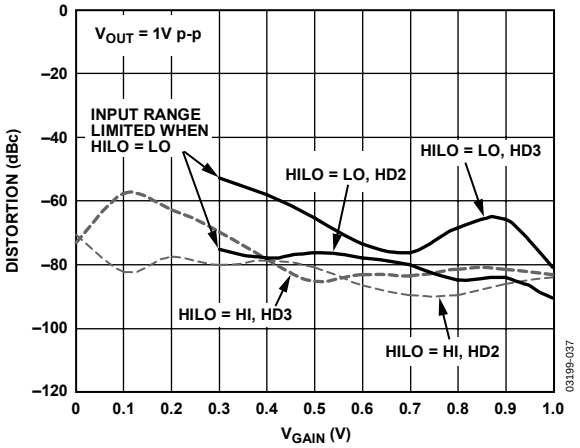


Figure 37. Harmonic Distortion vs. V_{GAIN}, f = 1 MHz

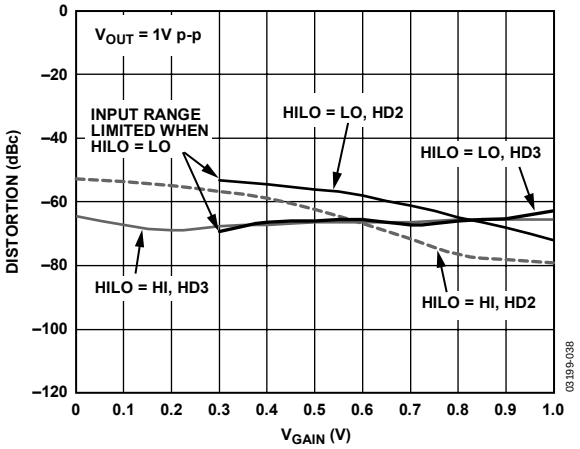


Figure 38. Harmonic Distortion vs. V_{GAIN}, f = 10 MHz

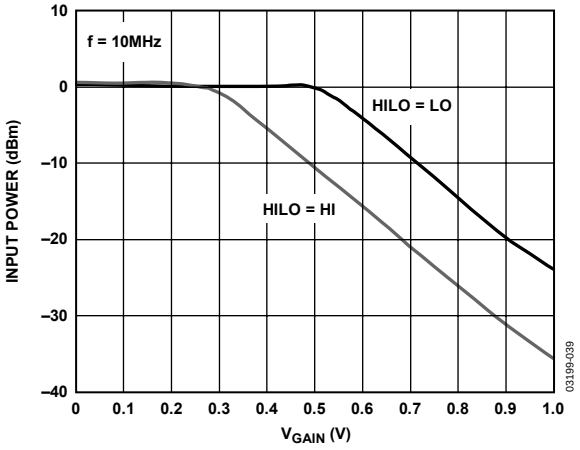


Figure 39. Input 1 dB Compression vs. V_{GAIN}

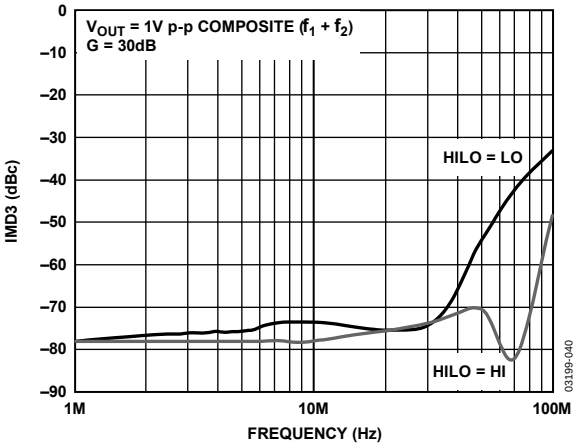


Figure 40. IMD3 vs. Frequency

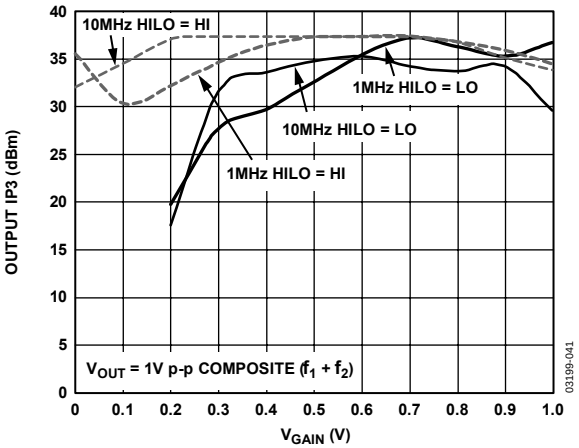


Figure 41. Output Third-Order Intercept vs. V_{GAIN}

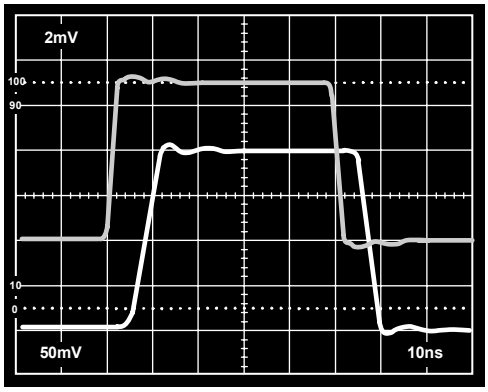


Figure 42. Small Signal Pulse Response, G = 30 dB, Top: Input, Bottom: Output Voltage, HILO = HI or LO

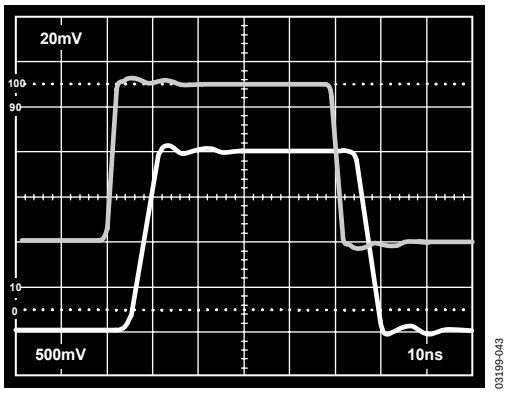


Figure 43. Large Signal Pulse Response, G = 30 dB, HILO = HI or LO, Top: Input, Bottom: Output Voltage

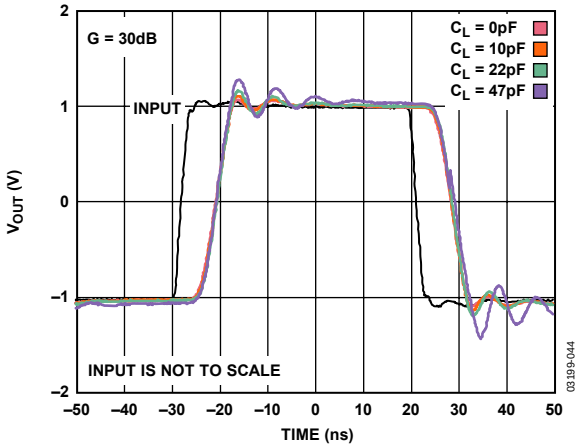


Figure 44. Large Signal Pulse Response for Various Capacitive Loads, C_L = 0 pF, 10 pF, 20 pF, 50 pF

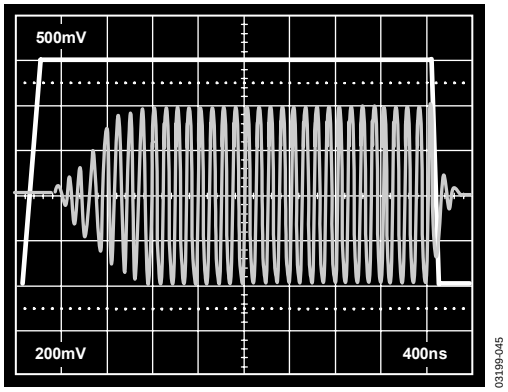


Figure 45. Pin GAIN Transient Response, Top: V_{GAIN}, Bottom: Output Voltage

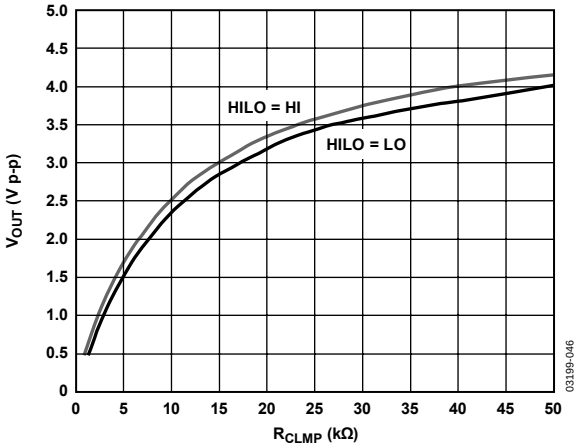


Figure 46. Clamp Level vs. R_{CLMP}

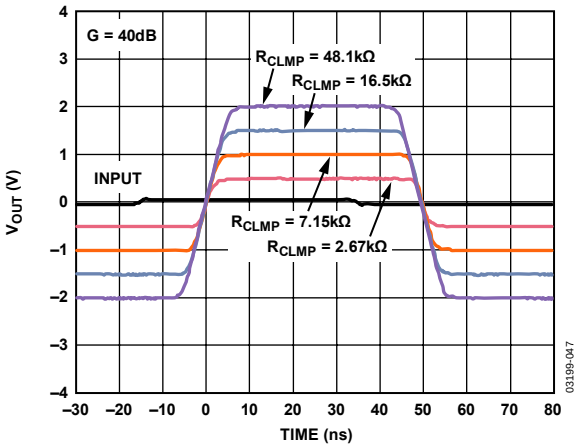


Figure 47. Clamp Level Pulse Response for 4 Values of R_{CLMP}

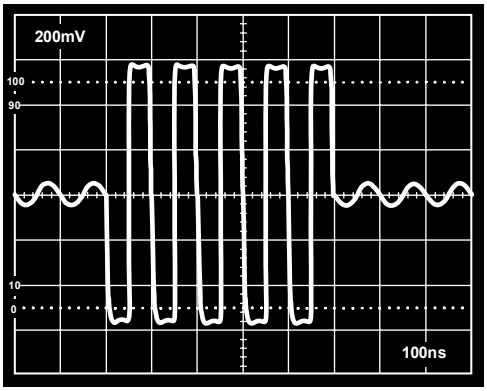


Figure 48. LNA Overdrive Recovery, V_{INH} 0.05 V p-p to 1 V p-p Burst, V_{GAIN} = 0.27 V VGA Output Shown

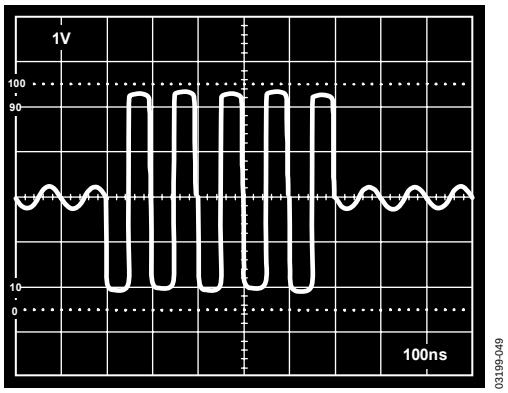


Figure 49. VGA Overdrive Recovery, V_{INH} 4 mV p-p to 70 mV p-p Burst, V_{GAIN} = 1 V VGA Output Shown Attenuated by 24 dB

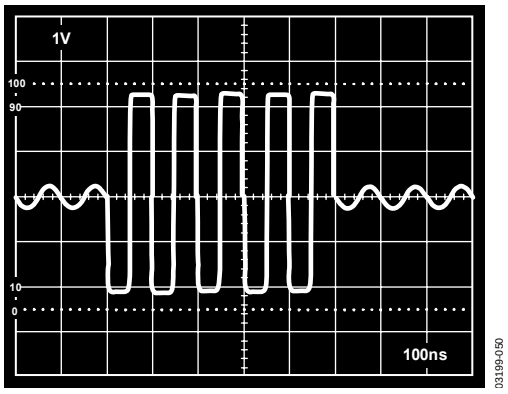


Figure 50. VGA Overdrive Recovery, V_{INH} 4 mV p-p to 275 mV p-p Burst, V_{GAIN} = 1 V VGA Output Shown Attenuated by 24 dB

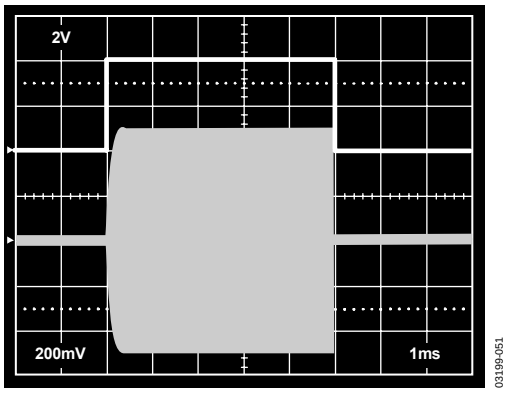


Figure 51. Enable Response, Top: V_{ENB}, Bottom: V_{OUT}, V_{INH} = 30 mV p-p

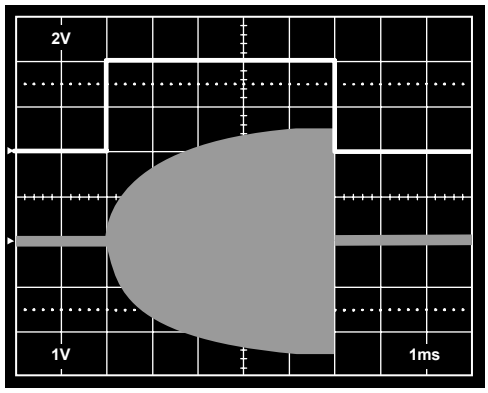


Figure 52. Enable Response, Large Signal, Top: V_{ENB}, Bottom: V_{OUT}, V_{INH} = 150 mV p-p

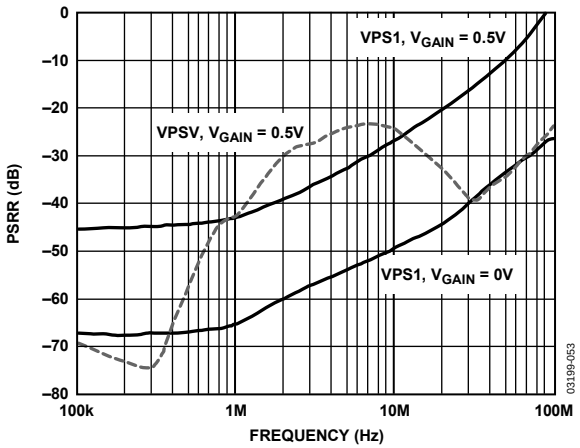


Figure 53. PSRR vs. Frequency (No Bypass Capacitor)

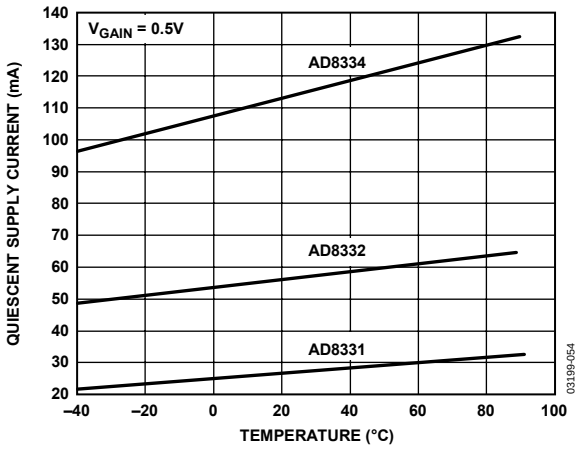


Figure 54. Quiescent Supply Current vs. Temperature

TEST CIRCUITS

MEASUREMENT CONSIDERATIONS

Figure 55 through Figure 68 show typical measurement configurations and proper interface values for measurements with 50 Ω conditions.

Short-circuit input noise measurements are made using Figure 62. The input-referred noise level is determined by dividing the output noise by the numerical gain between Point A and Point B and accounting for the noise floor of the spectrum analyzer. The gain should be measured at each frequency of interest and with low signal levels because a 50 Ω load is driven directly. The generator is removed when noise measurements are made.

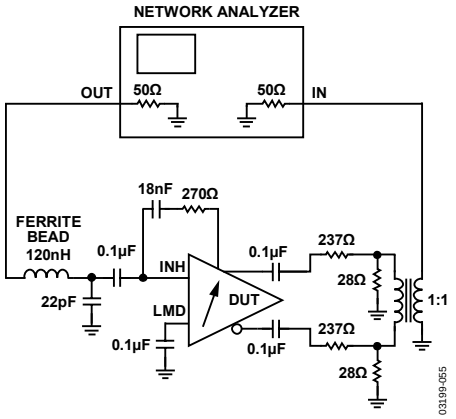


Figure 55. Gain and Bandwidth Measurements

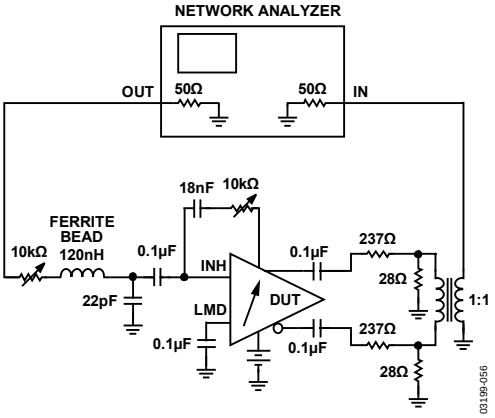


Figure 56. Frequency Response for Various Matched Source Impedances

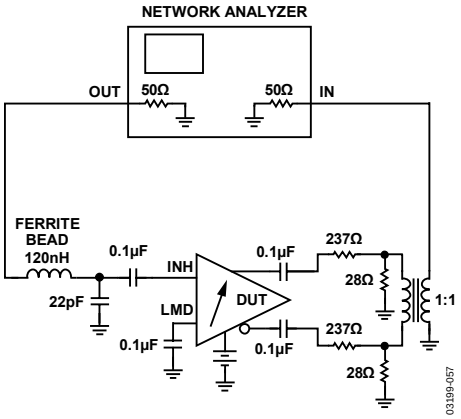


Figure 57. Frequency Response for Unterminated LNA, R_S = 50 Ω

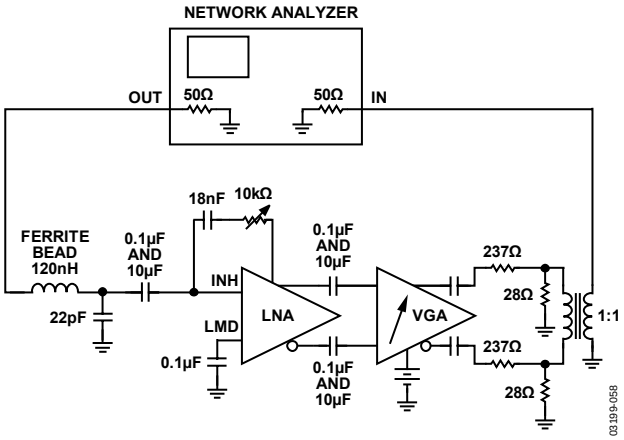


Figure 58. Group Delay vs. Frequency for Two Values of AC Coupling

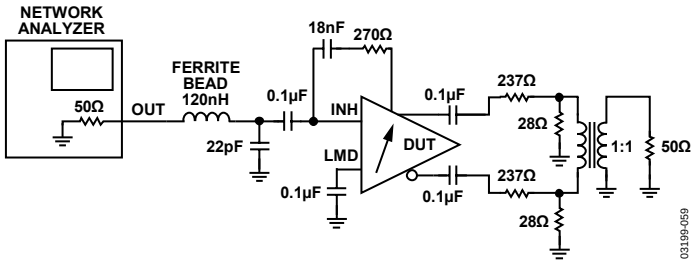


Figure 59. LNA Input Impedance vs. Frequency in Standard and Smith Chart (S11) Formats

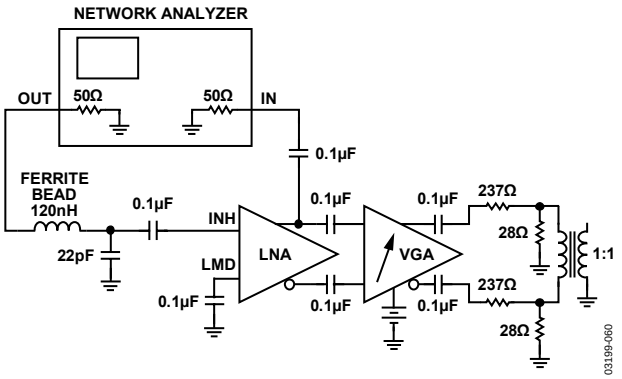


Figure 60. Frequency Response for Unterminated LNA, Single Ended

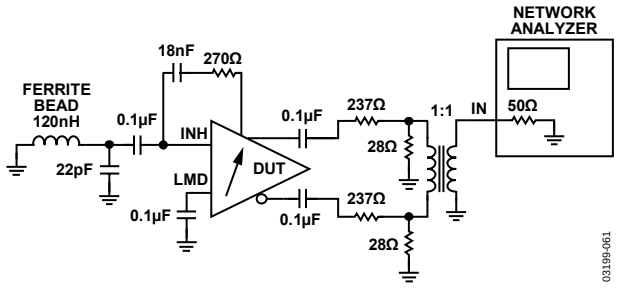


Figure 61. Short-Circuit, Input-Referred Noise

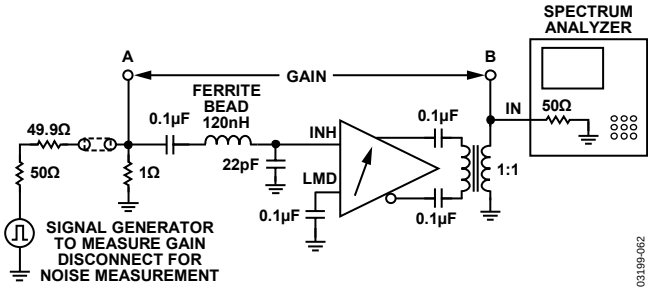


Figure 62. Noise Figure

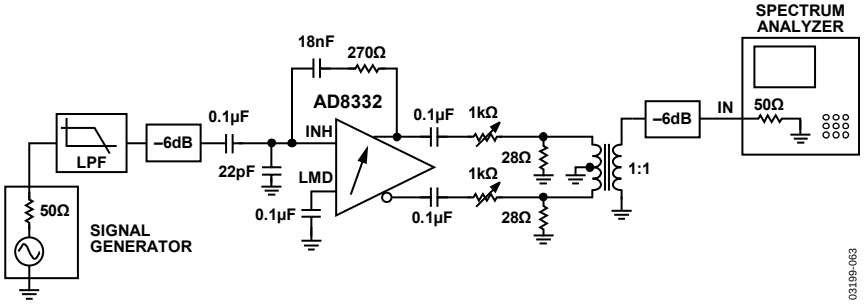


Figure 63. Harmonic Distortion vs. Load Resistance

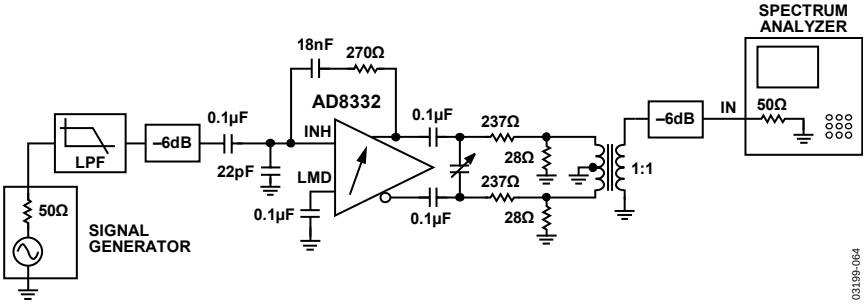


Figure 64. Harmonic Distortion vs. Load Capacitance

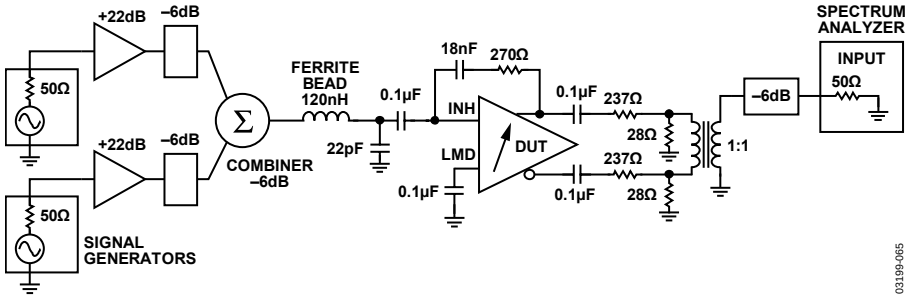


Figure 65. IMD3 vs. Frequency

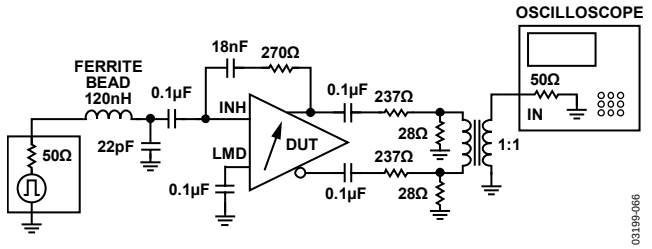


Figure 66. Pulse Response Measurements

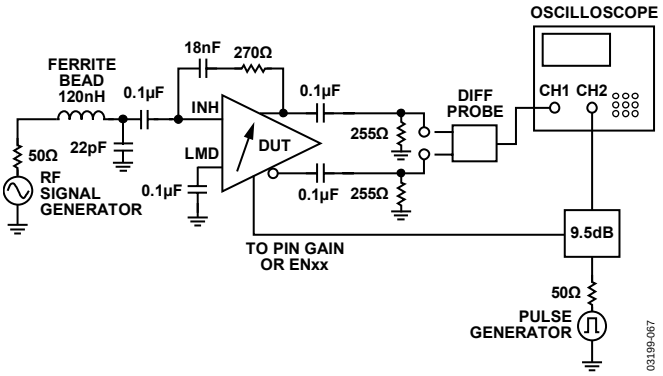


Figure 67. GAIN and Enable Transient Response

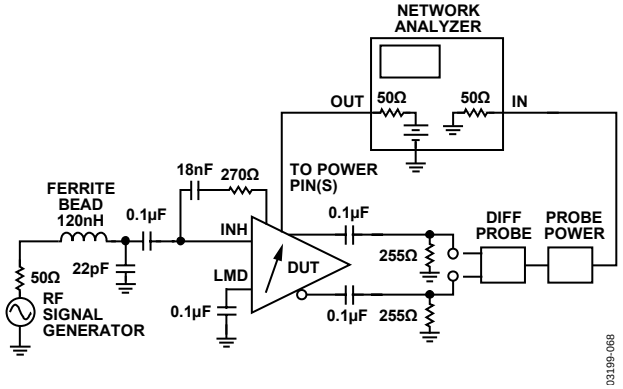


Figure 68. PSRR vs. Frequency

THEORY OF OPERATION

OVERVIEW

The following discussion applies to all part numbers. Figure 69, Figure 70, and Figure 71 are functional block diagrams of the AD8331, AD8332, and AD8334, respectively.

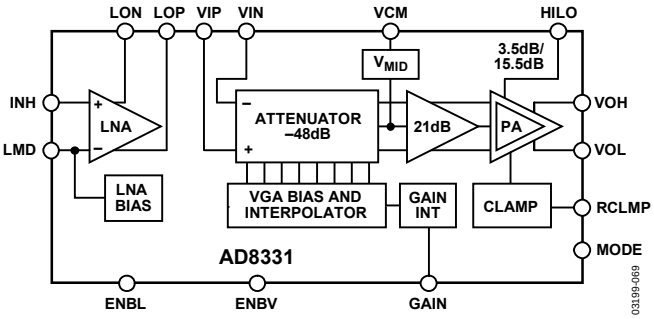


Figure 69. AD8331 Functional Block Diagram

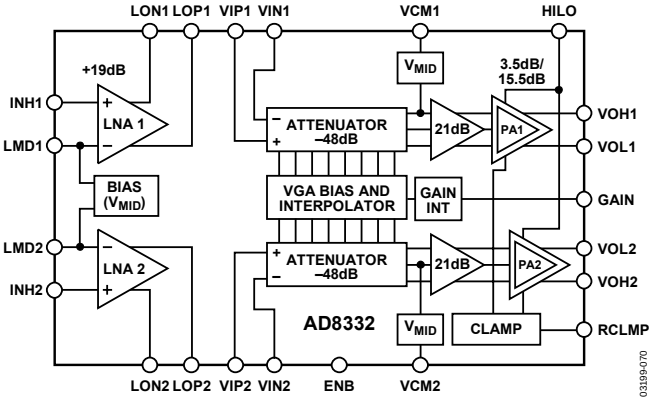


Figure 70. AD8332 Functional Block Diagram

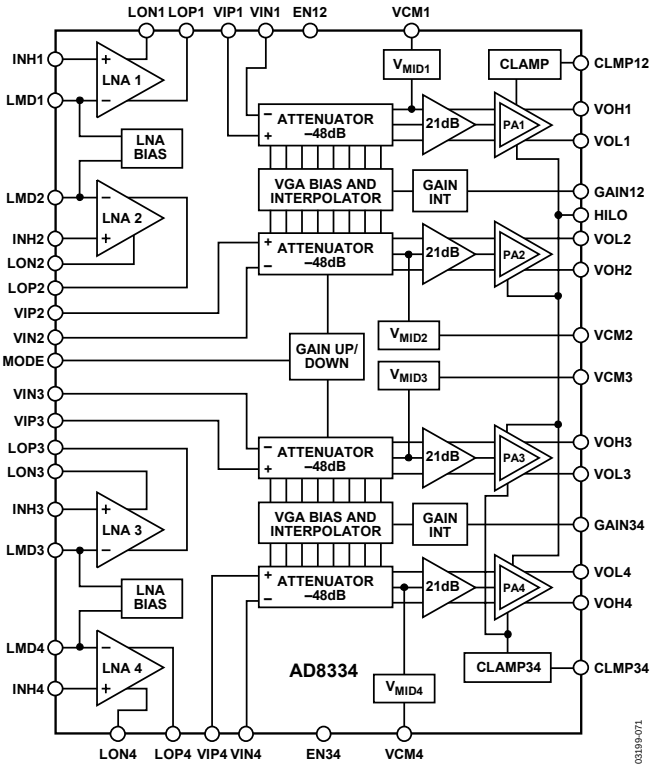


Figure 71. AD8334 Functional Block Diagram

Each channel contains an LNA that provides user-adjustable input impedance termination, a differential X-AMP VGA, and a programmable gain postamplifier with adjustable output voltage limiting. Figure 72 shows a simplified block diagram with external components.

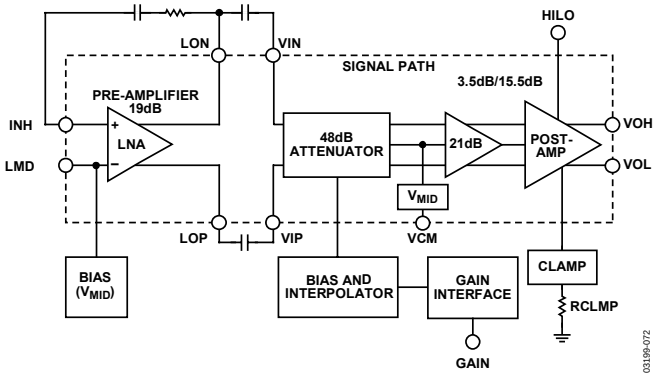


Figure 72. Simplified Block Diagram

The linear-in-dB gain-control interface is trimmed for slope and absolute accuracy. The gain range is 48 dB, extending from −4.5 dB to +43.5 dB in HI gain and +7.5 dB to +55.5 dB in LO gain mode. The slope of the gain control interface is 50 dB/V, and the gain control range is 40 mV to 1 V. Equation 1 and Equation 2 are the expressions for gain.

$$GAIN\ (\text{dB}) = 50\ (\text{dB/V}) \times V_{GAIN} - 6.5\ \text{dB},\ (HILO = LO) \quad (1)$$

or

$$GAIN\ (\text{dB}) = 50\ (\text{dB/V}) \times V_{GAIN} + 5.5\ \text{dB},\ (HILO = LO) \quad (2)$$

The ideal gain characteristics are shown in Figure 73.

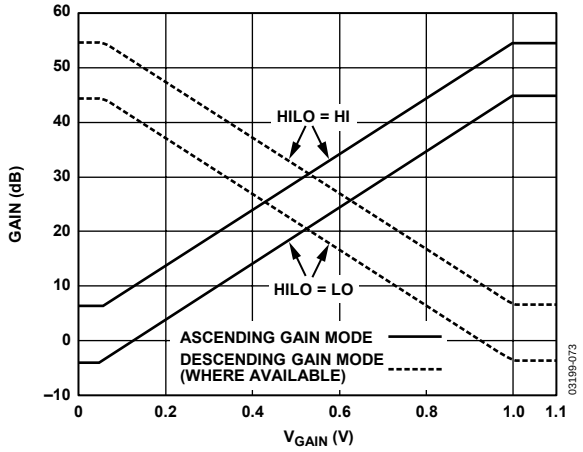


Figure 73. Ideal Gain Control Characteristics

The gain slope is negative with the MODE pulled high (where available):

$$GAIN\ (\text{dB}) = -50\ (\text{dB/V}) \times V_{GAIN} + 45.5\ \text{dB},\ (HILO = LO) \quad (3)$$

or

$$GAIN\ (\text{dB}) = -50\ (\text{dB/V}) \times V_{GAIN} + 57.5\ \text{dB},\ (HILO = HI) \quad (4)$$

The LNA converts a single-ended input to a differential output with a voltage gain of 19 dB. If only one output is used, the gain is 13 dB. The inverting output is used for active input impedance termination. Each of the LNA outputs is capacitively coupled to a VGA input. The VGA consists of an attenuator with a range of 48 dB followed by an amplifier with 21 dB of gain for a net gain range of −27 dB to +21 dB. The X-AMP gain-interpolation technique results in low gain error and uniform bandwidth, and differential signal paths minimize distortion.

The final stage is a logic programmable amplifier with gains of 3.5 dB or 15.5 dB. The LO and HI gain modes are optimized for 12-bit and 10-bit ADC applications, in terms of output-referred noise and absolute gain range. Output voltage limiting can be programmed by the user.

LOW NOISE AMPLIFIER (LNA)

Good noise performance relies on a proprietary ultralow noise preamplifier at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input matching.

A simplified schematic of the LNA is shown in Figure 74. INH is capacitively coupled to the source. An on-chip bias generator establishes dc input bias voltages of 3.25 V and centers the output common-mode levels at 2.5 V. A Capacitor C_{LMD} of the same value as the Input Coupling Capacitor C_{INH} is connected from the LMD pin to ground.

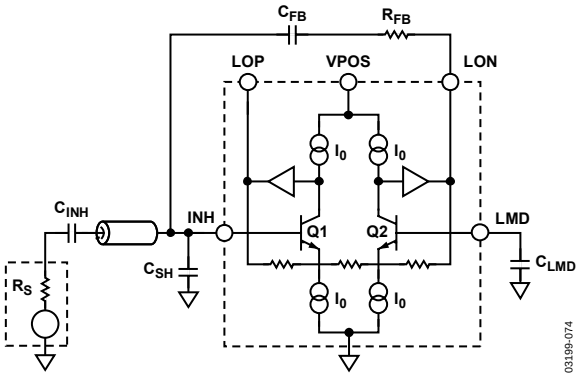


Figure 74. Simplified LNA Schematic

The LNA supports differential output voltages as high as 5 V p-p with positive and negative excursions of ±1.25 V, about a common-mode voltage of 2.5 V. Because the differential gain magnitude is 9, the maximum input signal before saturation is ±275 mV or +550 mV p-p. Overload protection ensures quick recovery time from large input voltages. Because the inputs are capacitively coupled to a bias voltage near midsupply, very large inputs can be handled without interacting with the ESD protection.

Low value feedback resistors and the current-driving capability of the output stage allow the LNA to achieve a low input-referred voltage noise of 0.74 nV/√Hz. This is achieved with a current consumption of only 11 mA per channel (55 mW). On-chip resistor matching results in precise single-ended gains of 4.5× (9× differential), critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low HD2 is particularly important in second harmonic ultrasound imaging applications. Differential signaling enables smaller swings at each output, further reducing third-order distortion.

Active Impedance Matching

The LNA supports active impedance matching through an external shunt feedback resistor from Pin LON to Pin INH. The input resistance, R_{IN}, is given by Equation 5, where A is the single-ended gain of 4.5, and 6 kΩ is the unterminated input impedance.

$$R_{IN} = \frac{R_{FB}}{1+A} \left\| 6\ \text{k}\Omega = \frac{6\ \text{k}\Omega \times R_{FB}}{33\ \text{k}\Omega + R_{FB}} \right. \quad (5)$$

C_{FB} is needed in series with R_{FB} because the dc levels at Pin LON and Pin INH are unequal. Expressions for choosing R_{FB} in terms of R_{IN} and for choosing C_{FB} are found in the Applications section. C_{SH} and the ferrite bead enhance stability at higher frequencies where the loop gain is diminished and prevent peaking. Frequency response plots of the LNA are shown in Figure 23 and Figure 24. The bandwidth is approximately 130 MHz for matched input impedances of 50 Ω to 200 Ω and declines at higher source impedances. The unterminated bandwidth (when $R_{FB} = \infty$) is approximately 80 MHz.

Each output can drive external loads as low as 100 Ω in addition to the 100 Ω input impedance of the VGA (200 Ω differential). Capacitive loading up to 10 pF is permissible. All loads should be ac-coupled. Typically, Pin LOP output is used as a single-ended driver for auxiliary circuits, such as those used for Doppler ultrasound imaging, and Pin LON drives R_{FB}. Alternatively, a differential external circuit can be driven from the two outputs in addition to the active feedback termination. In both cases, important stability considerations discussed in the Applications section should be carefully observed.

The impedance at each LNA output is 5 Ω. A 0.4 dB reduction in open-circuit gain results when driving the VGA, and 0.8 dB with an additional 100 Ω load at the output. The differential gain of the LNA is 6 dB higher. If the load is less than 200 Ω on either side, a compensating load is recommended on the opposite output.

LNA Noise

The input-referred voltage noise sets an important limit on system performance. The short-circuit input voltage noise of the LNA is 0.74 nV/√Hz or 0.82 nV/√Hz (at maximum gain), including the VGA noise. The open-circuit current noise is 2.5 pA/√Hz. These measurements, taken without a feedback resistor, provide the basis for calculating the input noise and noise figure performance of the configurations in Figure 75. Figure 76 and Figure 77 are simulations extracted from these results, and the 4.1 dB NF measurement with the input actively matched to a 50 Ω source. Unterminated ($R_{FB} = \infty$) operation exhibits the lowest equivalent input noise and noise figure. Figure 76 shows the noise figure vs. source resistance, rising at low R_S, where the LNA voltage noise is large compared to the source noise, and again at high R_S due to current noise. The VGA's input-referred voltage noise of 2.7 nV/√Hz is included in all of the curves.

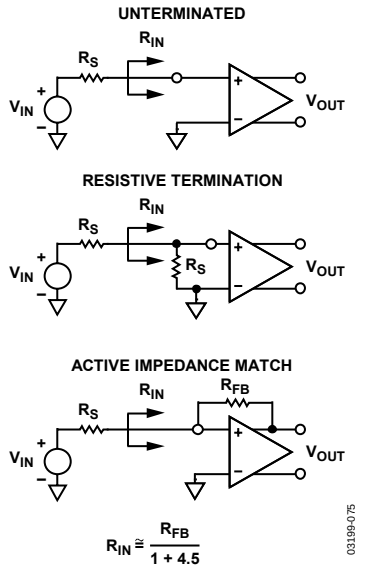


Figure 75. Input Configurations

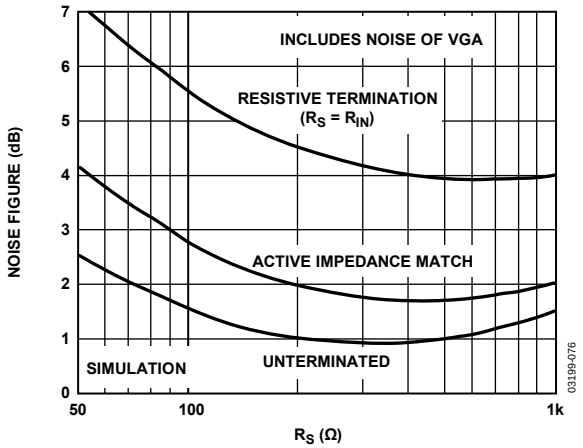


Figure 76. Noise Figure vs. R_S for Resistive, Active Matched and Unterminated Inputs

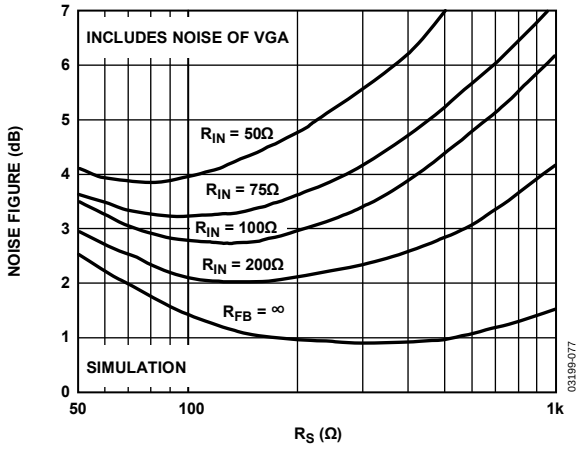


Figure 77. Noise Figure vs. R_S for Various Fixed Values of R_{IN}, Actively Matched

The primary purpose of input impedance matching is to improve the system transient response. With resistive termination, the input noise increases due to the thermal noise of the matching resistor and the increased contribution of the LNA's input voltage noise generator. With active impedance matching, however, the contributions of both are smaller than they would be for resistive termination by a factor of 1/(1 + *LNA Gain*). Figure 76 shows their relative noise figure (NF) performance. In this graph, the input impedance was swept with R_S to preserve the match at each point. The noise figures for a source impedance of 50 Ω are 7.1 dB, 4.1 dB, and 2.5 dB, respectively, for the resistive, active, and unterminated configurations. The noise figures for 200 Ω are 4.6 dB, 2.0 dB, and 1.0 dB, respectively.

Figure 77 is a plot of the NF vs. R_S for various values of R_{IN}, which is helpful for design purposes. The plateau in the NF for actively matched inputs mitigates source impedance variations. For comparison purposes, a preamp with a gain of 19 dB and noise spectral density of 1.0 nV/√Hz, combined with a VGA with 3.75 nV/√Hz, yields a noise figure degradation of approximately 1.5 dB (for most input impedances), significantly worse than the AD8332 performance.

The equivalent input noise of the LNA is the same for single-ended and differential output applications. The LNA noise figure improves to 3.5 dB at 50 Ω without VGA noise, but this is exclusive of noise contributions from other external circuits connected to LOP. A series output resistor is usually recommended for stability purposes when driving external circuits on a separate board (see the Applications section). In low noise applications, a ferrite bead is even more desirable.

VARIABLE GAIN AMPLIFIER

The differential X-AMP VGA provides precise input attenuation and interpolation. It has a low input-referred noise of 2.7 nV/√Hz and excellent gain linearity. A simplified block diagram is shown in Figure 78.

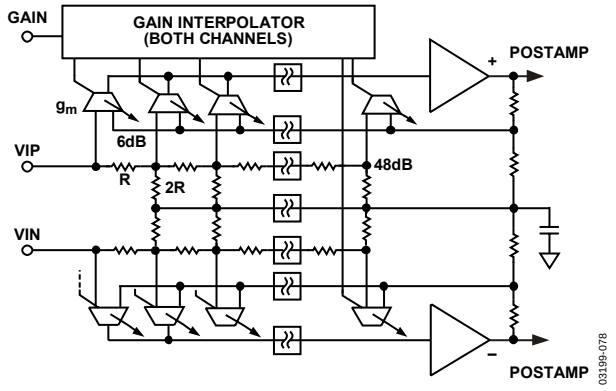


Figure 78. Simplified VGA Schematic

X-AMP VGA

The input of the VGA is a differential R-2R ladder attenuator network with 6 dB steps per stage and a net input impedance of 200 Ω differential. The ladder is driven by a fully differential input signal from the LNA and is not intended for single-ended operation. LNA outputs are ac-coupled to reduce offset and isolate their common-mode voltage. The VGA inputs are biased through the ladder's center tap connection to VCM, which is typically set to 2.5 V and is bypassed externally to provide a clean ac ground.

The signal level at successive stages in the input attenuator falls from 0 dB to −48 dB in 6 dB steps. The input stages of the X-AMP are distributed along the ladder, and a biasing interpolator, controlled by the gain interface, determines the input tap point. With overlapping bias currents, signals from successive taps merge to provide a smooth attenuation range from 0 dB to −48 dB. This circuit technique results in excellent, linear-in-dB gain law conformance and low distortion levels and deviates ±0.2 dB or less from the ideal. The gain slope is monotonic with respect to the control voltage and is stable with variations in process, temperature, and supply.

The X-AMP inputs are part of a gain-of-12 feedback amplifier that completes the VGA. Its bandwidth is 150 MHz. The input stage is designed to reduce feedthrough to the output and to ensure excellent frequency response uniformity across gain setting (see Figure 12 and Figure 13).

Gain Control

Position along the VGA attenuator is controlled by a single-ended analog control voltage, V_{GAIN}, with an input range of 40 mV to 1.0 V. The gain control scaling is trimmed to a slope of 50 dB/V (20 mV/dB). Values of V_{GAIN} beyond the control range saturate to minimum or maximum gain values. Both channels of the AD8332 are controlled from a single gain interface to preserve matching. Gain can be calculated using Equation 1 and Equation 2.

Gain accuracy is very good because both the scaling factor and absolute gain are factory trimmed. The overall accuracy relative to the theoretical gain expression is ±1 dB for variations in temperature, process, supply voltage, interpolator gain ripple, trim errors, and tester limits. The gain error relative to a best-fit line for a given set of conditions is typically ±0.2 dB. Gain matching between channels is better than 0.1 dB (Figure 11 shows gain errors in the center of the control range). When V_{GAIN} < 0.1 or > 0.95, gain errors are slightly greater.

The gain slope can be inverted, as shown in Figure 73 (available in most versions). The gain drops with a slope of −50 dB/V across the gain control range from maximum to minimum gain. This slope is useful in applications, such as automatic gain control, where the control voltage is proportional to the measured output signal amplitude. The inverse gain mode is selected by setting the MODE pin HI.

Gain control response time is less than 750 ns to settle within 10% of the final value for a change from minimum to maximum gain.

VGA Noise

In a typical application, a VGA compresses a wide dynamic range input signal to within the input span of an ADC. While the input-referred noise of the LNA limits the minimum resolvable input signal, the output-referred noise, which depends primarily on the VGA, limits the maximum instantaneous dynamic range that can be processed at any one particular gain control voltage. This limit is set in accordance with the quantization noise floor of the ADC.

Output and input-referred noise as a function of V_{GAIN} are plotted in Figure 25 and Figure 27 for the short-circuited input conditions. The input noise voltage is simply equal to the output noise divided by the measured gain at each point in the control range.

The output-referred noise is flat over most of the gain range, because it is dominated by the fixed output-referred noise of the VGA. Values are 48 nV/√Hz in LO gain mode and 178 nV/√Hz in HI gain mode. At the high end of the gain control range, the noise of the LNA and source prevail. The input-referred noise reaches its minimum value near the maximum gain control voltage, where the input-referred contribution of the VGA becomes very small.

At lower gains, the input-referred noise, and thus noise figure, increases as the gain decreases. The instantaneous dynamic range of the system is not lost, however, because the input capacity increases with it. The contribution of the ADC noise floor has the same dependence as well. The important relationship is the magnitude of the VGA output noise floor relative to that of the ADC.

With its low output-referred noise levels, these devices ideally drive low voltage ADCs. The converter noise floor drops 12 dB for every 2 bits of resolution and drops at lower input full-scale voltages and higher sampling rates. ADC quantization noise is discussed in the Applications section.

The preceding noise performance discussion applies to a differential VGA output signal. Although the LNA noise performance is the same in single-ended and differential applications, the VGA performance is not. The noise of the VGA is significantly higher in single-ended usage, because the contribution of its bias noise is designed to cancel in the differential signal. A transformer can be used with single-ended applications when low noise is desired.

Gain control noise is a concern in very low noise applications. Thermal noise in the gain control interface can modulate the channel gain. The resultant noise is proportional to the output signal level and usually only evident when a large signal is present. Its effect is observable only in LO gain mode, where the noise floor is substantially lower. The gain interface includes an on-chip noise filter, which reduces this effect significantly at frequencies above 5 MHz. Care should be taken to minimize noise impinging at the GAIN input. An external RC filter can be used to remove V_{GAIN} source noise. The filter bandwidth should be sufficient to accommodate the desired control bandwidth.

Common-Mode Biasing

An internal bias network connected to a midsupply voltage establishes common-mode voltages in the VGA and postamp. An externally bypassed buffer maintains the voltage. The bypass capacitors form an important ac ground connection, because the VCM network makes a number of important connections internally, including the center tap of the VGA's differential input attenuator, the feedback network of the VGA's fixed gain amplifier, and the feedback network of the postamplifier in both gain settings. For best results, use a 1 nF and a 0.1 µF capacitor in parallel, with the 1 nF nearest to the VCM pin. Separate VCM pins are provided for each channel. For dc-coupling to a 3 V ADC, the output common-mode voltage is adjusted to 1.5 V by biasing the VCM pin.

POSTAMPLIFIER

The final stage has a selectable gain of 3.5 dB (×1.5) or 15.5 dB (×6), set by the logic pin, HILO. Figure 79 is a simplified block diagram.

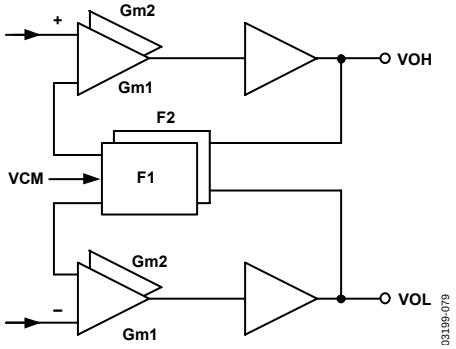


Figure 79. Postamplifier Block Diagram

Separate feedback attenuators implement the two gain settings. These are selected in conjunction with an appropriately scaled input stage to maintain a constant 3 dB bandwidth between the two gain modes (~150 MHz). The slew rate is 1200 V/µs in HI gain mode and 300 V/µs in LO gain mode. The feedback networks for HI and LO gain modes are factory trimmed to adjust the absolute gains of each channel.

Noise

The topology of the postamplifier provides constant input-referred noise with the two gain settings and variable output-referred noise. The output-referred noise in HI gain mode increases (with gain) by four. This setting is recommended when driving converters with higher noise floors. The extra gain boosts the output signal levels and noise floor appropriately. When driving circuits with lower input noise floors, the LO gain mode optimizes the output dynamic range.

Although the quantization noise floor of an ADC depends on a number of factors, the 48 nV/√Hz and 178 nV/√Hz levels are well suited to the average requirements of most 12-bit and 10-bit converters, respectively. An additional technique, described in the Applications section, can extend the noise floor even lower for possible use with 14-bit ADCs.

Output Clamping

Outputs are internally limited to a level of 4.5 V p-p differential when operating at a 2.5 V common-mode voltage. The postamp implements an optional output clamp engaged through a resistor from R_{CLMP} to ground. Table 8 shows a list of recommended resistor values.

Output clamping can be used for ADC input overload protection, if needed, or postamp overload protection when operating from a lower common-mode level, such as 1.5 V. The user should be aware that distortion products increase as output levels approach the clamping levels, and the user should adjust the clamp resistor accordingly. For additional information, see the Applications section.

The accuracy of the clamping levels is approximately ±5% in LO or HI mode. Figure 80 illustrates the output characteristics for a few values of R_{CLMP}.

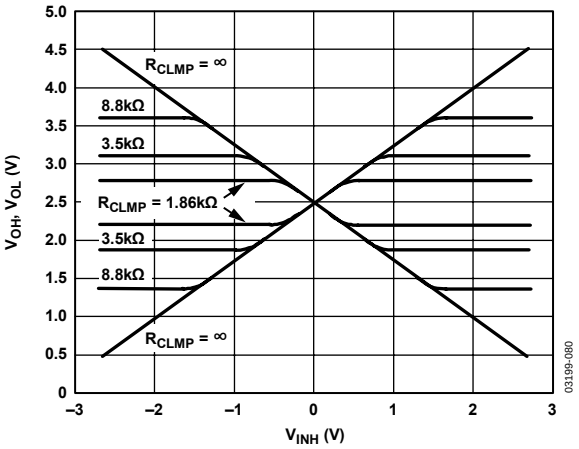


Figure 80. Output Clamping Characteristics

APPLICATIONS

LNA—EXTERNAL COMPONENTS

The LMD pin (connected to the bias circuitry) must be bypassed to ground and signal sourced to the INH pin capacitively coupled using 2.2 nF to 0.1 µF capacitors (see Figure 81).

The unterminated input impedance of the LNA is 6 kΩ. The user can synthesize any LNA input resistance between 50 Ω and 6 kΩ. R_{FB} is calculated according to Equation 6 or selected from Table 7.

$$R_{FB} = \frac{33\ \text{k}\Omega \times (R_{IN})}{6\ \text{k}\Omega - (R_{IN})} \quad (6)$$

Table 7. LNA External Component Values for Common Source Impedances

R_{IN} (Ω)	R_{FB} (Nearest STD 1% Value, Ω)	C_{SH} (pF)
50	280	22
75	412	12
100	562	8
200	1.13 k	1.2
500	3.01 k	None
6 k	∞	None

When active input termination is used, a decoupling capacitor (C_{FB}) is required to isolate the input and output bias voltages of the LNA.

The shunt input capacitor, C_{SH}, reduces gain peaking at higher frequencies where the active termination match is lost due to the gain roll-off of the LNA at high frequencies. The value of C_{SH} diminishes as R_{IN} increases to 500 Ω, at which point no capacitor is required. Suggested values for C_{SH} for 50 Ω ≤ R_{IN} ≤ 200 Ω are shown in Table 7.

When a long trace to Pin INH is unavoidable, or if both LNA outputs drive external circuits, a small ferrite bead (FB) in series with Pin INH preserves circuit stability with negligible effect on noise. The bead shown is 75 Ω at 100 MHz (Murata BLM21 or equivalent). Other values can prove useful.

Figure 82 shows the interconnection details of the LNA output. Capacitive coupling between the LNA outputs and the VGA inputs is required because of the differences in their dc levels and the need to eliminate the offset of the LNA. Capacitor values of 0.1 µF are recommended. There is 0.4 dB loss in gain between the LNA output and the VGA input due to the 5 Ω output resistance. Additional loading at the LOP and LON outputs affect LNA gain.

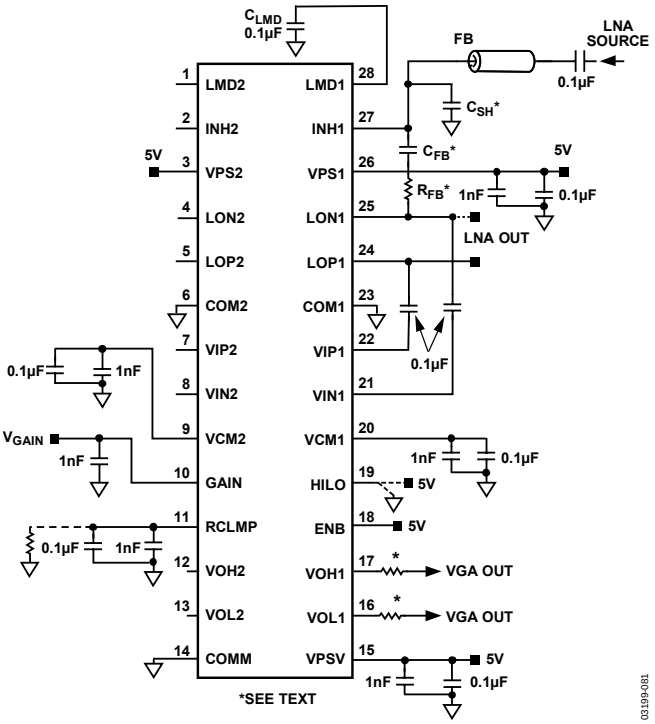


Figure 81. Basic Connections for a Typical Channel (AD8332 Shown)

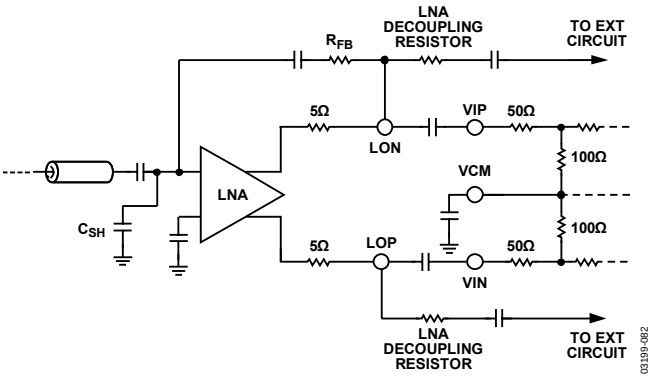


Figure 82. Interconnections of the LNA and VGA

Both LNA outputs are available for driving external circuits. Pin LOP should be used in those instances when a single-ended LNA output is required. The user should be aware of stray capacitance loading of the LNA outputs, in particular LON. The LNA can drive 100 Ω in parallel with 10 pF. If an LNA output is routed to a remote PC board, it tolerates a load capacitance up to 100 pF with the addition of a 49.9 Ω series resistor or ferrite 75 Ω/100 MHz bead.

Gain Input

The GAIN pin is common to both channels of the AD8332. The input impedance is nominally 10 MΩ and a bypass capacitor from 100 pF to1 nF is recommended.

Parallel connected devices can be driven by a common voltage source or DAC. Decoupling should take into account any bandwidth considerations of the drive waveform, using the total distributed capacitance.

If gain control noise in LO gain mode becomes a factor, maintaining ≤15 nV/√Hz noise at the GAIN pin ensures satisfactory noise performance. Internal noise prevails below 15 nV/√Hz at the GAIN pin. Gain control noise is negligible in HI gain mode.

VCM Input

The common-mode voltage of Pin VCM, Pin VOL, and Pin VOH defaults to 2.5 V dc. With output ac-coupled applications, the VCM pin is unterminated; however, it must still be bypassed in close proximity for ac grounding of internal circuitry. The VGA outputs can be dc connected to a differential load, such as an ADC. Common-mode output voltage levels between 1.5 V and 3.5 V can be realized at Pin VOH and Pin VOL by applying the desired voltage at Pin VCM. DC-coupled operation is not recommended when driving loads on a separate PC board.

The voltage on the VCM pin is sourced by an internal buffer with an output impedance of 30 Ω and a ±2 mA default output current (see Figure 83). If the VCM pin is driven from an external source, its output impedance should be <<30 Ω and its current drive capability should be >>2 mA. If the VCM pins of several devices are connected in parallel, the external buffer should be capable of overcoming their collective output currents. When a common-mode voltage other than 2.5 V is used, a voltage-limiting resistor, R_{CLMP}, is needed to protect against overload.

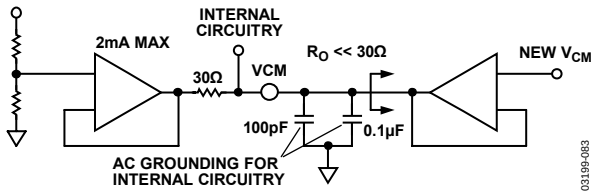


Figure 83. VCM Interface

Logic Inputs—ENB, MODE, and HILO

The input impedance of all enable pins is nominally 25 kΩ and can be pulled up to 5 V (a pull-up resistor is recommended) or driven by any 3 V or 5 V logic families. The enable pin, ENB, powers down the VGA—when pulled low, the VGA output voltages are near ground. Multiple devices can be driven from a common source. Consult Table 3, Table 4, Table 5, and Table 6 for circuit functions controlled by the enable pins.

Pin HILO is compatible with 3 V or 5 V CMOS logic families. It is either connected to ground or pulled up to 5 V, depending on the desired gain range and output noise.

Optional Output Voltage Limiting

The RCLMP pin provides the user with a means to limit the output voltage swing when used with loads that have no provisions for prevention of input overdrive. The peak-to-peak limited voltage is adjusted by a resistor to ground, and Table 8 lists several voltage levels and the corresponding resistor value. Unconnected, the default limiting level is 4.5 V p-p.

Note that third harmonic distortion increases as waveform amplitudes approach clipping. For lowest distortion, the clamp level should be set higher than the converter input span. A clamp level of 1.5 V p-p is recommended for a 1 V p-p linear output range, 2.7 V p-p for a 2 V p-p range, or 1 V p-p for a 0.5 V p-p operation. The best solution is determined experimentally. Figure 84 shows third harmonic distortion as a function of the limiting level for a 2 V p-p output signal. A wider limiting level is desirable in HI gain mode.

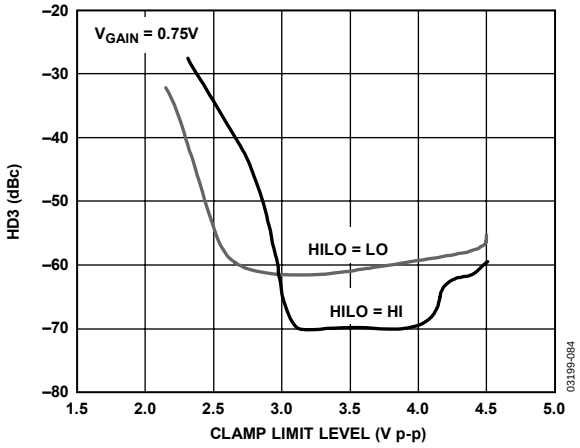


Figure 84. HD3 vs. Clamping Level for 2 V p-p Differential Input

Table 8. Clamp Resistor Values

	Clamp Resistor Value (kΩ)	
Clamp Level (V p-p)	**HILO = LO**	**HILO = HI**
0.5	1.21	
1.0	2.74	2.21
1.5	4.75	4.02
2.0	7.5	6.49
2.5	11	9.53
3.0	16.9	14.7
3.5	26.7	23.2
4.0	49.9	39.2
4.4	100	73.2

Output Decoupling

When driving capacitive loads greater than about 10 pF, or long circuit connections on other boards, an output network of resistors and/or ferrite beads can be useful to ensure stability. These components can be incorporated into a Nyquist filter such as the one shown in Figure 81. In Figure 81, the resistor value is 84.5 Ω. The AD8332-EVAL incorporates 100 Ω in parallel with a 120 nH bead. Lower value resistors are permissible for applications with nearby loads or with gains less than 40 dB. The exact values of these components can be selected empirically.

An antialiasing noise filter is typically used with an ADC. Filter requirements are application dependent.

When the ADC resides on a separate board, the majority of filter components should be placed nearby to suppress noise picked up between boards and to mitigate charge kickback from the ADC inputs. Any series resistance beyond that required for output stability should be placed on the ADC board. Figure 85 shows a second-order, low-pass filter with a bandwidth of 20 MHz. The capacitor is chosen in conjunction with the 10 pF input capacitance of the ADC.

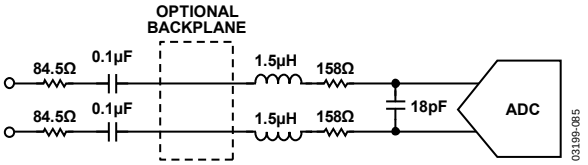


Figure 85. 20 MHz Second-Order, Low-Pass Filter

DRIVING ADCs

The output drive accommodates a wide range of ADCs. The noise floor requirements of the VGA depend on a number of application factors, including bit resolution, sampling rate, full-scale voltage, and the bandwidth of the noise/antialias filter. The output noise floor and gain range can be adjusted by selecting HI or LO gain mode.

The relative noise and distortion performance of the two gain modes can be compared in Figure 25 and Figure 31 through Figure 41. The 48 nV/√Hz noise floor of the LO gain mode is suited to converters with higher sampling rates or resolutions (such as 12 bits). Both gain modes can accommodate ADC full-scale voltages as high as 4 V p-p. Because distortion performance remains favorable for output voltages as high as 4 V p-p (see Figure 36), it is possible to lower the output-referred noise even further by using a resistive attenuator (or transformer) at the output. The circuit in Figure 86 has an output full-scale range of 2 V p-p, a gain range of −10.5 dB to +37.5 dB, and an output noise floor of 24 nV/√Hz, making it suitable for some 14-bit ADC applications.

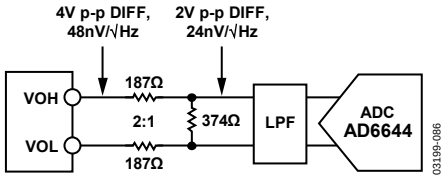


Figure 86. Adjusting the Noise Floor for 14-Bit ADCs

OVERLOAD

These devices respond gracefully to large signals that overload its input stage and to normal signals that overload the VGA when the gain is set unexpectedly high. Each stage is designed for clean-limited overload waveforms and fast recovery when gain setting or input amplitude is reduced.

Signals larger than ±275 mV at the LNA input are clipped to 5 V p-p differential prior to the input of the VGA. Figure 48 shows the response to a 1 V p-p input burst. The symmetric overload waveform is important for applications, such as CW Doppler ultrasound, where the spectrum of the LNA outputs during overload is critical. The input stage is also designed to accommodate signals as high as ±2.5 V without triggering the slow-settling ESD input protection diodes.

Both stages of the VGA are susceptible to overload. Postamp limiting is more common and results in the clean-limited output characteristics found in Figure 49. Recovery is fast in all cases. The graph in Figure 87 summarizes the combinations of input signal and gain that lead to the different types of overload.

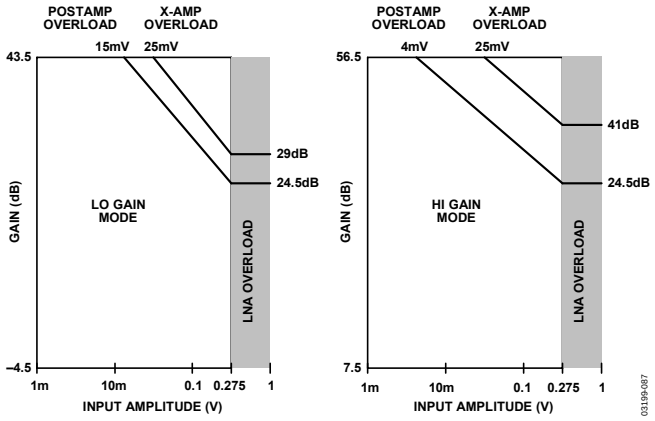


Figure 87. Overload Gain and Signal Conditions

The previously mentioned clamp interface controls the maximum output swing of the postamp and its overload response. When the clamp feature is not used, the output level defaults to approximately 4.5 V p-p differential centered at 2.5 V common mode. When other common-mode levels are set through the VCM pin, the value of R_{CLMP} should be selected for graceful overload. A value of 8.3 kΩ or less is recommended for 1.5 V or 3.5 V common-mode levels (7.2 kΩ for HI gain mode). This limits the output swing to just above 2 V p-p differential.

OPTIONAL INPUT OVERLOAD PROTECTION

Applications in which high transients are applied to the LNA input can benefit from the use of clamp diodes. A pair of back-to-back Schottky diodes can reduce these transients to manageable levels. Figure 88 illustrates how such a diode-protection scheme can be connected.

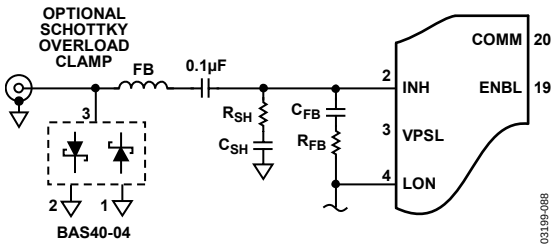


Figure 88. Input Overload Clamping

When selecting overload protection, the important parameters are forward and reverse voltages and t_{rr} (or τ_{rr}). The Infineon BAS40-04 series shown in Figure 88 has a τ_{rr} of 100 ps and V_F of 310 mV at 1 mA. Many variations of these specifications can be found in vendor catalogs.

LAYOUT, GROUNDING, AND BYPASSING

Due to their excellent high frequency characteristics, these devices are sensitive to their PCB environment. Realizing expected performance requires attention to detail critical to good high speed board design.

A multilayer board with power and ground planes is recommended with blank areas in the signal layers filled with ground plane. Be certain that the power and ground pins provided for robust power distribution to the device are connected. Decouple the power supply pins with surface-mount capacitors as close as possible to each pin to minimize impedance paths to ground. Decouple the LNA power pins from the VGA supply using ferrite beads. Together with the capacitors, ferrite beads eliminate undesired high frequencies without reducing the headroom. Use a larger value capacitor for every 10 chips to 20 chips to decouple residual low frequency noise. To minimize voltage drops, use a 5 V regulator for the VGA array.

Several critical LNA areas require special care. The LON and LOP output traces must be as short as possible before connecting to the coupling capacitors connected to Pin VIN and Pin VIP. R_{FB} must be placed near the LON pin as well. Resistors must be placed as close as possible to the VGA output pins, VOL and VOH, to mitigate loading effects of connecting traces. Values are discussed in the Output Decoupling section.

Signal traces must be short and direct to avoid parasitic effects. Wherever there are complementary signals, symmetrical layout should be employed to maintain waveform balance. PCB traces should be kept adjacent when running differential signals over a long distance.

MULTIPLE INPUT MATCHING

Matching of multiple sources with dissimilar impedances can be accomplished as shown in Figure 90. A relay and low supply voltage analog switch can be used to select between multiple sources and their associated feedback resistors. An ADG736 dual SPDT switch is shown in this example; however, multiple switches are also available and users are referred to the Analog Devices Selection Guide for switches and multiplexers.

DISABLING THE LNA

Where accessible, connection of the LNA enable pin to ground powers down the LNA, resulting in a current reduction of about half. In this mode, the LNA input and output pins can be left unconnected; however, the power must be connected to all the supply pins for the disabling circuit to function. Figure 89 illustrates the connections using an AD8331 as an example.

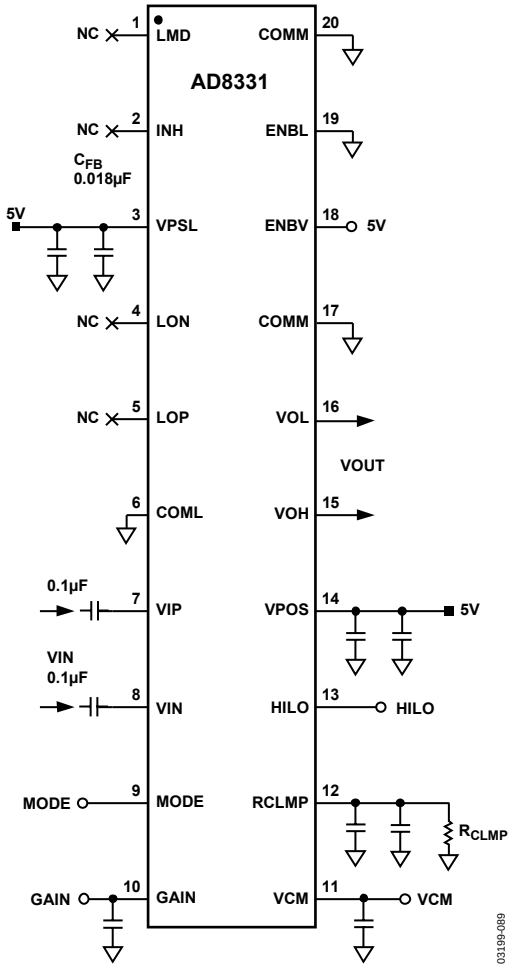


Figure 89. Disabling the LNA

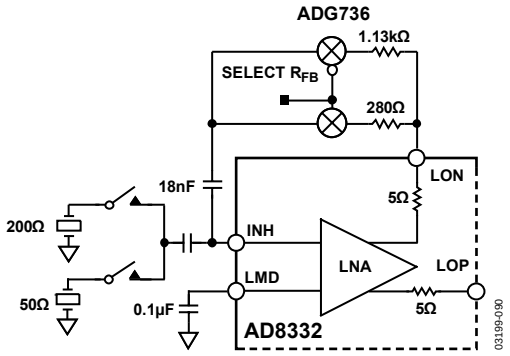


Figure 90. Accommodating Multiple Sources

ULTRASOUND TGC APPLICATION

The AD8332 ideally meets the requirements of medical and industrial ultrasound applications. The TGC amplifier is a key subsystem in such applications, because it provides the means for echolocation of reflected ultrasound energy.

Figure 91 through Figure 93 are schematics of a dual, fully differential system using the AD8332 and the AD9238, 12-bit high speed ADC with conversion speeds as high as 65 MSPS.

Using the EVAL-AD8332/AD9238 evaluation board and a high speed ADC FIFO evaluation kit connected to a laptop, an FFT can be performed on the AD8332. With the on-board clock of 20 MHz, minimal low-pass filtering, and both channels driven with a 1 MHz filtered sine wave, the THD is −75 dB, noise floor is −93 dB, and HD2 is −83 dB.

HIGH DENSITY QUAD LAYOUT

The AD8334 is the ideal solution for applications with limited board space. Figure 94 represents four channels routed to and away from this very compact quad VGA. Note that none of the signal paths crosses and that all four channels are spaced apart to eliminate crosstalk.

In this example, all of the components shown are 0402 size; however, the same layout is executable at the expense of slightly more board area. The sketch also assumes that both sides of the printed circuit board are available for components, and that the bypass and power supply decoupling circuitry is located on the wiring side of the board.

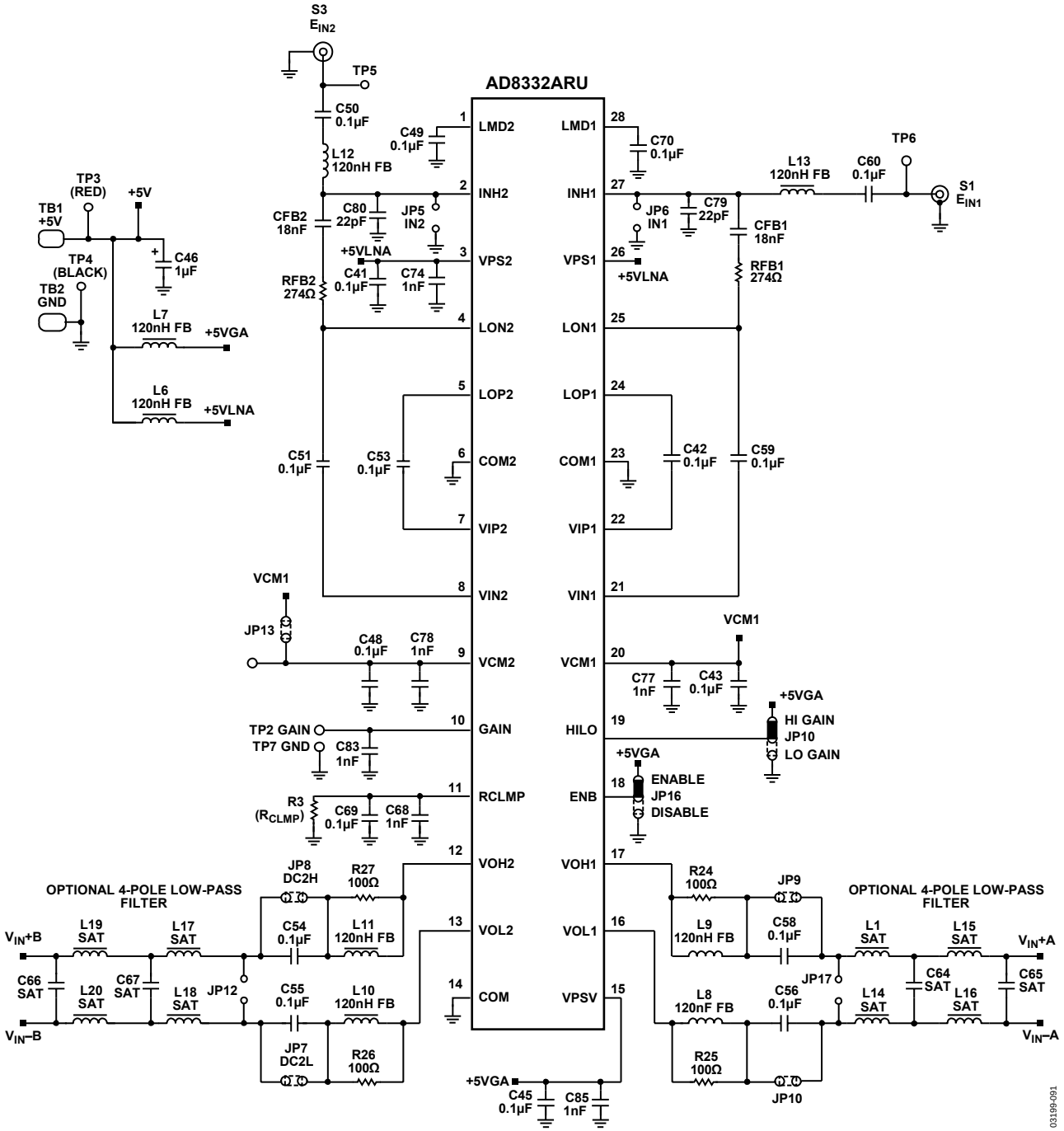


Figure 91. Schematic, TGC, VGA Section Using an AD8332 and AD9238

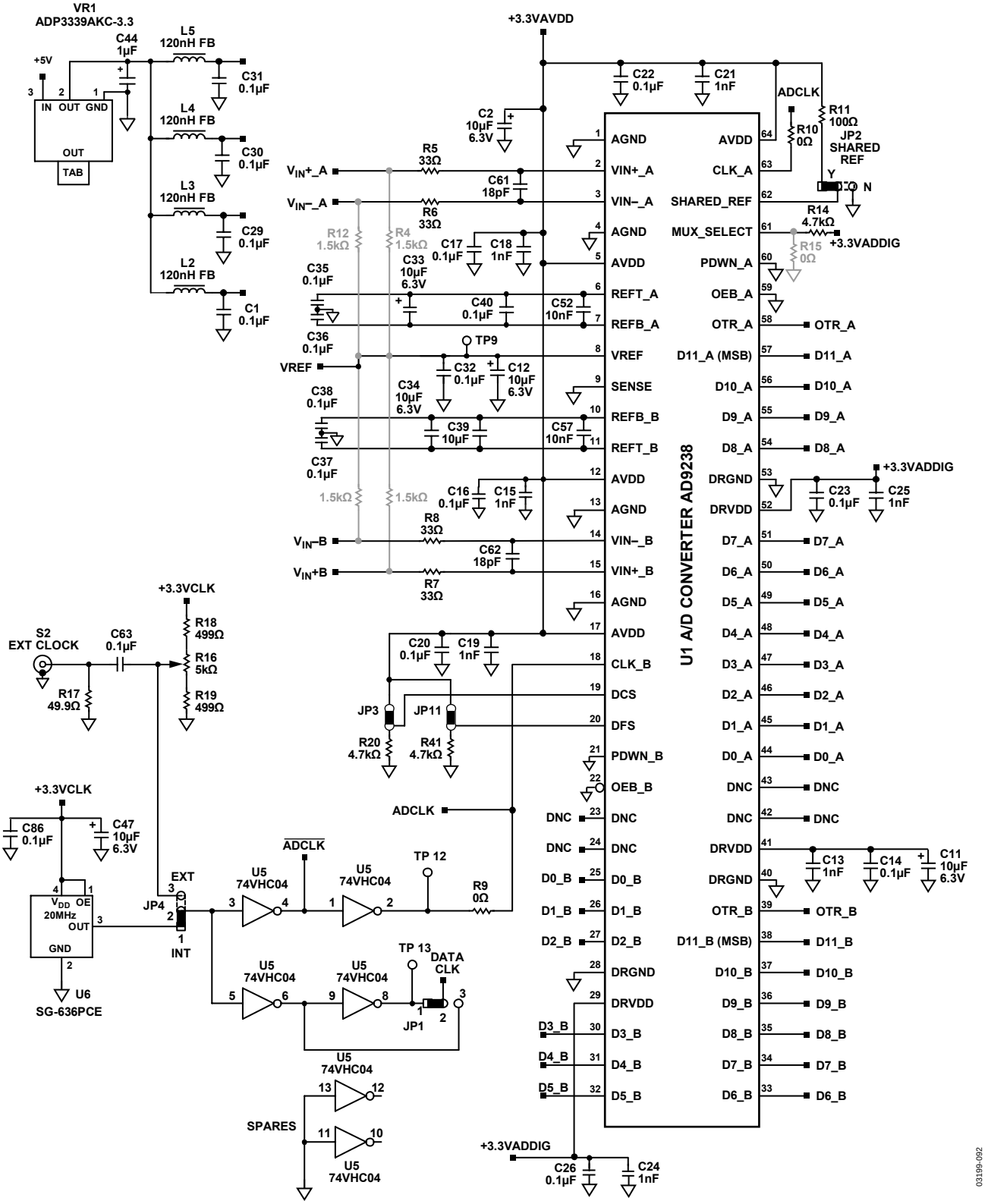


Figure 92. Converter Schematic, TGC Using an AD8332 and AD9238

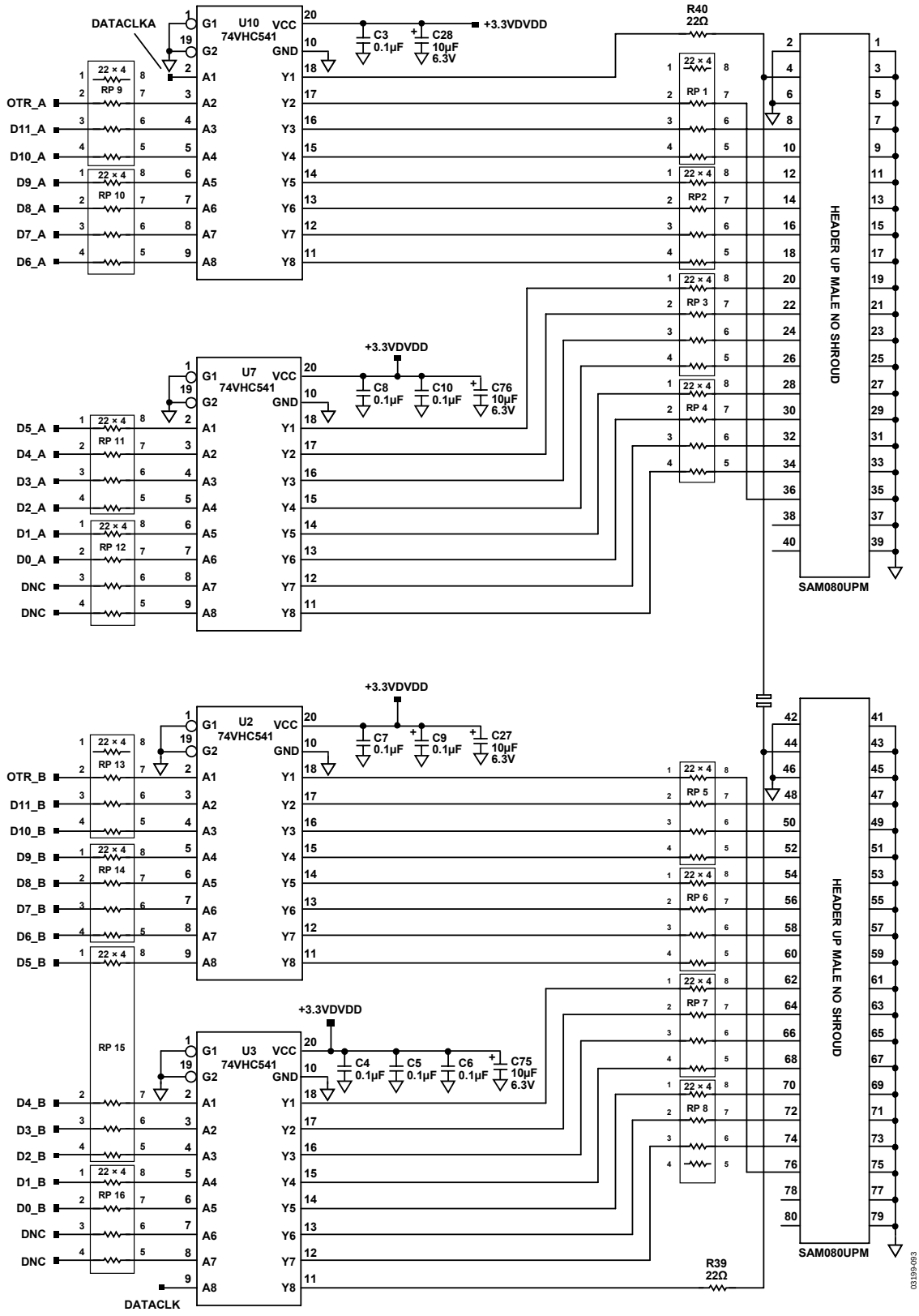


Figure 93. Interface Schematic, TGC Using an AD8332 and AD9238

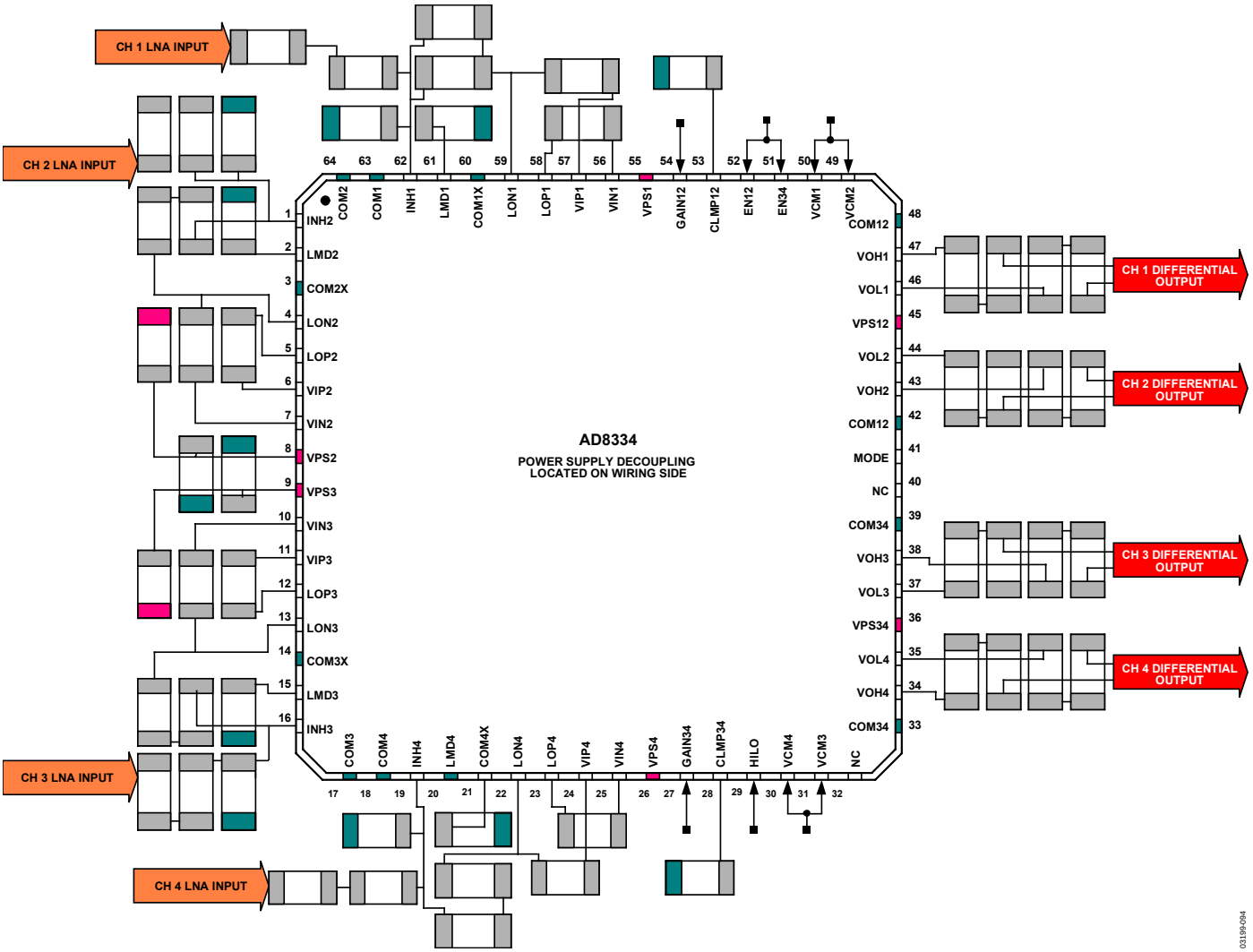
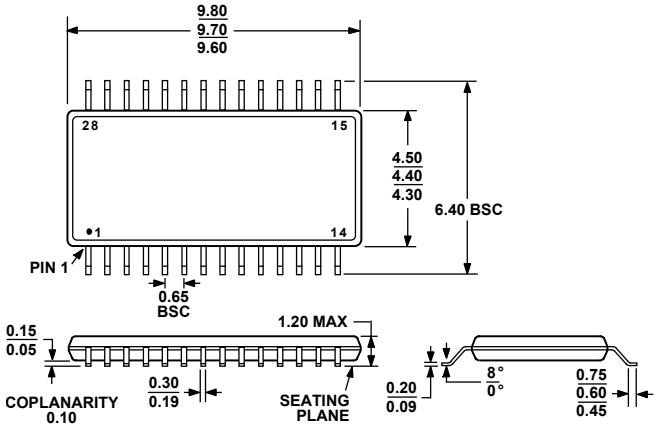


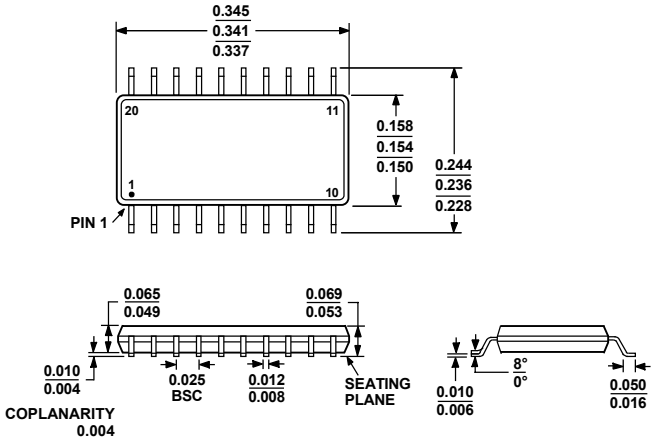
Figure 94. Signal Path and Board Layout for AD8334

OUTLINE DIMENSIONS



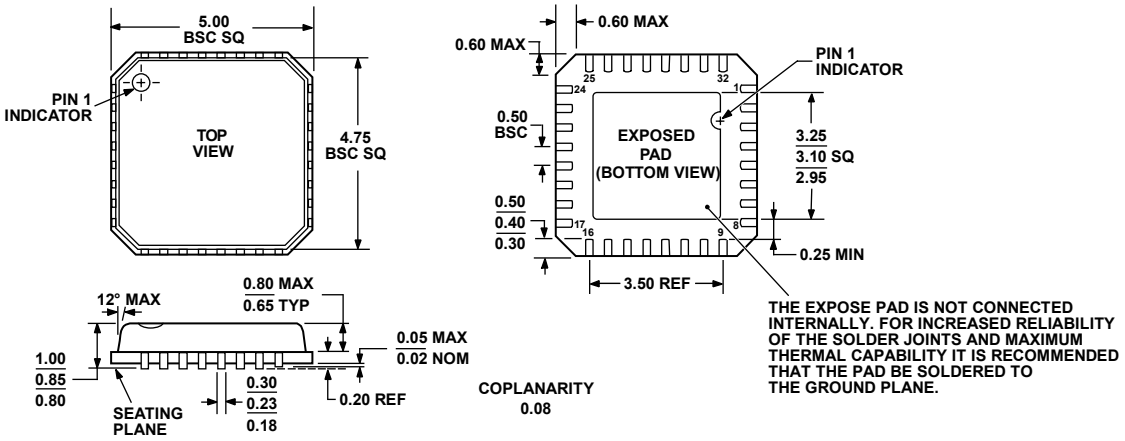
COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 95. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137-AD

Figure 96. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in Inches



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 97. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

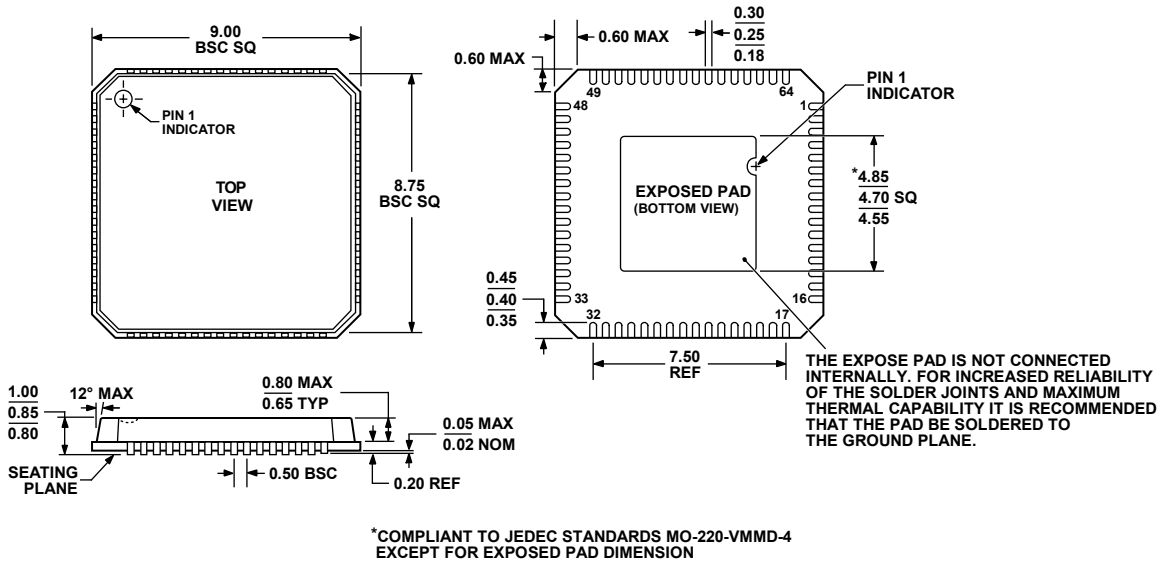


Figure 98. 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8331ARQ	–40°C to +85°C	20-Lead Shrink Small Outline Package (QSOP)	RQ-20
AD8331ARQ-REEL	–40°C to +85°C	20-Lead Shrink Small Outline Package (QSOP)	RQ-20
AD8331ARQ-REEL7	–40°C to +85°C	20-Lead Shrink Small Outline Package (QSOP)	RQ-20
AD8331ARQZ[1]	–40°C to +85°C	20-Lead Shrink Small Outline Package (QSOP)	RQ-20
AD8331ARQZ-RL[1]	–40°C to +85°C	20-Lead Shrink Small Outline Package (QSOP)	RQ-20
AD8331ARQZ-R7[1]	–40°C to +85°C	20-Lead Shrink Small Outline Package (QSOP)	RQ-20
AD8331-EVAL		Evaluation Board with AD8331ARQ	
AD8332ACP-R2	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-2
AD8332ACP-REEL	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-2
AD8332ACP-REEL7	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-2
AD8332ACPZ-R7[1]	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-2
AD8332ACPZ-RL[1]	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-2
AD8332ARU	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD8332ARU-REEL	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD8332ARU-REEL7	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD8332ARUZ[1]	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD8332ARUZ-R7[1]	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD8332ARUZ-RL[1]	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD8332-EVAL		Evaluation Board with AD8332ARU	
EVAL-AD8332/AD9238		Evaluation Board with AD8332ARU and AD9238 ADC	
AD8334ACPZ-WP[1]	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1
AD8334ACPZ-REEL[1]	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1
AD8334ACPZ-REEL7[1]	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1
AD8334-EVAL		Evaluation Board with AD8334ACP	

[1] Z = Pb-free part.

©2006 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
C03199-0-4/06(E)