ATP Industrial Grade CompactFlash Card Specification

Revision 3.6

Disclaimer:

ATP Electronics Inc. shall not be liable for any errors or omissions that may appear in this document, and disclaims responsibility for any consequences resulting from the use of the information set forth herein.

The information in this manual is subject to change without notice.

ATP general policy does not recommend the use of its products in life support applications where in a failure or malfunction of the product may directly threaten life or injury.

The information set forth in this document is considered to be "Proprietary" and "Confidential" property owned by ATP.

Revision History

Date	Version	Changes compared to previous issue
Aug.25th,2010	2.3	- Update 16GB capacity - Update certification and compliance - Update CHS Parameters - Update Type II CF card information
Jan.26th,2011	3.0	- Support S.M.A.R.T. command - StaticDataRefresh and EarlyRetirement Technology - Update performance - Update MTBF - Revise density
Feb.25th,2011	3.1	- Revise Figure 4-1: ATP S.M.A.R.T. tool operation - Revise UDMA mode 0~4
Apr.14th,2011	3.2	- Add power failure protection feature
Sep.30th,2011	3.3	- Preliminary spec sheet of Industrial grade CF card with PowerProtector feature - Update new P/N and performance - Update ATP branch/office contact information
Dec.16th，2011	3.31	- Official released version - Revise Table 3-19: Ultra DMA Data Burst Timing Requirements - Revise environment specifications
Jan.31st, 2012	3.4	- Add density 512MB/1GB/2GB
Mar.14th, 2012	3.5	- Add TBW (Total Bytes Written) information - Revise StaticDataRefresh technology
Nov. 8th, 2012	3.6	- Revise table 2-1 system power table

Table of Contents

1 ATP Industrial Grade CompactFlash Card Overview

1.1 ATP Product Availability

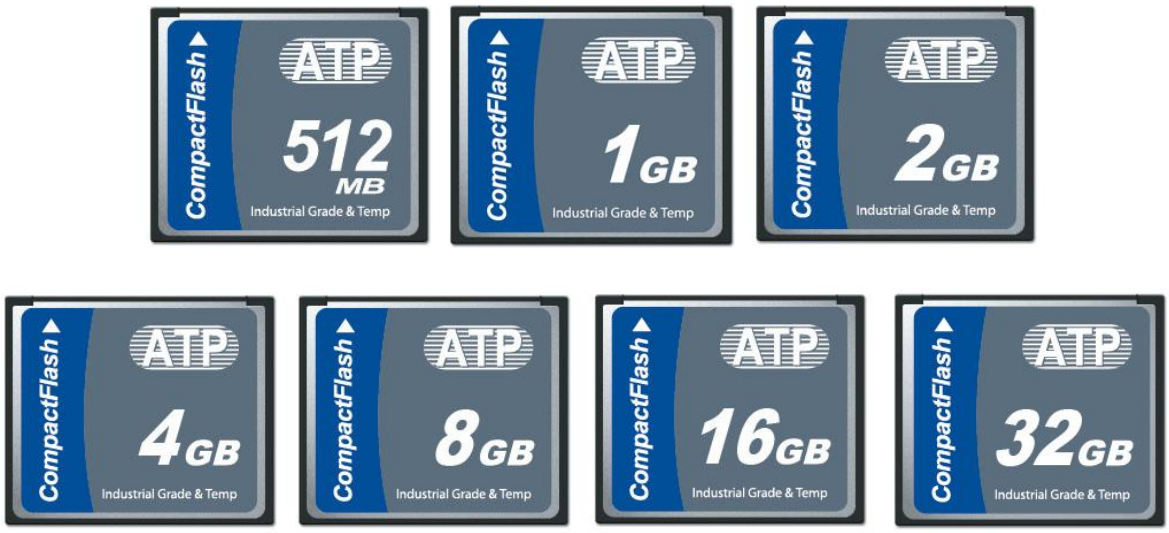


Figure 1-1: ATP Product Availability

Table 1-1: Capacities

ATP P/N	CAPACITY
AF512CFI-7ACXP	512MB
AF1GCFI-7ACXP	1GB
AF2GCFI-7ACXP	2GB
AF4GCFI-7ACXP	4GB
AF8GCFI-7ABXP	8GB
AF16GCFI-7ABXP	16GB
AF32GCFI-7AAXP	32GB

*Note: ” P” stands for PowerProtector feature

1.2 Introduction

By utilizing SLC NAND flash memory and advanced Global Wear Leveling technology, the ATP Industrial Grade CompactFlash Card has enhanced endurance levels and a longer product lifespan. The ATP Industrial Grade CF card implements the StaticDataRefresh technology, which monitors the error bit levels during each read operation to ensure data integrity, and the EarlyRetirement technology prevents data loss from weak blocks.

The ATP Industrial Grade CF card has also incorporated the S.M.A.R.T. (Self-Monitoring, Analysis, and Reporting Technology) function which monitors various parameters of endurance and reliability, indicating activity that is out of the normal range. This information helps predict storage failure for preventative action.

Patent ATP PowerProtector technology is implemented in ATP industrial grade CF card to ensure a sufficient amount of backup power during power abnormalities to minimize the risk of data loss or firmware corruption.

1.3 Main Features

- **Host Interface:**
  - λ Compliance with CF specification 4.1
  - λ Pre-screened Single Level Cell (SLC) NAND flash memory
  - λ True IDE mode compatible:

    Support PIO mode 0~6, MDMA mode 0~2, UDMA mode 0~4
- **High performance:**
  - λ Sequential read up to 51MByte/s (UDMA 4, Flash number x 2)
  - λ Sequential write up to 25MByte/s (UDMA 4, Flash number x 2)
  - λ Capacity: 512MB to 32GB
- **Industrial grade temp.**: -40^{o}C to 85^{o}C
- **Endurance:**
  - λ Enhanced endurance by *Global wear leveling* and bad block management
  - λ 13/24 bit BCH-ECC engines can correct up to 24 bit errors per 1,024 byte data
  - λ MTBF > 5,000,000 hours (@25^{o}C)
  - λ Data reliability: Bit error rate 10E-15 (NAND flash)
  - λ Number of connector insertion/removals: >10,000

- **StaticDataRefresh technology to assure data integrity in read operations.**
- **PowerProtector, built-in power-down data protection**
- **S.M.A.R.T. function support for life time monitor**
- **Power saving mode (automatic sleep and wake-up mechanism)**

1.4 Application

ATP Industrial Grade CF cards are designed for demanding industrial applications, such as military/aerospace, automation, marine navigation, embedded systems, telecommunication equipment or networking and medical equipment where mission-critical data requires the highest level of reliability, durability, and data integrity.

2 Product Specification

2.1 System Power Requirement

Table2-1: System power table

Voltage	Maximum Average RMS Current	Measurement Method
3.3V +/- 5%	75mA (500mA in Power Level 1)	3.3V at 25℃
5.0V +/- 10%	100mA (500mA in Power Level 1)	5.0V at 25℃

2.2 Environment Specifications

Table2-2: Environment Specifications

Type		Standard
Temperature	Operating	-40℃ to 85℃
	Non-Operating	-40℃ to 85℃
Humidity	Storage	40℃, 93% RH / 500hrs 85℃,85%RH / 500hrs
Random Vibration test	Non-Operating	10~2000Hz, 6Grms, 30min per axis
Drop test	Non-Operating	150cm/Free fall
UV light exposure test (ISO 7816-1)	Non-Operating	254nm, 15Ws/cm2

2.3 Reliability

Table 2-3: Reliability

Type	Measurement
Number of insertions	10,000 minimum
Endurance	100,000 P/E cycles SLC NAND Flash cell endurance
TBW (Total Bytes Written)	512MB 10 terabyte random write 1GB 20 terabyte random write 2GB 40 terabyte random write 4GB 80 terabyte random write 8GB 160 terabyte random write 16GB 320 terabyte random write 32GB 640 terabyte random write
MTBF (@ 25°C)	> 5,000,000 hours

Note: Endurance for flash cards can be predicted based on the usage conditions applied to the device, the internal NAND flash cycles, the write amplification factor, and the wear leveling efficiency of the flash devices.

2.4 Performance

Table 2-4: Performance

Model P/N	Seq. Read (KB/s)	Seq. Write (KB/s)	Random Read (KB/s)	Random Write (KB/s)
AF512CFI-7ACXP	24945	10742	24265	3408
AF1GCFI-7ACXP	29446	15597	28464	5200
AF2GCFI-7ACXP	30476	16075	29090	5624
AF4GCFI-7ACXP	50319	19266	44377	6285
AF8GCFI-7ABXP	51328	24945	44377	7261
AF16GCFI-7ABXP	51328	25190	44377	7402
AF32GCFI-7AAXP	50381	24945	43620	7553

Note: Tested by HDBench 3.40 beta6 with 40MB file size. The performance may vary based on different testing environments.

2.5 CHS Parameters

Table 2-5 CHS Table

SM2232AD with SLC						
Product density	**Flash type**	**Cylinders**	**Heads**	**Sectors**	**Total sectors**	**Physical capacity**
512MB	2K page	991	16	63	998928	511451136
1GB	2K page	1966	16	63	1981728	1014644736
2GB	2K page	3900	16	63	3931200	2012774400
4GB	8K page	7785	16	63	7847280	4017807360
8GB	8K page	15538	16	63	15662304	8019099648
16GB	8K page	31045	16	63	31293360	16022200320
32GB	8K page	62041	16	63	62537328	32019111936

2.6 Extra Features

Table 2-6: Extra Features

Type	Measurement
ESD Proof	Yes
RoHS Compliant	Yes
ESD Proof	IEC 61000-4-2: non-contact pad (Coupling plane discharge) +/- 8KV, non-contact pad (Air discharge) +/- 15KV

2.7 Global Wear Leveling- Longer Life Expectancy

The program / erase cycle of each sector/page/block is finite. Writing constantly on the same spot will cause the flash to wear out quickly. Furthermore, bit errors are not proportioned to P/E cycles; sudden death may occur when the block is close to its P/E cycle limit. Then unrecoverable bit errors will cause fatal data loss (especially for system data or FAT).

Global wear leveling algorithm evenly distributes the P/E cycles of each block to minimize the possibility of one block exceeding its max P/E cycles before the rest. In return, the life expectancy of memory storage device is prolonged and the chance/occurrence of unrecoverable bit errors could be reduced.

2.8 StaticDataRefresh Technology – Assure Data Integrity

Over time the error bits accumulate to the threshold in the flash memory cell and eventually become uncorrectable despite using the ECC engine. In the traditional handling method, the data is moved to a different location in the flash memory; despite the corrupted data is beyond repaired before the transition.

To prevent data corruption, the CF card monitors the error bit levels in each read operation; when it reaches the preset threshold value, StaticDataRefresh is achieved by erasing and re-programming the data into the same block or into another block. After the re-programming operation is completed, the controller reads the data and compares the data/parity to ensure data integrity.

2.9 ATP PowerProtector – Built-in Power Down Data Protection

ATP PowerProtector technology ensures a sufficient amount of reserve power during any power abnormalities such as unstable voltages and power outages. PowerProtector's patent pending technology is a stand alone hardware design that does not require specific controllers or customized firmware. This feature provides greater flexibility during the design of a smaller form factor such as CompactFlash cards.

During a sudden power failure, the drive then draws power from PowerProtector's solid state capacitors for reserve power, which guarantee reliable drive operations. The solid state capacitors allow the flash to finish processing the last command or data.

SuperCap, the traditional power protection design, is well known for its sensitivity to temperature change and has a tendency of losing its capacitance and functionality at extreme temperatures. The average life span of SuperCap is less than two years; the capacitance will degrade over time and eventually fail to perform.

ATP PowerProtector surpasses the natural limitations of SuperCap designs by supporting wide temperature and an average life span of over five years without capacitance degradation.

PowerProtector offers an advanced level of protection ensuring that data integrity is not compromised during a power failure scenario, and preserves critical data in mission critical applications.

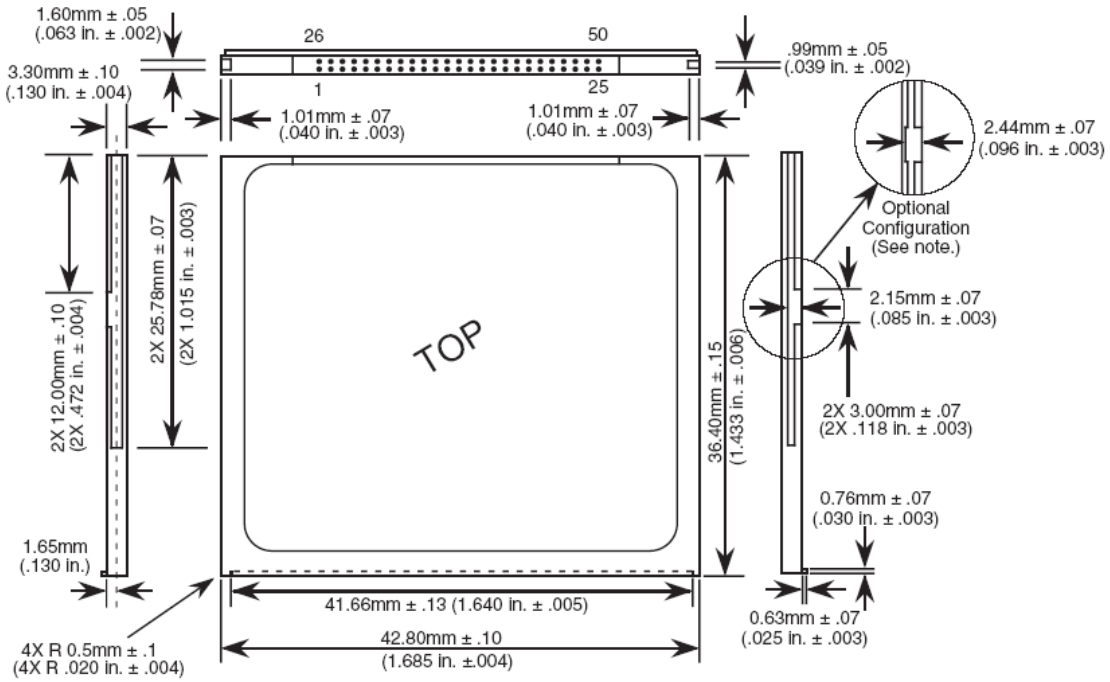
2.10 Physical Dimension Specification

Table 2-7: Physical Specifications

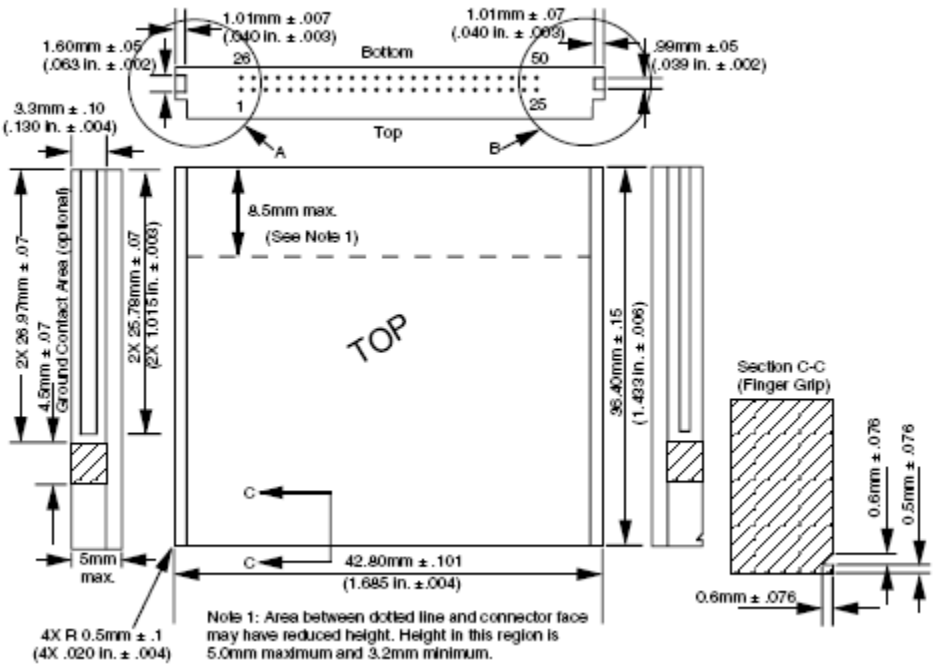
Type		Measurement
Type I	Length	36.4mm ± 0.15mm
	Width	42.8mm ± 0.10mm
	Thickness	3.3mm ±0.10mm
	Weight	9.0 g typical
Type II	Length	36.4mm ± 0.15mm
	Width	42.8mm ± 0.10mm
	Thickness	5.0mmMax
	Weight	9.0 g typical

2.11 Mechanical Form Factor (Units in MM)

Figure 2-1: ATP CompactFlash Card Physical Dimensions



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.



Type II

2.12 Certification and compliance

2.12.1 Certification table

Table 2-8: Certification table

Mark/Approval	Documentation	Certification
CE	The CE marking (also known as CE mark) is a mandatory conformance mark on many products placed on the single market in the European Economic Area (EEA). The CE marking certifies that a product has met EU consumer safety, health or environmental requirements. CE stands for Conformité Européenne, "European conformity" in French.	Yes
FC	FCC Part 15 Class B was used for Evolution of United States (US) Emission Standards for Commercial Electronic Products, The United States (US) covers all types of unintentional radiators under Subparts A and B (Sections 15.1 through 15.199) of FCC 47 CFR Part 15, usually called just FCC Part 15	Yes
RoHS	RoHS is the acronym for Restriction of Hazardous Substances. RoHS, also known as Directive 2002/95/EC, originated in the European Union and restricts the use of specific hazardous materials found in electrical and electronic products. All applicable products in the EU market after July 1, 2006 must pass RoHS compliance. For the complete directive, see Directive 2002/95/EC of the European Parliament.	Yes

3 Electrical Interface

3.1 Pin Assignments and Pin Type

The host is connected to the CompactFlash Card using a standard 50-pin connector. The connector in the host consists of two rows of 25 male contacts each on 50 mil (1.27 mm) centers.

The signal/pin assignments are listed in Table 3-1. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Section 3.3 defines the DC characteristics for all input and output type structures.

Table 3-1: Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[13]			
Pin	Signal Name	Pin Type	In, Out Type	Pin	Signal Name	Pin Type	In, Out Type	Pin	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	Ground	I1Z,OZ3	2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3
7	−CE1	I	I3U	7	−CE1	I	I3U	7	−CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	−OE	I	I3U	9	−OE	I	I3U	9	−ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09[2]	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08[2]	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07[2]	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06[2]	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05[2]	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04[2]	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03[2]	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3
23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3

24	WP	O	OT3	24	−IOIS16	O	OT3	24	−IOIS16	O	ON3
PC Card Memory Mode				**PC Card I/O Mode**				**True IDE Mode13**			
Pin	**Signal Name**	**Pin Type**	**In, Out Type**	**Pin**	**Signal Name**	**Pin Type**	**In, Out Type**	**Pin**	**Signal Name**	**Pin Type**	**In, Out Type**
25	−CD2	O	Ground	25	−CD2	O	Ground	25	−CD2	O	Ground
26	−CD1	O	Ground	26	−CD1	O	Ground	26	−CD1	O	
27	D11[1]	I/O	I1Z,OZ 3	27	D11[1]	I/O	I1Z,OZ 3	27	D11[1]	I/O	I1Z,OZ3
28	D12[1]	I/O	I1Z,OZ 3	28	D12[1]	I/O	I1Z,OZ 3	28	D12[1]	I/O	I1Z,OZ3
29	D13[1]	I/O	I1Z,OZ 3	29	D13[1]	I/O	I1Z,OZ 3	29	D13[1]	I/O	I1Z,OZ3
30	D14[1]	I/O	I1Z,OZ 3	30	D14[1]	I/O	I1Z,OZ 3	30	D14[1]	I/O	I1Z,OZ3
31	D15[1]	I/O	I1Z,OZ 3	31	D15[1]	I/O	I1Z,OZ 3	31	D15[1]	I/O	I1Z,OZ3
32	−CE2[1]	I	I3U	32	−CE2[1]	I	I3U	32	−CS1[1]	I	I3Z
33	−VS1	O	Ground	33	−VS1	O	Ground	33	−VS1	O	Ground
34	-IORD HSTROBE[9] HDMARDY[10]	I	I3U	34	-IORD HSTROBE[9] HDMARDY[10]	I	I3U	34	-IORD[6] HSTROBE[7] HDMARDY[8]	I	I3Z
35	−IOWR STOP[9,10]	I	I3U	35	−IOWR STOP[9,10]	I	I3U	35	−IOWR[6] STOP[7,8]	I	I3Z
36	−WE	I	I3U	36	−WE	I	I3U	36	−WE[3]	I	I3U
37	READY	O	OT1	37	−IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	−CSEL[4]	I	I2Z	39	−CSEL[4]	I	I2Z	39	−CSEL	I	I2U
40	−VS2	O	OPEN	40	−VS2	O	OPEN	40	−VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	−RESET	I	I2Z
42	−WAIT −DDMARDY[9] DSTROBE[10]	O	OT1	42	−WAIT −DDMARDY[9] DSTROBE[10]	O	OT1	42	IORDY[6] −DDMARDY[7] DSTROBE[8]	O	ON1 / OT1[12]
43	−INPACK −DMARQ[11]	O	OT1	43	−INPACK −DMARQ[11]	O	OT1	43	DMARQ	O	OZ1
44	−REG −DMARQ[11]	I	I3U	44	−REG −DMARQ[11]	I	I3U	44	−DMACK[5]	I	I3U
45	BVD2	O	OT1	45	−SPKR	I/O	OT1	45	−DASP	I/O	I1U,ON 1
46	BVD1	O	OT1	46	−STSCHG	I/O	OT1	46	−PDIAG	I/O	I1U,ON 1
47	D08[1]	I/O	I1Z,OZ 3	47	D08[1]	I/O	I1Z,OZ 3	47	D08[1]	I/O	I1Z,OZ3
48	D09[1]	I/O	I1Z,OZ 3	48	D09[1]	I/O	I1Z,OZ 3	48	D09[1]	I/O	I1Z,OZ3
49	D10[1]	I/O	I1Z,OZ 3	49	D10[1]	I/O	I1Z,OZ 3	49	D10[1]	I/O	I1Z,OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

Notes:

1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2) The signal should be grounded by the host.
3) The signal should be tied to VCC by the host.
4) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
5) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older

hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition

6) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
7) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.
9) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active.
10) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.
11) Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active.
12) Signal is a totem-pole output during Ultra DMA data bursts in True IDE mode.
13) The mode is optional for CF+ Cards, but required for CompactFlash Storage Cards.

3.2 Electrical Description

The CompactFlash Card functions in three basic modes:

1) PC Card ATA using I/O Mode

2) PC Card ATA using Memory Mode

3) True IDE Mode, which is compatible with most disk drives.

ATP Industrial CompactFlash Card supports all three modes. The configuration of the CompactFlash Card is controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the storage card or for True IDE Mode, pin 9 being grounded.

Table 3-2: Signal Description

SIGNAL NAME	DIR.	PIN	DESCRIPTION
A10 - A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Card, the memory mapped port address registers within the CompactFlash Card, a byte in the card's information structure and its configuration control and status registers.
A10 - A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode)		18,19,20	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-CD1, -CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Card. They are used by the host to determine that the CompactFlash Card is fully inserted into its socket.

SIGNAL NAME	DIR.	PIN	DESCRIPTION
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)	--	1,50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.

SIGNAL NAME	DIR.	PIN	DESCRIPTION
-INPACK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the CompactFlash Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card and the CPU. Hosts that support a single socket per interface logic, such as for Advanced Timing Modes and Ultra DMA operation may ignore the –INPACK signal from the device and manage their input buffers based solely on Card Enable signals.
DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with (-)DMACK, In PCMCIA I/O Mode, the -DMARQ shall be ignored by the host while the host is performing an I/O Read cycle to the device. The host shall not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1)and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode operation. A host that does not support DMA mode and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode. is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1)and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits.

SIGNAL NAME	DIR.	PIN	DESCRIPTION
-IORD (PC Card Memory Mode except Ultra DMA Protocol Active)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode except Ultra DMA Protocol Active)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
-HDMARDY (All Modes - Ultra DMA Protocol DMA Read)			In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer.
HSTROBE (All Modes - Ultra DMA Protocol DMA Write)			In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (PC Card Memory Mode – Except Ultra DMA Protocol Active)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode – Except Ultra DMA Protocol Active)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (All Modes – Ultra DMA Protocol Active)			In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.

SIGNAL NAME	DIR.	PIN	DESCRIPTION
-OE (PC Card Memory Mode) -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
-IREQ (PC Card I/O Mode) INTRQ (True IDE Mode)			I/O Operation – After the CompactFlash Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode – Except Ultra DMA Protocol Active) Attribute Memory Select -REG (PC Card I/O Mode – Except Ultra DMA Protocol Active) -DMACK (PC Card Memory Mode when Ultra DMA Protocol Active) DMACK (PC Card I/O Mode when Ultra DMA Protocol Active) -DMACK (True IDE Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal negated during the execution of any DMA Command by the Device The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device. This is a DMA Acknowledge signal that is asserted by the host in response to (-)DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-)DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PC Card and True-IDE modes of operation need not alter the PC Card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.

SIGNAL NAME	DIR.	PIN	DESCRIPTION
RESET (PC Card Memory Mode)	I	41	The CompactFlash Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	--	13,38	+5 V, +3.3 V power.
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.

SIGNAL NAME	DIR.	PIN	DESCRIPTION
-WAIT (PC Card Memory Mode – Except Ultra DMA Protocol Active) -WAIT (PC Card I/O Mode – Except Ultra DMA Protocol Active) IORDY (True IDE Mode – Except Ultra DMA Protocol Active) -DDMARDY (All Modes – Ultra DMA Write Protocol Active) DSTROBE (All Modes – Ultra DMA Read Protocol Active)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer. In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O Mode) -IOCS16 (True IDE Mode)	O	24	Memory Mode – The CompactFlash Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation – When the CompactFlash Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

3.3 Electrical Specification

The following tables define all D.C. Characteristics for the ATP Industrial Grade CompactFlash Card Series. Unless otherwise stated, conditions are:

Vcc = 5V ±10%

Vcc = 3.3V ± 10%

Table 3-3: Absolute Maximum Conditions

PARAMETER	SYMBOL	CONDITIONS
Input Power	Vcc	-0.3V min. to 6.5V max.
Voltage on any pin except Vcc with respect to GND.	V	-0.5V min. to Vcc + 0.5V max.

3.3.1 Input Leakage Current

Note: In Table 3-4 below, x refers to the characteristics. For example, I1U indicates a pull-up resistor with a type 1 input characteristic.

Table 3-4: Input Leakage Current

TYPE	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IxZ	Input Leakage Current	IL	Vih = Vcc / Vil = Gnd	-1		1	µA
IxU	Pull-Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
IxD	Pull-Down Resistor	RPD1	Vcc = 5.0V	50k		500k	Ohm

Note:

The minimum pull-up resistor leakage current meets the PCMCIA specification of 10k ohms but is intentionally higher in the CompactFlash Specification to reduce power use.

3.3.2 Input Characteristics

Table 3-5: Input Characteristics

TYPE	PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
			VCC = 3.3 V			VCC = 5.0 V			
1	Input Voltage CMOS	Vih Vil	2.4		 0.6	4.0 [1]		 0.8	Volts
2	Input Voltage CMOS	Vih Vil	1.5		 0.6	2.0		 0.8	Volts
3	Input Voltage CMOS Schmitt Trigger	Vth Vtl		1.8 1.0			2.8 2.0		Volts

Notes:

Per PCMCIA Electrical Specification Signal Interface note 1, the host provides a logic output high voltage for a CMOS load of .9 x VCC. For a 5 volt product, this translates to .9 x 4.5 = 4.05 volts minimum Voh.

In UDMA modes greater than 4, the following characteristics apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table 3-6: Input Characteristics (UDMA Mode > 4)

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC supply voltage to receivers	V_{DD3}	3.3 - 8%	3.3 + 8%	Volts
Low to high input threshold	V+	1.5	2.0	Volts
High to low input threshold	V−	1.0	1.5	Volts
Difference between input thresholds: ((V+current value) − (V−current value))	V_{HYS}	320		mV
Average of thresholds: ((V+current value) + (V−current value))/2	V_{THRAVG}	1.3	1.7	Volts

Note:

In Table 3-7 below, x refers to the characteristics. For example, OT3 refers to Totem pole output with a type 3 output drive characteristic.

3.3.3 Output Drive Type

Table 3-7: Output Drive Type

TYPE	OUTPUT TYPE	VALID CONDITIONS
OTx	Totempole	Ioh & Iol
OZx	Tri-State N-P Channel	Ioh & Iol
OPx	P-Channel Only	Ioh Only
ONx	N-Channel Only	Iol Only

3.3.4 Output Drive Characteristics

Table 3-8: Output Drive Characteristics

TYPE	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
2	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
3	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
X	Tri-State Leakage Current	Ioz	Vol = Gnd Voh = Vcc	-10		10	µA

In UDMA modes greater than 4, the characteristics specified in the following table apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table 3-9: Output Drive (UDMA Mode > 4)

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC supply voltage to drivers	V_{DD3}	3.3 - 8%	3.3 + 8%	Volts
Voltage output high at -6 mA to +3 mA (at VoH2 the output shall be able to supply and sink current to VDD3)	V_{oH2}	V_{DD3} - 0.51	V_{DD3} + 0.3	Volts
Voltage output low at 6 mA	V_{oL2}		0.51	Volts

Notes:

1) IoLDASP shall be 12 mA minimum to meet legacy timing and signal integrity.
2) IoH value at 400 µA is insufficient in the case of DMARQ that is pulled low by a 5.6 kΩ resistor.
3) Voltage output high and low values shall be met at the source connector to include the effect of series termination.
4) A device shall have less than 64 µA of leakage current into a 6.2 KΩ pull-down resistor while the INTRQ signal is in the released state.

3.3.5 Attribute Memory Read Timing

Attribute Memory access time is defined as 300 ns. Detailed timing specs are shown in Table 3-10.

Table 3-10: Attribute Memory Read Timing

SPEED VERSION			300 NS	
ITEM	SYMBOL	IEEE SYMBOL	MIN ns.	MAX ns.
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

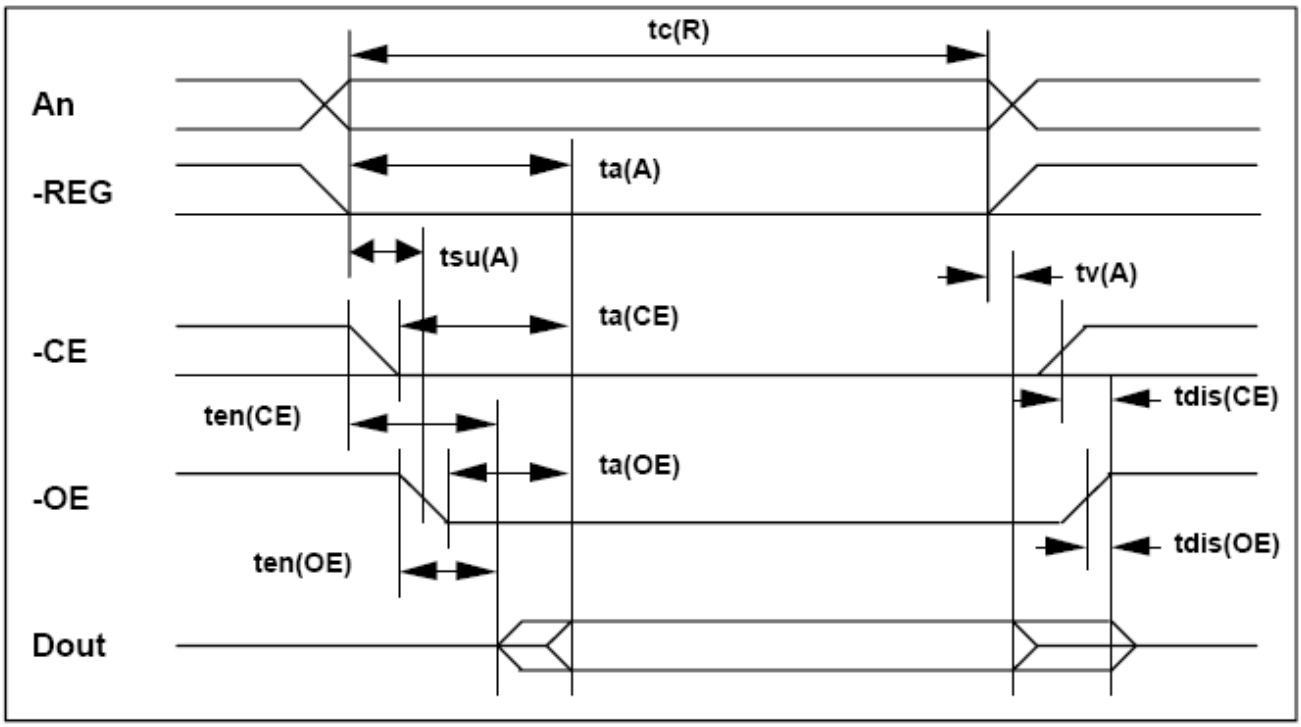


Figure 3-1: Attribute Memory Read Timing Diagram

3.3.6 Configuration Register (Attribute Memory) Write Timing Specification

Table 3-11: Configuration Register (Attribute Memory) Write Timing

SPEED VERSION			250 ns	
ITEM	SYMBOL	IEEE SYMBOL	MIN ns	MAX ns
Write Cycle Time	Tc(W)	tAVAV	250	
Write Pulse Width	Tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	Th(D)	tWMDX	30	

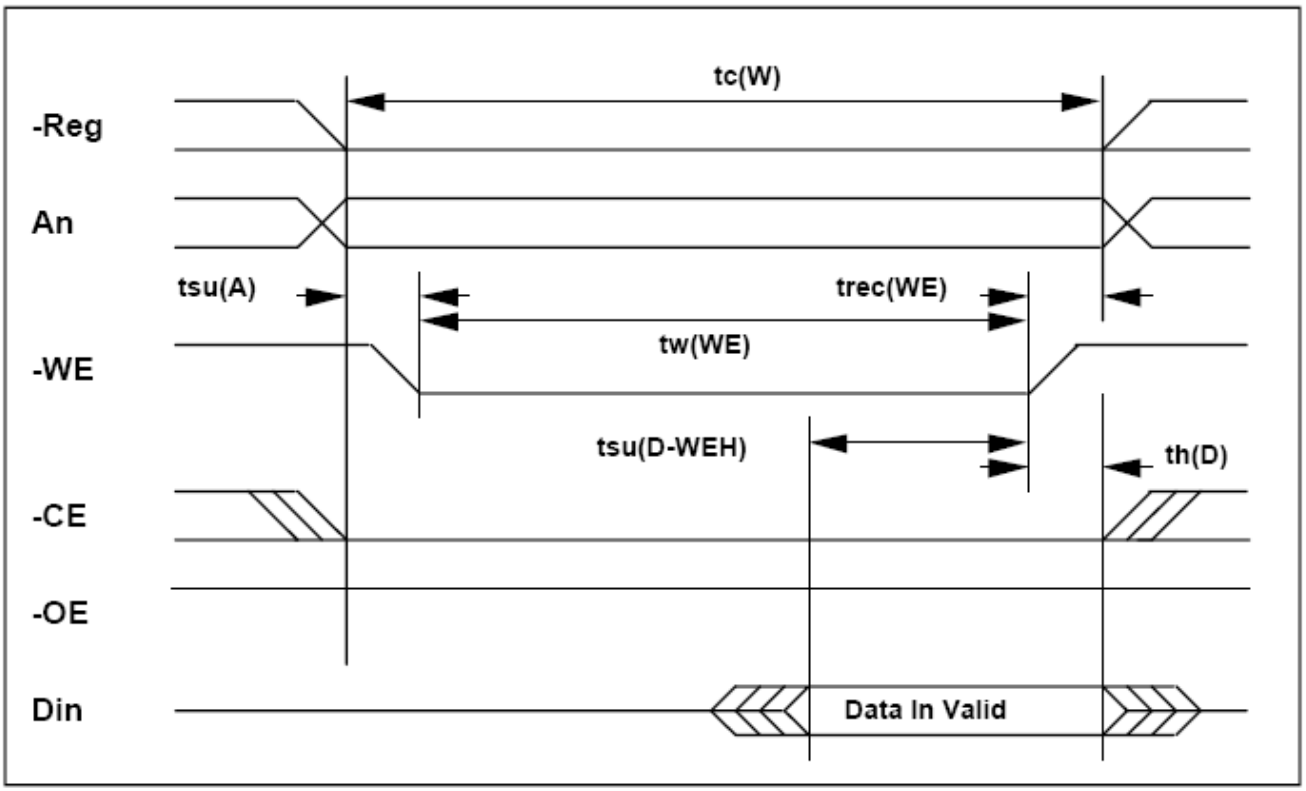


Figure 3-2: Configuration Register (Attribute Memory) Write Timing Diagram

3.3.7 Common Memory Read Timing Specification

Table 3-12: Common Memory Read Timing

CYCLE TIME MODE:			250 ns		120 ns		100 ns		80 ns	
ITEM	SYMBOL	IEEE SYMBOL	MIN ns.	MAX ns.	MIN ns.	MAX ns.	MIN ns.	MAX ns.	MIN ns.	MAX ns.
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		na[1]
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350		350		350		na[1]

Notes:

1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load.

All times are in nanoseconds. Dout signifies data provided by the CompactFlash Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

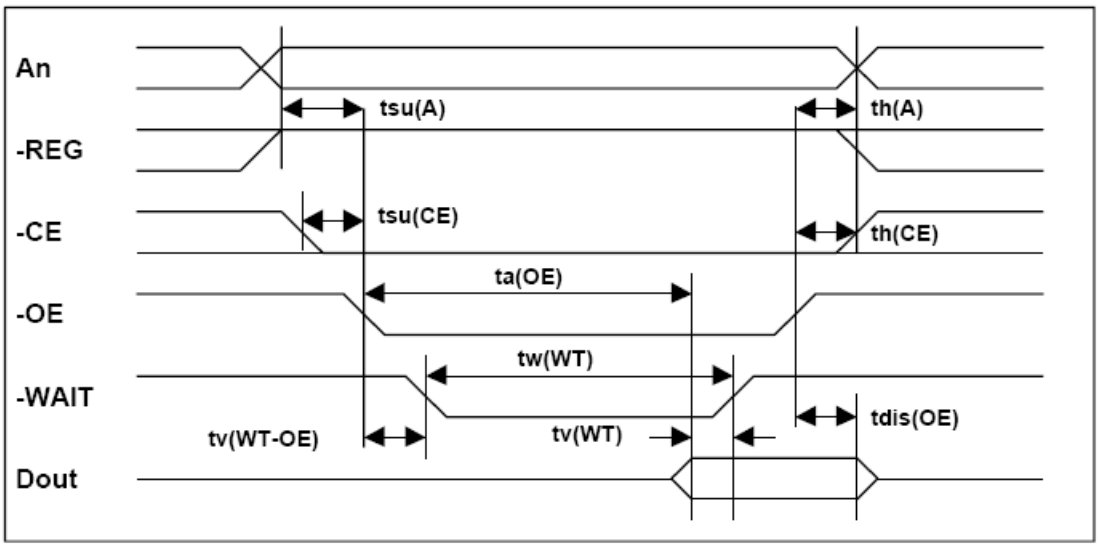


Figure 3-3: Common Memory Read Timing Diagram

3.3.8 Common Memory Write Timing Specification

Table 3-13: Common Memory Write Timing

CYCLE TIME MODE:			250 ns		120 ns		100 ns		80 ns	
ITEM	SYMBOL	IEEE SYMBOL	MIN ns.	MAX ns.	MIN ns.	MAX ns.	MIN ns.	MAX ns.	MIN ns.	MAX ns.
Data Setup before WE	tsu (D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
CYCLE TIME MODE:			**250 ns**		**120 ns**		**100 ns**		**80 ns**	
ITEM	**SYMBOL**	**IEEE SYMBOL**	**MIN ns.**	**MAX ns.**	**MIN ns.**	**MAX ns.**	**MIN ns.**	**MAX ns.**	**MIN ns.**	**MAX ns.**
Wait Delay Falling from WE	tv (WT-WE)	tWLWTV		35		35		35		na[1]
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw (WT)	tWTLWTH		350		350		350		na[2`]

Notes:

1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load.

All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

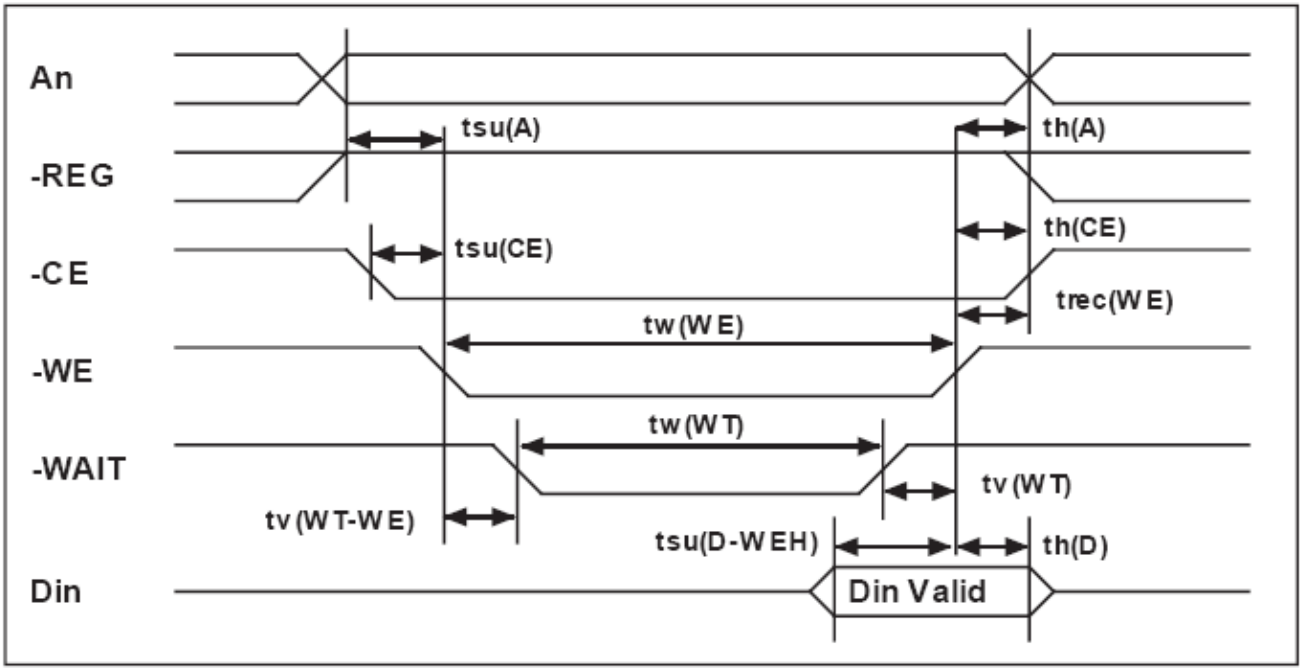


Figure 3-4: Common Memory Write Timing

3.3.9 I/O Input (Read) Timing Specification

Table 3-14: I/O Read Timing

CYCLE TIME MODE:			250 ns		120 ns		100 ns		80 ns	
ITEM	SYMBOL	IEEE SYMBOL	MIN ns.	MAX ns.	MIN ns.	MAX ns.	MIN ns.	MAX ns.	MIN ns.	MAX ns.
Data Delay after IORD	td(IORD)	tlGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tlGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tlGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tlGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tlGHEH	20		10		10		10	

REG Setup before IORD	tsuREG (IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG (IORD)	tlGHRGH	0		0		0		0	
INPACK Delay Falling from IORD[3]	tdfINPACK (IORD)	tlGLIAL	0	45	0	na1	0	na1	0	na1
INPACK Delay Rising from IORD[3]	tdrINPACK (IORD)	tlGHIAH		45		na[1]		na[1]		na[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IORD[3]	tdWT(IORD)	tlGLWTL		35		35		35		na[2]
Data Delay from Wait Rising[3]	td(WT)	tWTHQV		0		0		0		na[2]
Wait Width Time[3]	tw(WT)	tWTLWTH		350		350		350		na[2]

Notes:

1) -IOIS16 and -INPACK are not supported in this mode.
2) -WAIT is not supported in this mode.
3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.

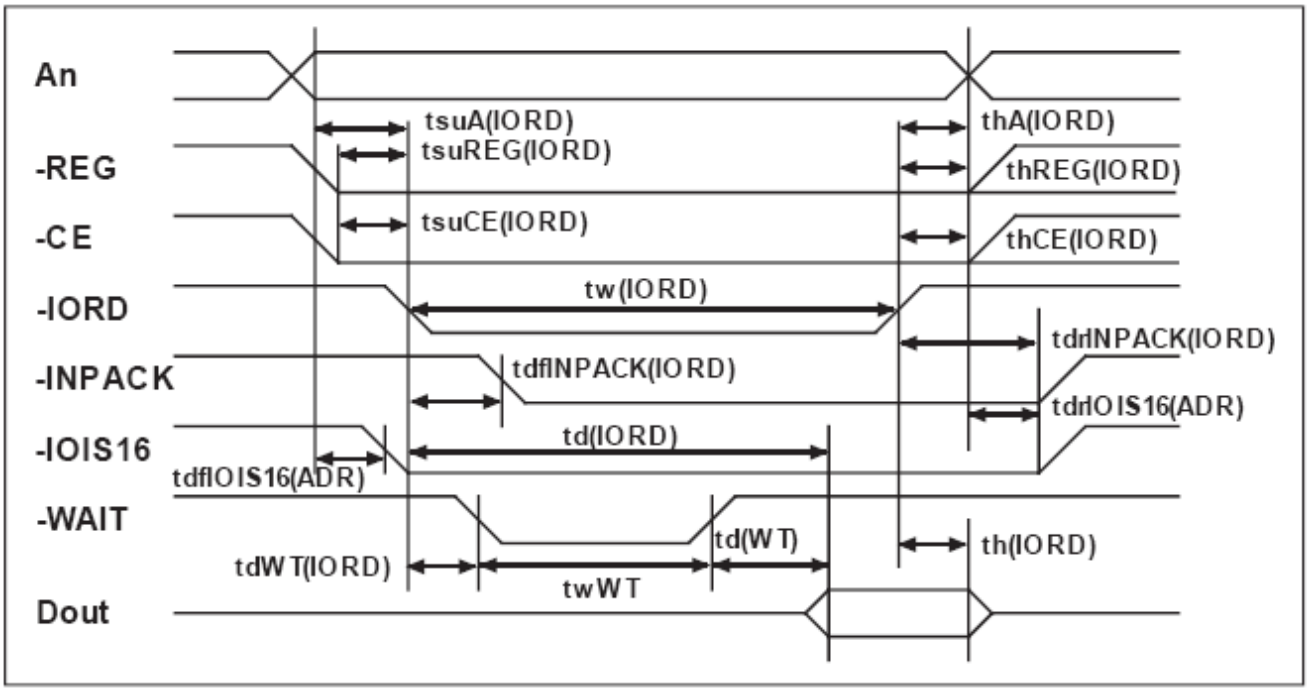


Figure 3-5: I/O Read Timing Diagram

3.3.10 I/O Output (Write) Timing Specification

Table 3-15: I/O Write Timing

CYCLE TIME MODE:			255 ns		120 ns		100 ns		80 ns	
ITEM	SYMBOL	IEEE SYMBOL	MIN ns.	MAX ns.	MIN ns.	MAX ns.	MIN ns.	MAX ns.	MIN ns.	MAX ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tlWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tlWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tlWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE (IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE (IOWR)	tlWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG (IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG (IOWR)	tlWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address3	tdfIOIS16 (ADR)	tAVISL		35		na1		na1		na1
IOIS16 Delay Rising from Address3	tdrIOIS16 (ADR)	tAVISH		35		na1		na1		na1
Wait Delay Falling from IOWR3	tdWT(IOWR)	tlWLWTL		35		35		35		na2
IOWR high from Wait high3	tdrIOWR (WT)	tWTJIWH	0		0		0		na2	
Wait Width Time3	tw(WT)	tWTLWTH		350		350		350		na2

Notes:

1) -IOIS16 and -INPACK are not supported in this mode.
2) -WAIT is not supported in this mode.
3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the CompactFlash Card. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.

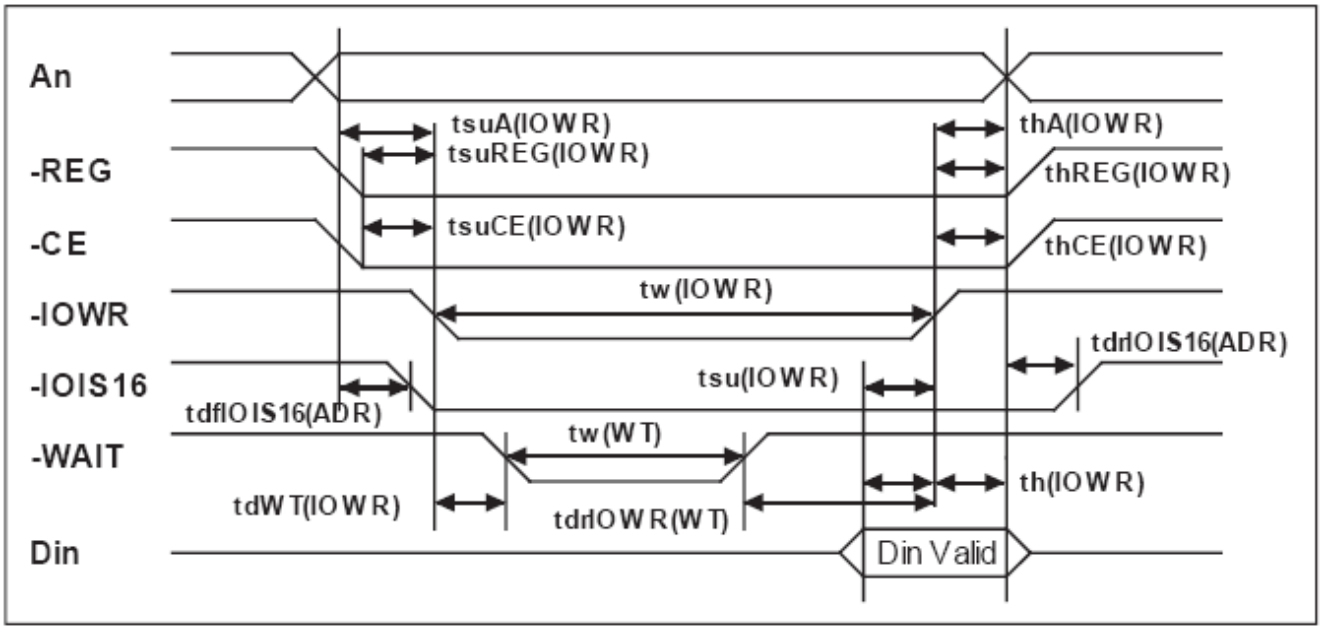


Figure 3-6: I/O Write Timing Diagram

3.3.11 True IDE PIO Mode Read/Write Timing Specification

The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 3-16: True IDE PIO Mode Read/Write Timing

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data hold (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na[5]	na[5]	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]	
tC	IORDY assertion to release (max)	5	5	5	5	5	na[5]	na[5]	

Notes:

All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).

3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

5) IORDY is not supported in this mode.

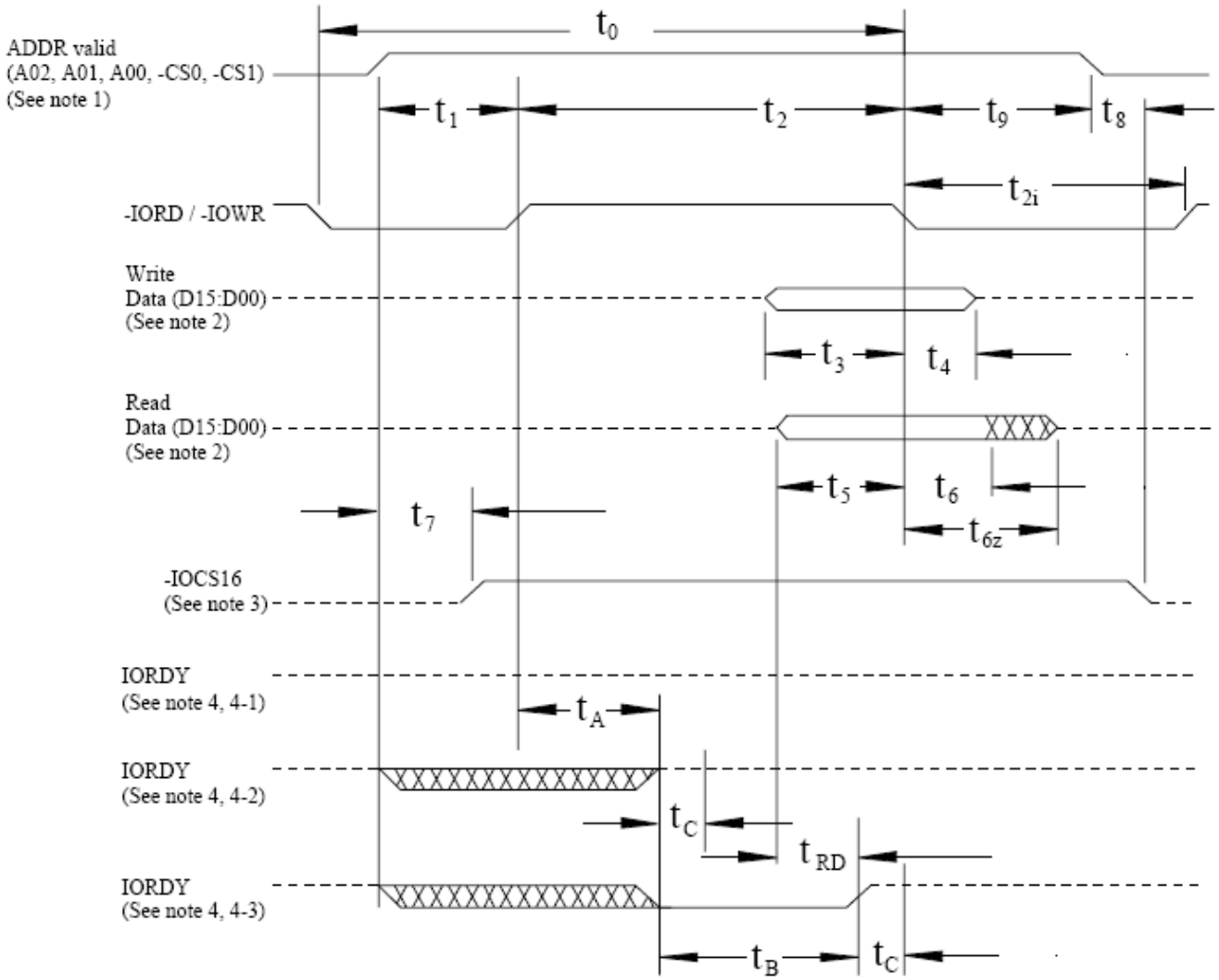


Figure 3-7: True IDE PIO Mode Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

1) Device address consists of -CS0, -CS1, and A[02::00]
2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
   4-1) Device never negates IORDY: No wait is generated.
   4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
   4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles
   where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

3.3.12 True IDE Multiword DMA Mode Read/Write Timing Specification

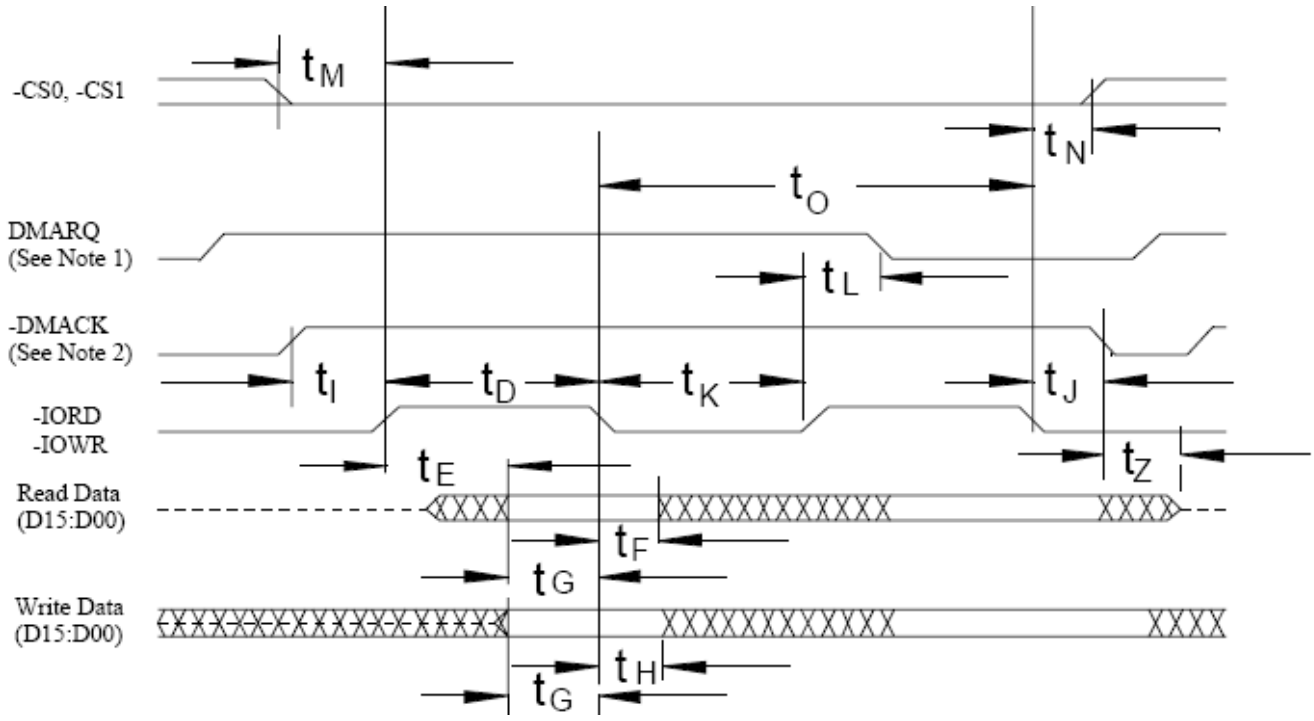
The timing diagram for True IDE DMA mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 3-17: True IDE Multiword DMA Mode Read/Write Timing

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Note
tO	Cycle time (min)	480	150	120	100	80	1
tD	-IORD / -IOWR asserted width (min)	215	80	70	65	55	1
tE	-IORD data access (max)	150	60	50	50	45	
tF	-IORD data hold (min)	5	5	5	5	5	
tG	-IORD/-IOWR data setup (min)	100	30	20	15	10	
tH	-IOWR data hold (min)	20	15	10	5	5	
tI	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0	
tJ	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5	
tKR	-IORD negated width (min)	50	50	25	25	20	1
tKW	-IOWR negated width (min)	215	50	25	25	20	1
tLR	-IORD to DMARQ delay (max)	120	40	35	35	35	
tLW	-IOWR to DMARQ delay (max)	40	40	35	35	35	
tM	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5	
tN	CS(1:0) hold	15	10	10	10	10	
tZ	-DMACK	20	25	25	25	25	

Notes:

1) t0 is the minimum total cycle time and tD is the minimum command active time, while tKR and tKW are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tKR, and tKW shall be met. The minimum total cycle time requirement is greater than the sum of tD and tKR or tKW.for input and output cycles respectively. This means a host implementation can lengthen either or both of tD and either of tKR, and tKW as needed to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.



Notes:

(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

(2) This signal may be negated by the host to suspend the DMA transfer in progress.

Figure 3-8: True IDE Multiword DMA Mode Read/Write Timing Diagram

3.3.13 Ultra DMA Mode Read/Write Timing Specification

Ultra DMA Overview

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g., Command Block Register access).

Ultra DMA operations can take place in any of the three basic interface modes: PC Card Memory mode, PC Card I/O mode, and True IDE (the original mode to support UDMA). The usage of signals in each of the modes is shown in Table 3-18:Ultra DMA Signal Usage In Each Interface Mode

Table 3-18:Ultra DMA Signal Usage In Each Interface Mode

UDMA Signal	Type	Pin # (Non UDMA MEM MODE)	PC CARD MEM MODE UDMA	PC CARD IO MODE UDMA	TRUE IDE MODE UDMA
DMARQ	Output	43 (-INPACK)	-DMARQ	-DMARQ	DMARQ
DMACK	Input	44 (-REG)	-DMACK	DMACK	-DMACK
STOP	Input	35 (-IOWR)	STOP 1	STOP 1	STOP 1
HDMARDY(R) HSTROBE(W)	Input	34 (-IORD)	-HDMARDY(R) 1, 2HSTROBE(W) 1, 3, 4	-HDMARDY(R) 1, 2 HSTROBE(W) 1, 3, 4	-HDMARDY(R) 1, 2 HSTROBE(W) 1, 3, 4
DDMARDY(W) DSTROBE(R)	Output	42 (-WAIT)	-DDMARDY(W) 1, 3DSTROBE(R) 1. 2. 4	-DDMARDY(W) 1, 3 DSTROBE(R) 1. 2. 4	-DDMARDY(W) 1, 3 DSTROBE(R) 1. 2. 4
DATA	Bidir	… (D[15:00])	D[15:00]	D[15:00]	D[15:00]
ADDRESS	Input	… (A[10:00])	A[10:00]	A[10:00]	A[02:00] 5
CSEL	Input	39 (-CSEL)	-CSEL	-CSEL	-CSEL
INTRQ	Output	37 (READY)	READY	-INTRQ	INTRQ
Card Select	Input	7 (-CE1) 31 (-CE2)	-CE1 -CE2	-CE1 -CE2	-CS0 -CS1

Notes:

1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
2) The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.
3) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.
4) The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.
5) Address lines 03 through 10 are not used in True IDE mode.

Ultra DMA Data Transfers Timing

Table 3-19 and Table 3-20 define the timings associated with all phases of Ultra DMA data bursts.

Table 3-19: Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		UDMA Mode 5		Measure location[2]
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t2CYCTYP	240		160		120		90		60		40		Sender
tCYC	112		73		54		39		25		16.8		Note 3
t2CYC	230		153		115		86		57		38		Sender
tDS	15.0		10.0		7.0		7.0		5.0		4.0		Recipient
tDH	5.0		5.0		5.0		5.0		5.0		4.6		Recipient
tDVS	70.0		48.0		31.0		20.0		6.7		4.8		Sender
tDVH	6.2		6.2		6.2		6.2		6.2		4.8		Sender
tCS	15.0		10.0		7.0		7.0		5.0		5.0		Device
tCH	5.0		5.0		5.0		5.0		5.0		5.0		Device
tCVS	70.0		48.0		31.0		20.0		6.7		10.0		Host
tCVH	6.2		6.2		6.2		6.2		6.2		10.0		Host
tZFS	0		0		0		0		0		35		Device
tDZFS	70.0		48.0		31.0		20.0		6.7		25		Sender
tFS		230		200		170		130		120		90	Device
tLI	0	150	0	150	0	150	0	100	0	100	0	75	Note 4
tMLI	20		20		20		20		20		20		Host
tUI	0		0		0		0		0		0		Host
tAZ		10		10		10		10		10		10	Note 5
tZAH	20		20		20		20		20		20		Host
tZAD	0		0		0		0		0		0		Device
tENV	20	70	20	70	20	70	20	55	20	55	20	50	Host
tRFS		75		70		60		60		60		50	Sender
tRP	160		125		100		100		100		85		Recipient
tIORDYZ		20		20		20		20		20		20	Device
tZIORDY	0		0		0		0		0		0		Device
tACK	20		20		20		20		20		20		Host
tSS	50		50		50		50		50		50		Sender

Notes:

All Timings in ns

1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement

location column. For example, in the case of tRFS, both STROBE and -DMARDY transitions are measured at the sender connector.

3) The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

4) The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5) The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

6) See the AC Timing requirements in Table 3-21: Ultra DMA AC Signal Requirements.

Table 3-20: Ultra DMA Data Burst Timing Descriptions

NAME	COMMENT	NOTES
t2CYCTYP	Typical sustained average two cycle time	
tCYC	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t2CYC	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
tDS	Data setup time at recipient (from data valid until STROBE edge)	2, 5
tDH	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
tDVS	Data valid setup time at sender (from data valid until STROBE edge)	3
tDVH	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
tCS	CRC word setup time at device	2
tCH	CRC word hold time device	2
tCVS	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
tCVH	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
tZFS	Time from STROBE output released-to-driving until the first transition of critical timing.	
tDZFS	Time from data output released-to-driving until the first transition of critical timing.	
tFS	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
tLI	Limited interlock time	1
tMLI	Interlock time with minimum	1
tUI	Unlimited interlock time	1
tAZ	Maximum time allowed for output drivers to release (from asserted or negated)	

NAME	COMMENT	NOTES
tZAH	Minimum delay time required for output	
tZAD	drivers to assert or negate (from released)	
tENV	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
tRFS	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
tRP	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
tIORDYZ	Maximum time before releasing IORDY	6
tZIORDY	Minimum time before driving IORDY	4, 6
tACK	Setup and hold times for -DMACK (before assertion or negation)	
tSS	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

1) The parameters t_{UI}, t_{MLI} (in Figure 3-12: Ultra DMA Data-In Burst Device Termination Timing and Figure 3-13: Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks,i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum.

2) 80-conductor cabling (see 4.3.8.4) shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times inmodes greater than 2.

3) Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

4) For all timing modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

5) The parameters t_{DS}, and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

6) This parameter applies to True IDE mode operation only.

Table 3-21: Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode4 (ns)		UDMA Mode 5 (ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tDSIC	14.7		9.7		6.8		6.8		4.8		2.3	
tDHIC	4.8		4.8		4.8		4.8		4.8		2.8	
tDVSIC	72.9		50.9		33.9		22.6		9.5		6.0	
tDVHIC	9.0		9.0		9.0		9.0		9.0		6.0	
tDSIC	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)											
tDHIC	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)											
tDVSIC	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)											
tDVHIC	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)											

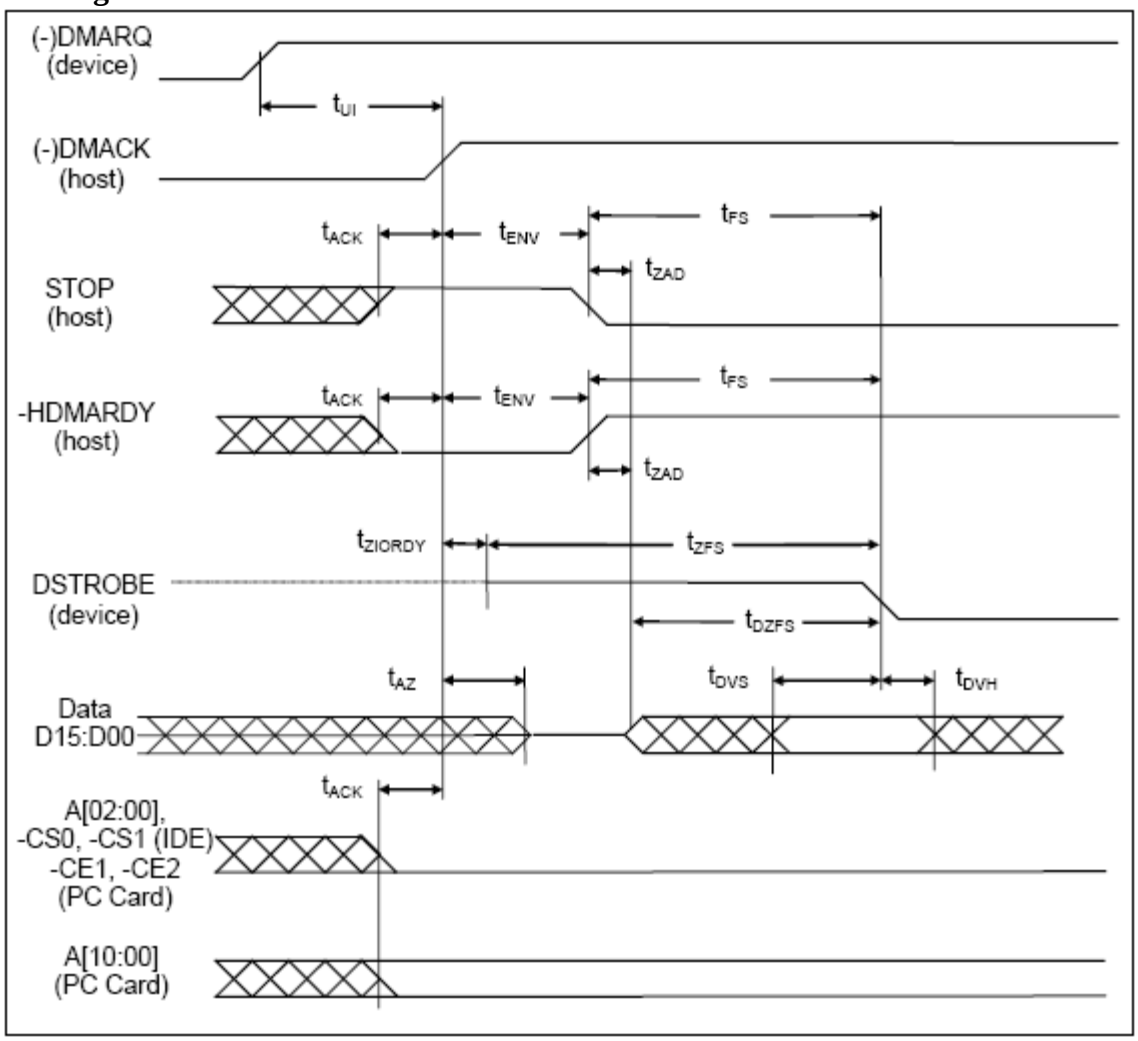
Notes:

1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V.

2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and fal ing and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).

3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Initiating an Ultra DMA Data-In Burst



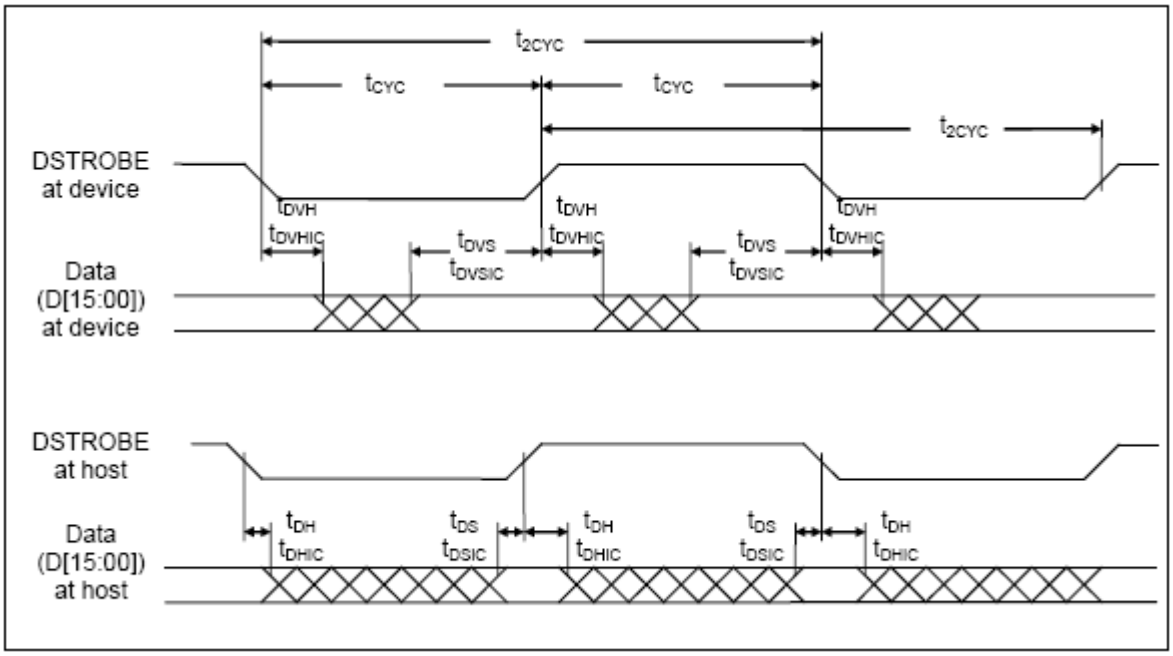
ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signals. The Bus polarity of (-)DMACK and (-)DMARQ are dependent on interface mode active.

Figure 3-9: Ultra DMA Data-In Burst Initiation Timing

Sustaining an Ultra DMA Data-In Burst



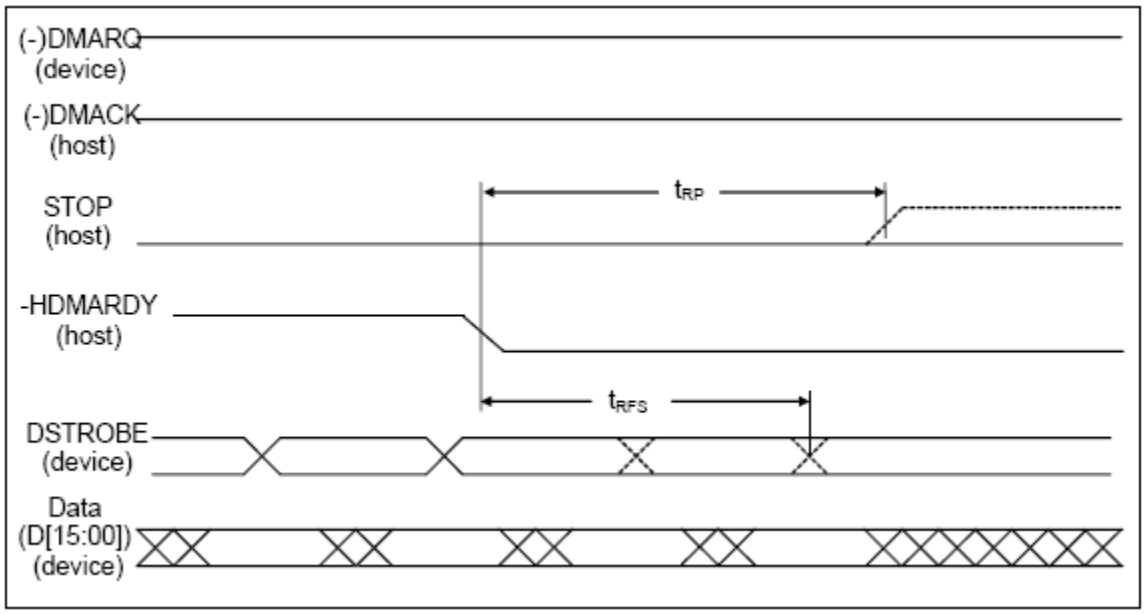
ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

D[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 3-10: Sustained Ultra DMA Data-In Burst Timing

Host Pausing an Ultra DMA Data-In Burst



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

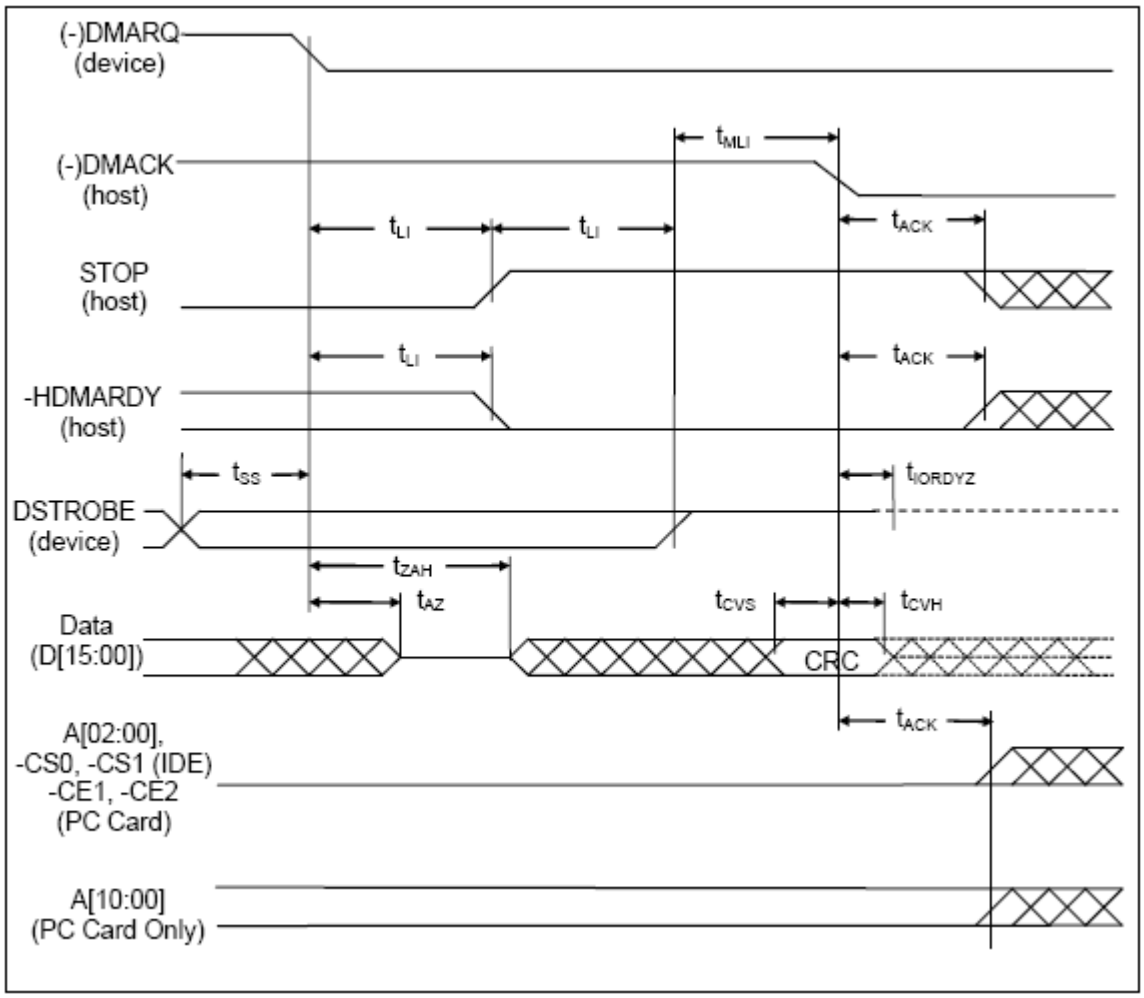
1) The host may assert STOP to request termination of the Ultra DMA data burst no sooner than t_{RP} after -HDMARDY is negated.

2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

3) The bus polarity of the (-) DMARQ and (-)DMACK signals is dependent on the active interface mode.

Figure 3-11: Ultra DMA Data-In Burst Host Pause Timing

Device Terminating an Ultra DMA Data-In Burst



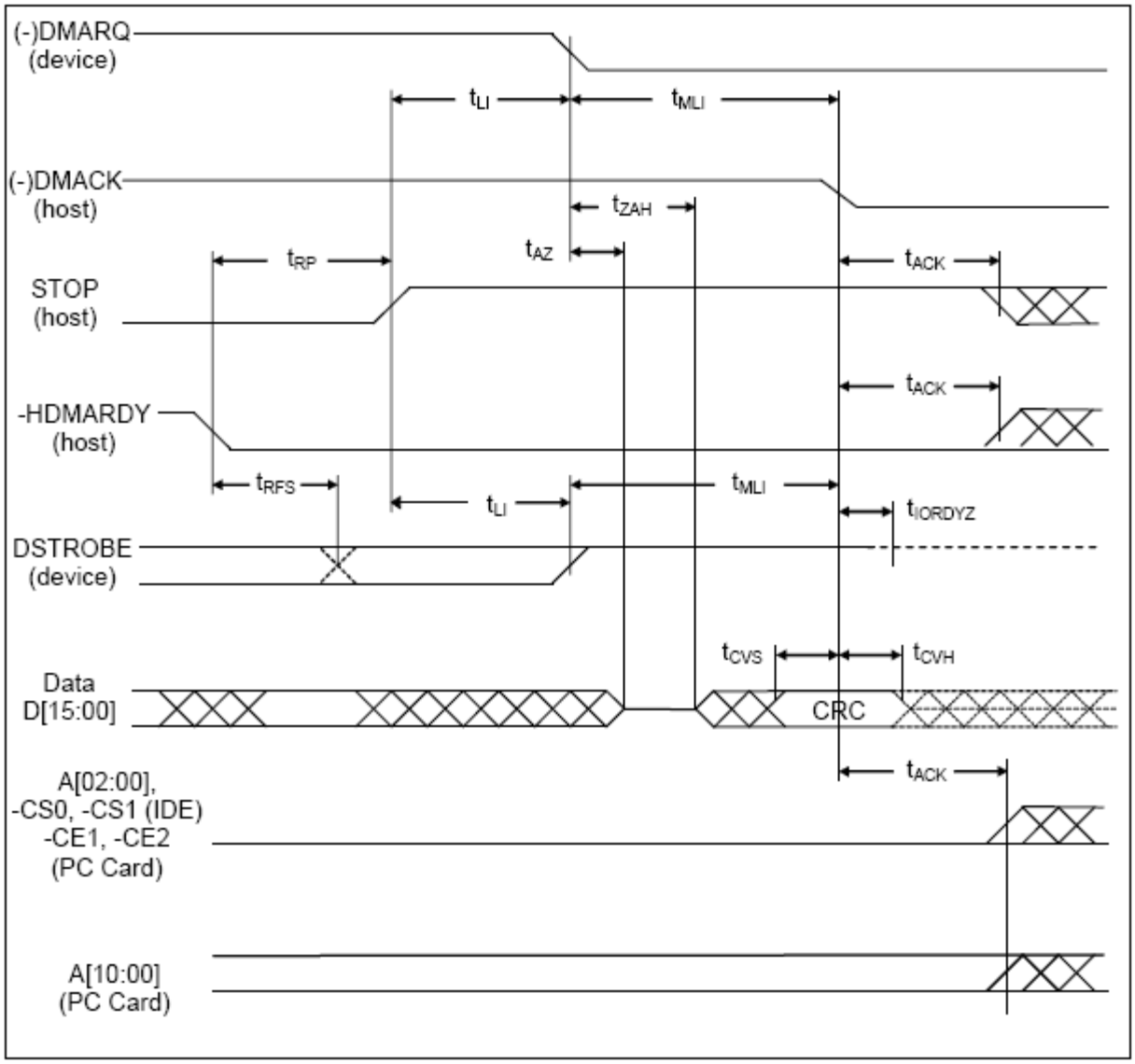
ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO HE DIAGRAM.

Notes:

The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

Figure 3-12: Ultra DMA Data-In Burst Device Termination Timing

Host Terminating an Ultra DMA Data-In Burst



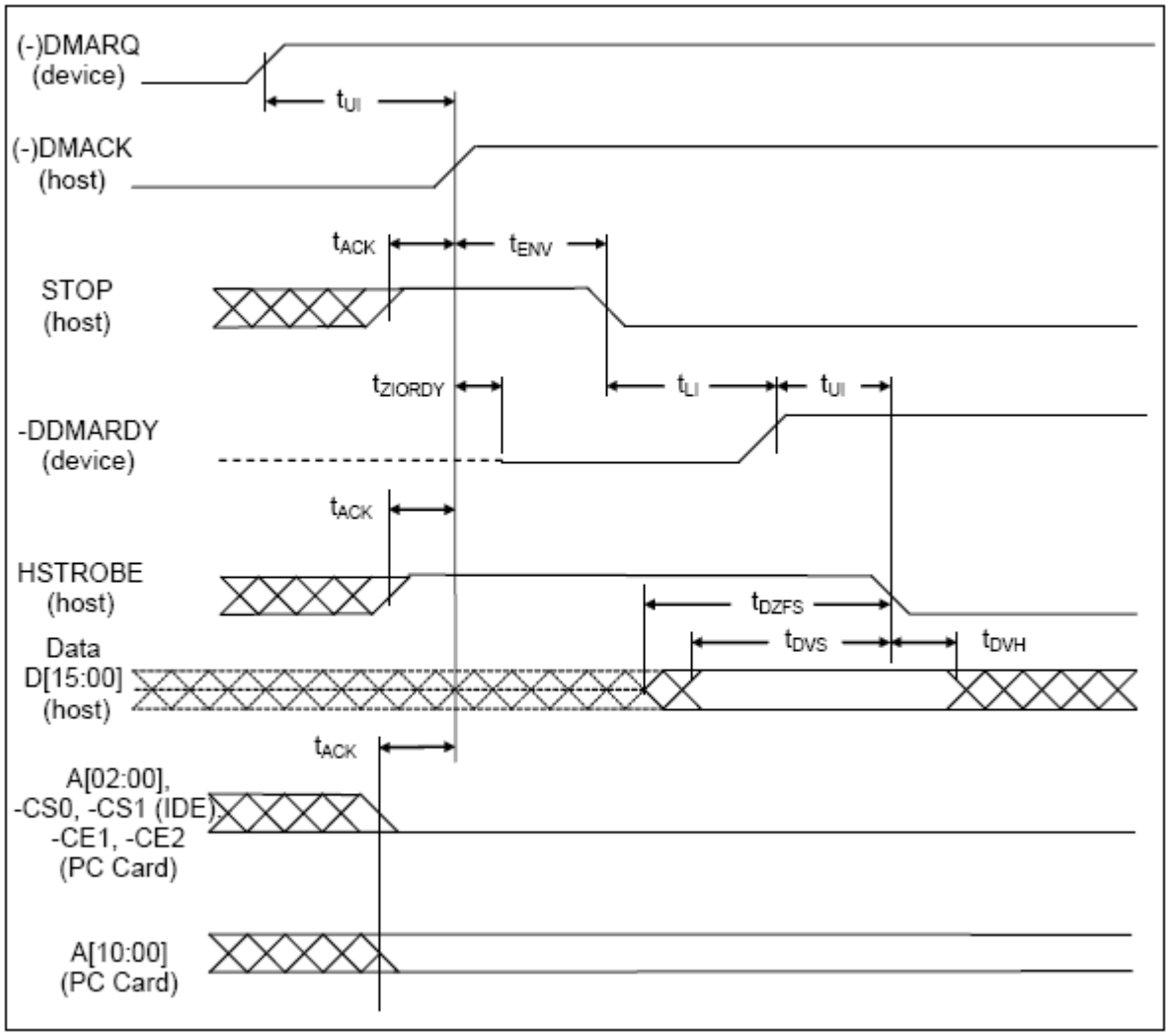
ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 3-13: Ultra DMA Data-In Burst Host Termination Timing

Initiating an Ultra DMA Data-Out Burst



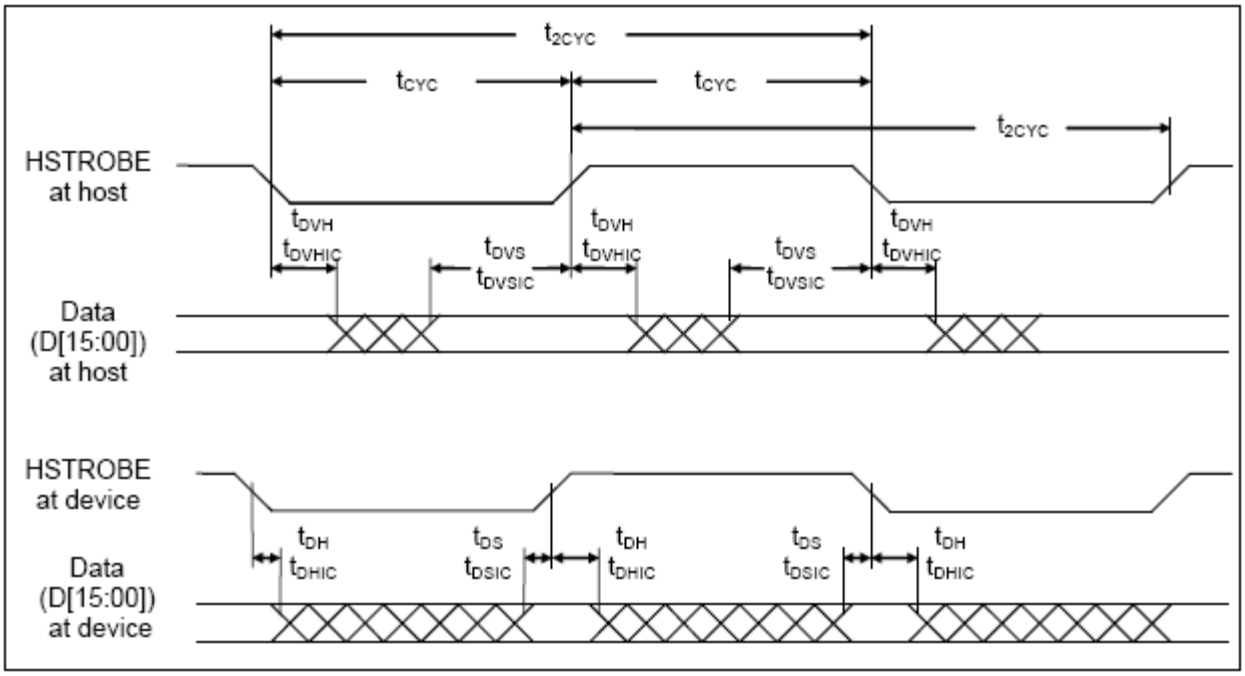
ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note:

The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 3-14: Ultra DMA Data-Out Burst Initiation Timing

Sustaining an Ultra DMA Data-Out Burst



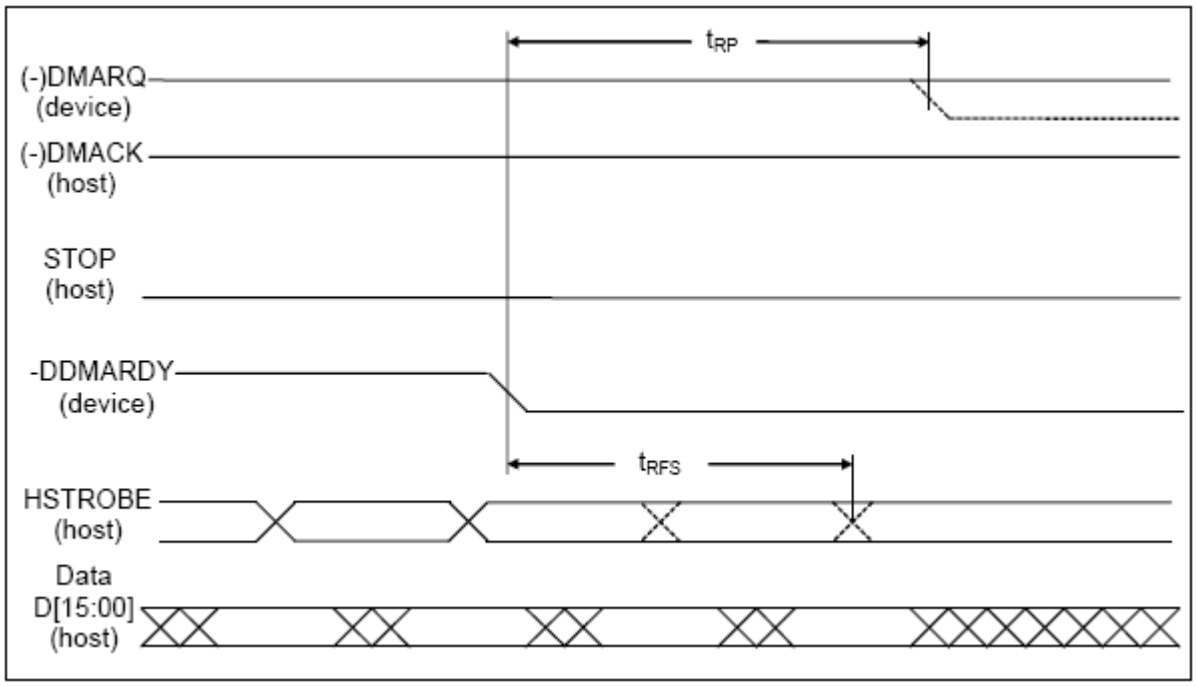
ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note:

Data (D[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not al ow the data signals to be considered stable at the device until some time after they are driven by the host.

Figure 3-15: Sustained Ultra DMA Data-Out Burst Timing

Device Pausing an Ultra DMA Data-Out Burst



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

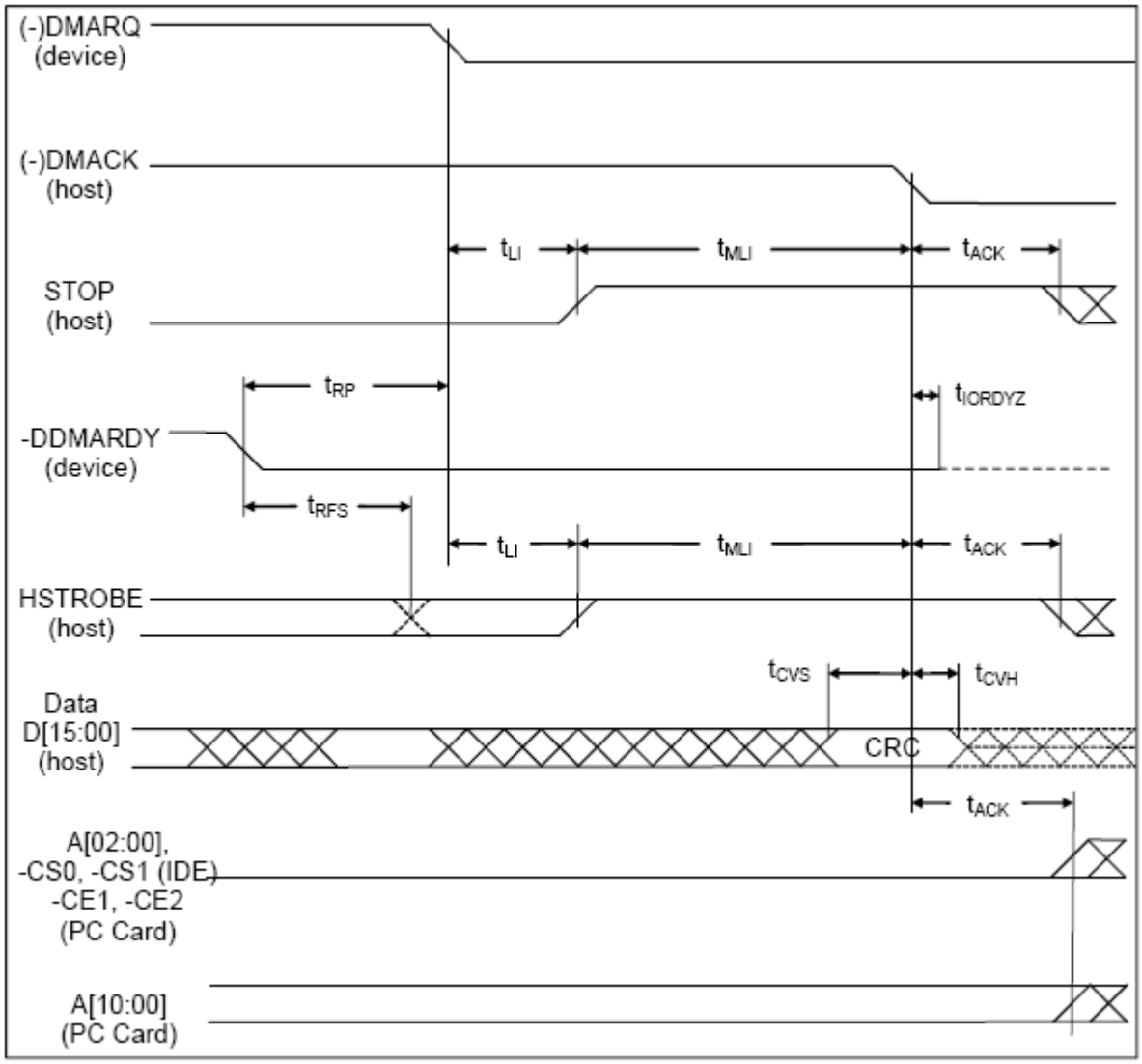
1) The device may negate DMARQ to request termination of the Ultra DMA data burst no sooner than t_{RP} after -DDMARDY is negated.

2) After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

3) The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 3-16: Ultra DMA Data-Out Burst Device Pause Timing

Device Terminating an Ultra DMA Data-Out Burst



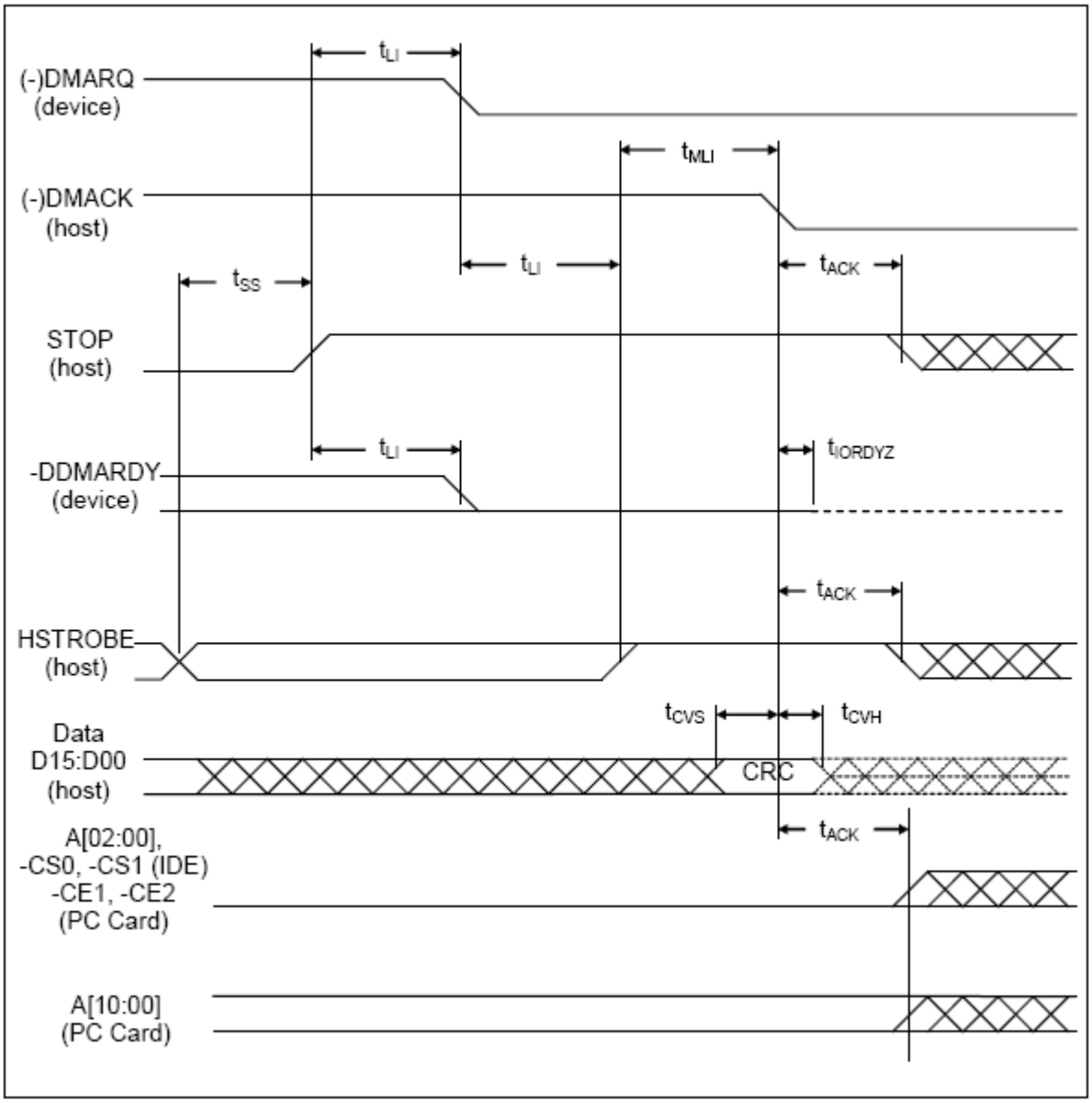
ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note:

The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect afterDMARQ and DMACK are negated. A00-A02, -CS0 & -CS1 are True IDE mode signal definitions. A00-A10, -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 3-17: Ultra DMA Data-Out Burst Device Termination Timing

Host Terminating an Ultra DMA Data-Out Burst



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO HE DIAGRAM.

Notes:

The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 3-18: Ultra DMA Data-Out Burst Host Termination Timing

Ultra DMA CRC Calculation

Table 3-22: Equations for parallel generation of an Ultra DMA CRC

CRCIN0 = f16	CRCIN8 = f8 XOR f13
CRCIN1 = f15	CRCIN9 = f7 XOR f12
CRCIN2 = f14	CRCIN10 = f6 XOR f11
CRCIN3 = f13	CRCIN11 = f5 XOR f10
CRCIN4 = f12	CRCIN12 = f4 XOR f9 XOR f16
CRCIN5 = f11 XOR f16	CRCIN13 = f3 XOR f8 XOR f15
CRCIN6 = f10 XOR f15	CRCIN14 = f2 XOR f7 XOR f14
CRCIN7 = f9 XOR f14	CRCIN15 = f1 XOR f6 XOR f13
f1 = D00 XOR CRCOUT15	f9 = D08 XOR CRCOUT7 XOR f5
f2 = D01 XOR CRCOUT14	f10 = D09 XOR CRCOUT6 XOR f6
f3 = D02 XOR CRCOUT13	f11 = D10 XOR CRCOUT5 XOR f7
f4 = D03 XOR CRCOUT12	f12 = D11 XOR CRCOUT4 XOR f1 XOR f8
f5 = D04 XOR CRCOUT11 XOR f1	f13 = D12 XOR CRCOUT3 XOR f2 XOR f9
f6 = D05 XOR CRCOUT10 XOR f2	f14 = D13 XOR CRCOUT2 XOR f3 XOR f10
f7 = D06 XOR CRCOUT9 XOR f3	f15 = D14 XOR CRCOUT1 XOR f4 XOR f11
f8 = D07 XOR CRCOUT8 XOR f4	f16 = D15 XOR CRCOUT0 XOR f5 XOR f12

Notes:

1) f=feedback
2) D[15:0] = Data to or from the bus
3) CRCOUT = 16-bit edge triggered result (current CRC)
4) CRCOUT[15:0] are sent on matching order bits of D[15:00]

An example of a CRC generator implementation is provided below in Figure 3-19: Ultra DMA Parallel CRC Generator Example.

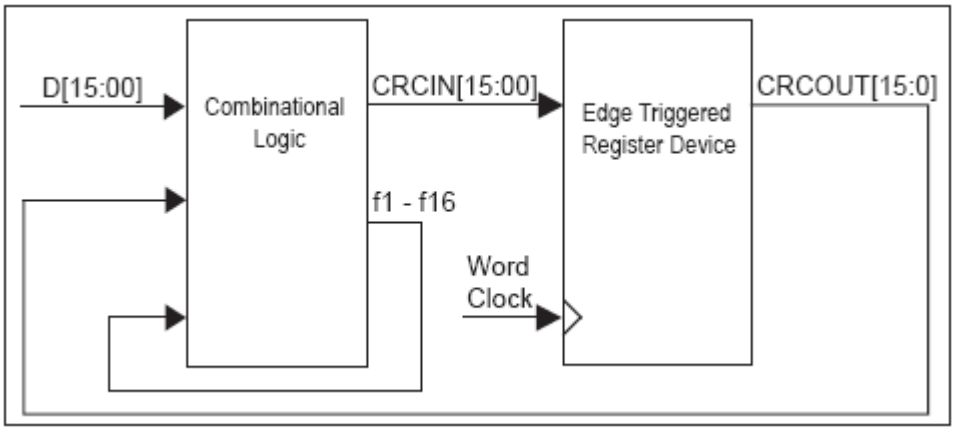


Figure 3-19: Ultra DMA Parallel CRC Generator Example

3.4 Card Configuration

The CompactFlash Storage Cards are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash Storage Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

3.4.1 CompactFlash Storage Card Registers and Memory Space Decoding

Table 3-23: CompactFlash Storage Card Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby and UDMA transfer
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Table 3-24: PC Card Memory Mode UDMA Function

-CE2	-CE1	-DMARQ -INPACK	-DMACK - REG	STOP -IOWR	-DMARDY -IORD (R) -WAIT (W)	STROBE -WAIT (R) -IORD (W)	DMA CMD	A10-A00	OPERATION
1	1	1	X	X	X	X	No	XX	Standby
X	X	0	1	X	X	1	YES	XX	Device UDMA Transfer Request (Assert DMARQ)
X	X	0	1	1	X	1	YES	XX	Host Acknowledge Preparation
1	1	0	1	1	1	1	YES	Static	Host Acknowledge Preparation
1	1	0	0	1	1	1	YES	Static	DMA Acknowledge (Stopped)
1	1	0	0	0	0	1	YES	Static	Burst Initiation / Active
1	1	0	0	0	X	/ or \	YES	Static	Burst Transfer
1	1	0	0	0	1	0 or 1	RD	Static	Data In Burst Host Pause
1	1	0	0	0	0	0 or 1	RD	Static	Data In Burst Device Pause
1	1	0	0	0	1	0 or 1	WR	Static	Data Out Burst Device Pause
1	1	0	0	0	0	0 or 1	WR	Static	Data Out Burst Host Pause
1	1	1	0	0	0	0 or 1	RD	Static	Device Initiating Burst Termination
1	1	1	0	1	1	0 or 1	RD	Static	Host Acknowledgement of Device Initiated Burst Termination
1	1	0	0	1	0	0 or 1	YES	Static	Host Initiating Burst Termination
1	1	1	0	1	1	0 or 1	YES	Static	Device Acknowledging Host Initiated Burst Termination
1	1	1	0	1	1	/	YES	Static	Device Aligning STROBE to Asserted before CRC Transfer
1	1	1	/	1	1	1	YES	Static	CRC Data Transfer for UDMA Burst
1	1	1	1	1	1	1	YES	Static	Burst Completed

Table 3-25: CompactFlash Storage Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

3.4.2 Attribute Memory Function

Attribute memory is a space where CompactFlash Storage Card identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the card configuration registers is 200h. For the Attribute Memory Read function, signals -REG and -OE shall be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 3-26: Attribute Memory Function below for signal states and bus validity for the Attribute Memory function.

Table 3-26: Attribute Memory Function

Function Mode	DMA CMD	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	Don't Care	H	H	H	X	X	X	X	X	High Z	High Z
Standby Mode	No	X	H	H	X	X	X	X	X	High Z	High Z
UDMA Operation: Ultra DMA Mode Read/Write Timing Specification)	Yes	L[1]	H	H	X	X	X	H	H	Odd Byte	Even Byte
Read Byte Access CIS ROM (8 bits)	No	L	H	L[2]	L	L	L	L[2]	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	No	L	H	L2	L	L	L	H	L[2]	Don't Care	Even Byte
Read Byte Access Configuration CompactFlash Storage (8 bits)	No	L	H	L	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration CompactFlash Storage (8 bits)	No	L	H	L	L	H	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration CF+ (8 bits)	No	L	H	L	X	X	L	L	H	High Z	Even Byte
Write Byte Access Configuration CF+ (8 bits)	No	L	H	L	X	X	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	No	L	L[2]	L[2]	L	L	X	L[2]	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	No	L	L[2]	L[2]	L	L	X	H	L[2]	Don't Care	Even Byte
Read Word Access Configuration CompactFlash Storage (16 bits)	No	L	L[2]	L[2]	L	H	X	L2	H	Not Valid	Even Byte
Write Word Access Configuration CompactFlash Storage (16 bits)	No	L	L[2]	L[2]	L	H	X	H	L[2]	Don't Care	Even Byte
Read Word Access Configuration CF+ (16 bits)	No	L	L[2]	L[2]	X	X	X	L[2]	H	Not Valid	Even Byte
Write Word Access Configuration CF+ (16 bits)	No	L	L[2]	L[2]	X	X	X	H	L[2]	Don't Care	Even Byte

Note:

1) In UDMA operation, the -REG (-DMACK) signal shall be asserted only in response to -DMARQ.
2) The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.

3.4.3 Configuration Option Register (Base + 00h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash Card.

OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Figure 3-20: Configuration Option Register

Note:

Conf5 and Conf4 are written as zero (0).

Table 3-27: CompactFlash Card Configurations

CONF5	CONF4	CONF3	CONF2	CONF1	CONF0	DISK CARD MODE
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0h-1F7h/3F6h-3F7h
0	0	0	0	1	1	I/O Mapped, 170h-177h/376h-377h

3.4.4 Card Configuration and Status Register (Base + 02h in Attribute Memory)

The Card Configuration and Status Register contains information about the Card's condition.

OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	-XE	Audio	PwrDwn	Int	0
Write	0	SigChg	IOis8	-XE	Audio	PwrDwn	0	0

Figure 3-21: Card Configuration and Status Register

3.4.5 Pin Replacement Register (Base + 04h in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CReady	CWProt	1	1	RReady	WProt
Write	0	0	CReady	CWProt	0	0	MReady	MWProt

Figure 3-22: Pin Replacement Register

Table 3-28: Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final "C" Bit	Comments
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

3.4.6 Socket and Copy Register (Base + 06h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Obsolete1(Drive#)	0	0	0	0
Write	0	0	0	Obsolete1(Drive#)	X	X	X	X

Figure 3-23: Socket and Copy Register

3.5 I/O Transfer Function

The I/O transfer to or from the CompactFlash Storage can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Card, the system shall generate a pair of 8 bit references to access the word's even byte and odd byte. The CompactFlash Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Card responds.

The CompactFlash Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 3-29: PCMCIA Mode I/O Function

FUNCTION CODE	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

3.6 Common Memory Transfer Function

The Common Memory transfer to or from the CompactFlash Storage can be either 8 or 16 bits. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its Common Memory addresses. The CompactFlash Storage Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 3-30: Common Memory Function

FUNCTION CODE	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

3.7 True IDE Mode I/O Transfer Function

The CompactFlash Storage Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. CompactFlash Storage Cards support the following optional detection methods:

1. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to PCMCIA mode upon detecting a high level on the pin.
2. The card is permitted to re-arbitrate the interface mode determination following a transition of the (-)RESET pin.
3. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time. Host implementers should not rely on any of these optional detection methods in their designs. In the True IDE Mode, the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode, no Memory or Attribute Registers are accessible to the host. CompactFlash Storage Cards permit 8 bit PIO mode data accesses if the user issues a Set Feature Command to put the CompactFlash Storage Card in 8 bit Mode.

Note:

Removing and reinserting the CompactFlash Storage Card while the host computer's power is on will reconfigure the CompactFlash Storage Card to PC Card ATA mode from the original True IDE Mode. To configure the CompactFlash Storage Card in True IDE Mode, the 50-pin socket is power cycled with the CompactFlash Storage Card inserted and -OE (output enable) asserted.

Table 3-31: True IDE Mode I/O Function

FUNCTION CODE	-CS1	-CS0	A0-A2	-DMACK	-IORD	-IOWR	D15-D8	D7-D0
Invalid Modes	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined In	Undefined In
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data Out
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address1	L	H	7h	H	L	H	High Z	Data Out

Notes:

1) Implemented for backward compatibility. Bit D7 of the register shall remain High Z to prevent conflict with any floppy disk controller at the same address. The host software should not rely on the contents of this register.

3.8 Host Configuration Requirements for Master/Slave or New Timing Modes

The CF Advanced Timing modes include PCMCIA style I/O modes that are faster than the original 250 ns cycle time. These modes are not supported by the PCMCIA specification nor CF by cards based on revisions of the CF specification before Revision 3.0. Hosts shall ensure that all cards accessed through a common electrical interface are capable of operation at the desired, faster than 250 ns, I/O mode before configuring the interface for that I/O mode.

Advanced Timing modes are PCMCIA style I/O modes that are 100 ns or faster, PCMCIA Memory modes that are 100ns or faster, True IDE PIO Modes 5,6 and Multiword DMA Modes 3,4. These modes are permitted to be used only when a single card is present and the host and card are connected directly, without a cable exceeding 0.15m in length. Consequently, the host shall not configure a card into an Advanced Timing Mode if two cards are sharing I/O lines, as in Master/Slave operation, nor if it is constructed such that a cable exceeding 0.15 meters is required to connect the host to the card.

The load presented to the Host by cards supporting Ultra DMA is more controlled than that presented by other CompactFlash cards. Therefore, the use of a card that does not support Ultra DMA in a Master/Slave arrangement with a Ultra DMA card can affect the critical timing of the Ultra DMA transfers. The host shall not configure a card into Ultra DMA mode when a card not supporting Ultra DMA is also present on the same interface

When the use of two cards on an interface is otherwise permitted, the host may use any mode that is supported by both cards, but to achieve maximum performance it should use its highest performance mode that is also supported by both cards.

3.9 Termination Resistors for Ultra DMA Operation

ATP Industrial Grade CF cards provide embedded termination resistors for operation in any of the Ultra DMA modes. The following table describes typical values for series termination at the CF card.

Table 3-2: Termination Resistors for Ultra DMA Operation

Signal	Termination
-IORD (-HDMARDY, HSTROBE)	82 ohm
-IOWR (STOP)	82 ohm
-CS0, -CS1	82 ohm
A00, A01, A02	82 ohm
-DMACK	82 ohm
D15 through D00	33 ohm
DMARQ	22 ohm
INTRQ	22 ohm
IORDY (-DDMARDY, DSTROBE)	22 ohm
-RESET	82 ohm

4 S.M.A.R.T. Function

4.1 S.M.A.R.T. Feature

Self-monitoring analysis and reporting technology (S.M.A.R.T.) is used to protect the user from unscheduled downtime. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T. feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Informing the host system of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action.

4.2 S.M.A.R.T. Feature Register Values

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T .Function Set command. The subcommands are listed below.

Table 4-2: S.M.A.R.T. Feature Register Values

Command	Command Code
S.M.A.R.T. READ DATA	D0h
S.M.A.R.T. READ ATTRIBUTE THRESHOLD	D1h
S.M.A.R.T. ENABLE/DISABLE AUTOSAVE	D2h
S.M.A.R.T. SAVE ATTRIBUTE VALUES	D3h
S.M.A.R.T. EXECUTE OFF-LINE IMMIDIATE	D4h
RESERVED	D5h
RESERVED	D6h
S.M.A.R.T. ENABLE OPERATIONS	D8h
S.M.A.R.T. DISABLE OPERATIONS	D9h
S.M.A.R.T. RETURN STATUS	DAh

Note:

If the reserved size is below a threshold, status can be read from the Cylinder Register using the Return Status command (DAh)

4.3 S.M.A.R.T. Data Structure

The following 512 bytes make up the device S.M.A.R.T. data structure. Users can obtain the data using the "Read Data" command (D0h).

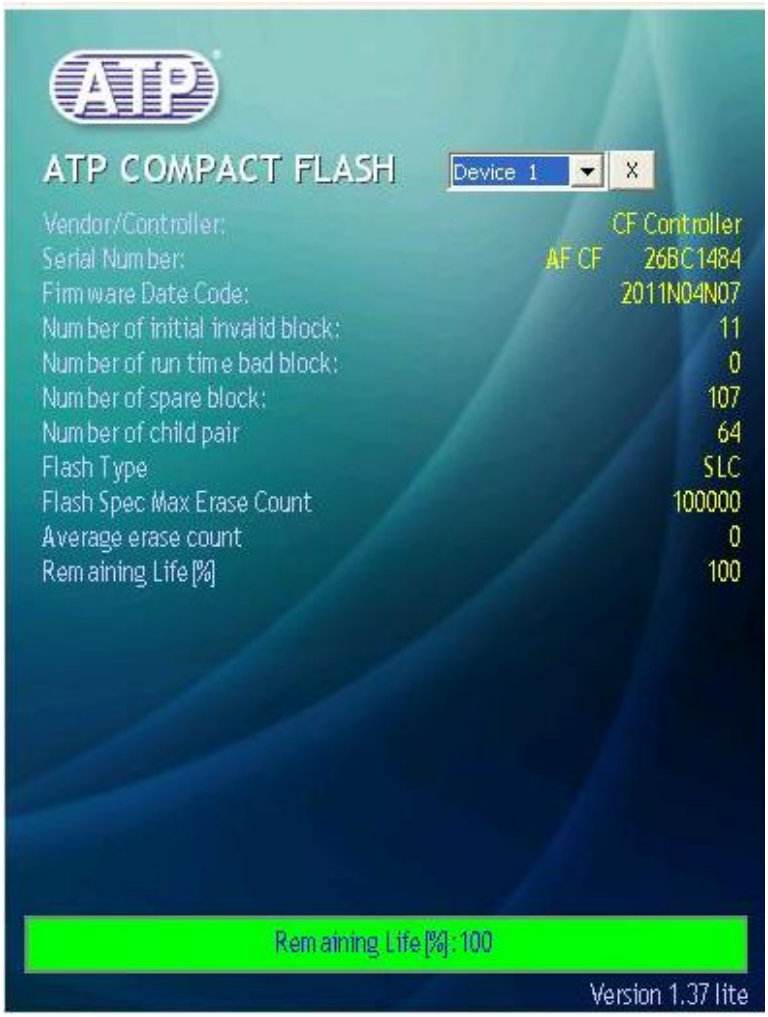
Table 4-3: S.M.A.R.T. Data Structure

Byte	F/V	Description
0~1	X	Revision code
115~116	V	Power Cycle count of the device
362	V	Off-line data collection status
363	X	Self-test execution status byte
364~365	V	Total time in seconds to complete off-line data collection activity
367	F	Off-line data collection capability
368~369	F	S.M.A.R.T. capability
370	F	Error logging capability：7-1 Reserved 0 1 = Device error logging supported
372	F	Short self-test routine recommended polling time(in minutes)
373	F	Extended self-test routine recommended polling time(in minutes)
374	F	Conveyance self-test routine recommended polling time(in minutes)
375~385	R	Reserved
386~395	F	Firmware Version/Date Code
396~397	F	Number of initial invalid block (396=MSB, 397=LSB)
398~399	V	Number of run time bad block (398=MSB, 399=LSB)
400	V	Number of spare block
401~402	V	Erase count (Low word. The value is identical to that of Byte 409~410)
403~405	F	'SMI"
406	F	Number of max pair
407~410	V	Erase count (407~408 =High word, 409~410 =Low word)
511	V	Data structure checksum

Notes:
F=content (byte) is fixed and does not change
V=content (byte) is variable and maybe change depending on the state of the device or the command executed by the device
X= content (byte) is vendor specific and maybe fixed or variable
R=content (byte) is reserved and shall be zero
N=Nth Management Unit
*4 Byte value: [MSB][2][1][LSB]

4.4 ATP S.M.A.R.T. Tool

ATP provides S.M.A.R.T. Tool for Windows 2000/XP/Vista/7 and Linux, It can monitor the state of Industrial Grad CompactFlash, and the following picture shows S.M.A.R.T. tool operation. This tool supports that users read spare and bad block information. Users can thus evaluate drive health at run time and receive an early warning before the drive life ends.



Note: Please contact ATP sales or visit ATP website for the updated ATP S.M.A.R.T. tool version.

ATP Electronics Inc.
TEL: +1-408-732-5000
FAX: +1-408-732-5055
sales@atpinc.com
750 North Mary Ave. Sunnyvale, CA 94085 USA

ATP Electronics Europe B.V.
TEL: +31-88-287-0000
FAX: +31-88-287-0099
sales-europe@atpinc.com
Corkstraat 46, Rotterdam 3047 AC, The Netherlands

ATP Electronics Tokyo Office
TEL: +81-03-6206-8097
FAX: +81-03-6206-8098
sales-japan@atpinc.com
www.atpinc.co.jp
#1007, 10F, 1-8-4 Kandasakuma-cho, Chiyoda-ku, Tokyo

ATP Electronics (Shanghai), Inc.
TEL: +86-21-5080-2220
FAX: +86-21-5080-2219
sales@cn.atpinc.com
www.atpinc.com.cn
Room 102, No.500 BiBo road, Zhangjiang High-tech park, Shanghai, China, 201203